PROMISE®
TECHNOLOGY, INC.

PDC20621

PCI Bus Mastering

ATA RAID Accelerator

Programming Guide for

PLL & ATA Timing

Powered by PROMISE ATA RAID

For Development Reference

Revision 1.2

1. General Description

PDC20621 can be used for FastTRAK100, SuperTRAK100 and others applicable application. At the controller initial stage, a PLL base clock synthesizer that refer to PCI clock to generate internal clock, must be programmed to generate appropriate clock for ASIC internal reference. Two type of clock frequency should be choosing that dependent on what type of DIMM modules supported. If any PC66 DIMM module is detected, then the internal clock must be programmed to 66MHz and ATA only support up to Ultra66. If any DIMM modules support PC100, the internal clock of PDC20621 must be programmed to 100MHz in all applications. If all DIMM modules support PC133, the internal clock of PDC20621 must be programmed to 100MHz in all applications.

2. PLL & ATA Timing Programming Sequence

1. Read SPD0/SPD1, and check whether any of DIMM modules support PC66/PC100.
2. If there is any DIMM module that supports only PC66, then 66 MHz clock is used for controller reference. If there is any DIMM module that supports only PC100, then100MHz clock is used for controller reference. Otherwise, 120 MHz internal system clock should be used.
3. Set Feature PIO Mode for existing drives.
4. Set Feature DMA Mode for existing drives.
5. If uses 66/120 MHz for controller reference, then program “ATA Configuration and Timing Control Register” (PIO/DMA/UDMA Timing Parameter).
6. Detect PCI clock frequency.
7. If uses 66 MHz for controller reference, then program “PLL Register “ for 66 MHz. If uses 100 MHz for controller reference, then program “PLL Register “ for 100 MHz. Otherwise, program “PLL Register” for 120MHz.
8. Based on PCI clock frequency then to program PLL Control Register F Parameter.
9. Program PLL Control Register OD, R Parameter.
10. Wait while PLL stable.

3. PLL Table

When PCI clock is not fixed to 66 MHz, any PC66 DIMM module is detected, or all DIMM modules support PC133, PLL must be programmed to generate an appropriate internal clock for ASIC reference. The programming table as follows:

PCI Control & Status register (index_CID0: 8h | BA#3 + C0008h)

PLL parameter	OD	R	F
120 MHz Internal System Clock	0x2	0x04	1440000/(Internal_Clock*330) - 2
100 MHz Internal System Clock	0x2	0x05	1400000/(Internal_Clock*330) – 2
66 MHz Internal System Clock	0x1	0x04	1584000/(Internal_Clock*330) – 2

4. How to Determine the Clock Frequency

1. Program Time Period Register (index_CID0: 40h | BA#3 + C0040h).
   Tperiod = 0xFFFFFFFF.
2. Program Time Control Register (index_CID0: 3Ch | BA#3 +C003Ch).
   Tcontrol = 0x00001a0.
3. Wait a moment (TWAIT). If the input clock is 33MHz, the counter will overflow after
   (2^32)/(50*10^6) = 85.9 sec.
4. Read Time Counter Register (index_CID0: 44h | BA#3 + C0044h).
5. Calculate the clock speed. The calculating method as follows:
   Internal_Clock = (Tperiod-Tcount) / (TWAIT * 10^6)
   F = 144000/ (Internal_Clock*33) –2
   R = 0x04
   OD = 0x2 When we program PLL to 120MHz
   or
   F = 140000/ (Internal_Clock*33) –2
   R = 0x05
   OD = 0x2 When we program PLL to 100MHz
   or
   F = 158400/ (Internal_Clock*33) –2
   R = 0x04
   OD = 0x01 When we program PLL to 66MHz
6. If we want to get more precise, it will turn to
   10*Internal_Clock = (Tperiod- Tcount) / (TWAIT * 10^5)
   F = 1440000 / (10*Internal_Clock*33) –2
   R = 0x04
   OD = 0x2 When we program PLL to 100MHz
   or

F = 1400000 / (10*Internal_Clock*33) –2
R = 0x05
OD = 0x2 When we program PLL to 100MHz
or
F = 1584000/ (10*Internal_Clock*33) –2
R = 0x04
OD = 0x1 When we program PLL to 66MHz

Example (All of DIMM modules support PC100):

1. Program Tperiod as "0xFFFFFFFF"
2. Program Tcontrol as "0x000001a0".
3. Wait 3 second(Twait is 3).
4. Read Tcount.
   If PCI is 66MHz, Tcount should be "0xFFFFFFFF- 3x10^8" approximately.
5. If the Tcount is "0xFFFFFFFF- 3x10^8", then the internal clock is 100MHz.
6. The PLL parameters are as follows:
   F=1400000/33000 –2 = 40
   R= 0x05
   OD = 0x02
7. The new internal clock is 99MHz.
   Internal_clock = ((F+2)*PCI_clock)/(4*(R+2)) When OD = 0x02.
   Internal_clock = ((F+2)*PCI_clock)/(8*(R+2)) When OD = 0x01.

5. ATA Timing Table that Based on 120MHz controller Clock

If all DIMM modules support PC133 after DIMM detection procedure, please program PLL to generate 120 MHz for controller reference and ATA should be programmed using this recommended blue-mark value.

ATA Configuration and Timing Control Register (Index0: C, D, 13 & Index0: 14,15,1B & Index1:C, D, 13 & Index1: 14, 15, 1B)

PIO Mode	PIO mode IORDY	TPENV	TPRCYC/TPDCYC	TPRCV
0	0	208 (70)	336 (290) (Timing Required)	56 (30)
	0	25	41/41 (Program value in dec.)	6
1	0	56 (50)	304 (290)	24 (20)
	0	6	37/37	2

2	0	32 (30)	296/192 (290/100)	16 (15)
	0	3	36/23	1
3	1	60 (30)	104 (80)	16 (10)
	1	7	12/12	1
4	1	32 (25)	72 (70)	16 (10)
	1	3	8/8	1

ATA Configuration and Timing Control Register (Index0: E, F & Index0: 16, 17 & Index1:E, F & Index1: 16, 17)

MDMA Mode	TDENV	TDCYCL	TDCYCH	TDN
0	56 (50)	480 (480)		24 (20)
		240 (215)	240 (215)	
	6	29	29	2
1	32 (30)	150 (150)		16 (15)
		88 (80)	64 (50)	
	3	10	7	1
2	32 (25)	120 (120)		16 (10)
		72 (70)	48 (25)	
	3	8	5	1

ATA Configuration and Timing Control Register (Index0: 10, 11, 12 & Index0: 18, 19, 1A & Index1: 10, 11, 12 & Index1: 18, 19, 1A)

UDMA Mode	TSS	TRP	TCYC/TCYC2	TMLI	TENV	TACK	tHOLD
0	56 (50)	168 (160)	120/240 (112/120)	72 (70)	24 (20)	24 (20)	0
	6	20	14	8	2	2	0
1	56 (50)	128 (125)	80/160 (73/160)	56 (48)	24 (20)	24 (20)	0
	6	15	9	6	2	2	0
2	56 (50)	104 (100)	64/128 (54/120)	40 (30)	24 (20)	24 20)	0
(Ultra33)	6	12	7	4	2	2	0
3	56 (50)	104 (100)	48/96 (39/90)	24 (20)	24 (20)	24 (20)	0
	6	12	5	2	2	2	0
4	56 (50)	104 (100)	32/64 (25/60)	24 (20)	24 (20)	24 (20)	0
(Ultra66)	6	12	3	2	2	2	0
5	56 (50)	88 (85)	24/48 (17/40)	24 (20)	24 (20)	24 (20)	0
(Ultra100)	6	10	2	2	2	2	0
6	***56 (50)***	***88 (85)***	***16/32 (13/30)***	***24 (20)***	***24 (20)***	***24 (20)***	***0***
(Ultra133)	***6***	***10***	***1***	***2***	***2***	***2***	***0***

6. ATA Timing Table that Based on 66MHz controller Clock

If any PC66 DIMM module is detected after DIMM detection procedure, please program PLL to generate 66 MHz for controller reference and ATA should be programmed using this recommended blue-mark value.

ATA Configuration and Timing Control Register0/1 (Index_IDEx:4Ch, ndex_IDEx:50h)

PIO Mode	PIO mode IORDY	TPENV	TPRCYC/TPDCYC	TPRCV
0	0	210 (70)	330 (290) (Timing Required)	60 (30)
	0	13	21/21 (Program value in dec.)	3
1	0	60 (50)	300 (290)	30 (20)
	0	3	19/19	1
2	0	30 (30)	300/180 (290/100)	30 (15)
	0	1	19/11	1
3	1	45 (30)	105 (80)	30 (10)
	1	2	6/6	1
4	1	30 (25)	75 (70)	30 (10)
	1	1	4/4	1

ATA Configuration and Timing Control Register0 (Index_IDEx:50h)

MDMA Mode	TDENV	TDCYCL	TDCYCH	TDN
0	60 (50)	480 (480)		30 (20)
		240 (215)	240 (215)	
	3	15	15	1
1	30 (30)	150 (150)		30 (15)
		90 (80)	60 (50)	
	1	5	3	1
2	30 (25)	120 (120)		30 (10)
		75 (70)	45 (25)	
	1	4	2	1

ATA Configuration and Timing Control Register1 (Index_IDEx:4Ch)

UDMA Mode	TSS	TRP	TCYC/TCYC2	TMLI	TENV	TACK	tHOLD
0	60 (50)	165 (160)	120/240 (112/120)	75 (70)	30 (20)	30 (20)	0
	3	10	7	4	1	1	0
1	60 (50)	135 (125)	90/180 (73/160)	60 (48)	30 (20)	30 (20)	0
	3	8	5	3	1	1	0
2	60 (50)	105 (100)	60/120 (54/120)	45 (30)	30 (20)	30 20)	0
(Ultra33)	3	6	3	2	1	1	0
3	60 (50)	105 (100)	45/90 (39/90)	30 (20)	30 (20)	30 (20)	0
	3	6	2	1	1	1	0
4	60 (50)	105 (100)	30/60 (25/60)	30 (20)	30 (20)	30 (20)	0
(Ultra66)	3	6	1	1	1	1	0