Sil-DS-0095-B2
Revision B2
June, 2003

Sil3112A
PCI to Serial ATA Controller

MSL™ Technology
SATALink™

Silicon Image

Datasheet
- Confidential –

NDA Required

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PCI LOCAL BUS

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Revision History:

Version	Comment	Date
Rev. A	First draft (derived from SiI3112 Data Sheet)	8/22/02
Rev. A1	Changed Absolute Maximum rating Voltage for VDDDO, VDDD and VDDI - Table 2-1 – Added VDDD in the DC specification – Table 2-2 – Changed VDDI (1.8 +/- 0.09 Volt) form (1.8 +/- 0.2 Volt) – Pin Descriptions -	8/27/02
Rev. A2	Revised Power supply current value Added pin 4 description Revised Table 3-1 SiI3112A Pin Listing	10/28/02
Rev. A3	Added Table 2-3 SATA Interface DC Specifications Added Table 2-4 SATA Interface Timing Specifications Added Table 2-5 SATA Interface Transmitter Output Jitter Characteristics Added Table 2-6 CLKI SerDes Reference Clock Input Requirements Removed Section 2-7 Power Supply Bypass Considerations Changed pin name for pin number 4 from SCAN_CK to NC	11/25/02
Rev. B	Removed CleanupAndRequestSense command code 13h from supported command list Defined RJ_{250UI}, DJ_{250UI} in Table 2-5 SATA Interface Transmitter Output Jitter Characteristics Updated 7.2. Serial ATA Device Initialization Removed Memory Write and Invalidate (Memory Write) support from PCI bus target operations	1/15/03
Rev. B1	Removed WriteFPDMAQueued and ReadFPDMAQueued command from supported command list Added the description for bit 21 in BAR5 offset 144_H SATA PHY Configuration Register Added the register description for BAR5 offset 98_H/$D8_H$ IDE Extebded Task File Register – Command Buffering Changed the desctiption for bit 16 in BAR5 offset 48_H System Configuration Status Corrected inconsistence sentence (minor fixed including miss typing) Changed the reset value for Flash memory address – command + status, EEPROM memory address – command + status register	4/9/03
Rev. B2	Changed the rating for VIN in Table 2-1 Absolute Maxmum rating	6/30/03

1 Overview

The Silicon Image SiI3112A is a single-chip solution for a PCI to Serial ATA controller. It accepts host commands through the PCI bus, processes them and transfers data between the host and Serial ATA devices. It can be used to control two independent Serial ATA channels. Each channel has its own Serial ATA bus and will support one Serial ATA device. The SiI3112A supports a 32-bit 66 MHz PCI bus and the Serial ATA Generation 1 transfer rate of 1.5 Gb/s (150 MB/s).

1.1 Key Benefits

The Silicon Image SiI3112A PCI to Serial ATA Controller is the perfect single-chip solution for designs that need to accommodate storage peripherals with the new Serial ATA interface. Any system with a PCI bus interface can simply add the Serial ATA interface by adding a card with the SiI3112A and loading the driver into the system.

The SiI3112A comes complete with drivers for Windows 98, Windows Millennium, Windows NT 4.0, Windows 2000, XP, Netware and Linux.

1.2 Features

1.2.1 Overall Features

- Standalone PCI to Serial ATA host controller chip
- Compliant with PCI Specification, revision 2.2.
- Compliant with Programming Interface for Bus Master IDE Controller, revision 1.0.
- Driver support for Win98, WinME, NT4, Win2K, XP, Netware and Linux
- Supports up to 4Mbit external FLASH or EPROM for BIOS expansion.
- Supports an external EEPROM, FLASH or EPROM for programmable device ID, subsystem vendor ID, subsystem product ID and PCI sub-class code.
- Supports the Silicon Image specific driver for special chip functions.
- Fabricated in a 0.18µ CMOS process with a 1.8 volt core and 3.3 volt (5V tolerant) I/Os.
- Supports Plug and Play
- Supports SATA active signal for LED implementation
- Available in a 144-pin TQFP package.

1.2.2 PCI Features

- Supports 66 MHz PCI with 32-bit data.
- Supports PCI PERR and SERR reporting.
- Supports PCI bus master operations: Memory Read, Memory Read Multiple, and Memory Write.
- Supports PCI bus target operations: Configuration Read, Configuration Write, I/O Read, I/O Write, Memory Read, Memory Write, Memory Read Line (Memory Read) and Memory Read Multiple (Memory Read)
- Supports byte alignment for odd-byte PCI address access.
- Supports jumper configurable PCI class code.
- Supports programmable and EEPROM, FLASH and EPROM loadable PCI class code.
- Supports Base Address Register 5 in memory space.

1.2.3 Serial ATA Features

- Integrated Serial ATA Link and PHY logic
- Compliant with Serial ATA 1.0 specifications
- Supports two independent Serial ATA channels.
- Supports Serial ATA Generation 1 transfer rate of 1.5Gb/s.
- Supports Spread Spectrum in receiver
- Single PLL architecture, 1 PLL for both ports
- Programmable drive strengths for Backplane applications

1.2.4 Other Features

- Features independent 256-byte FIFOs (32-bit x 64 deep) per Serial ATA channel for host reads and writes.
- Features Serial ATA to PCI interrupt masking.
- Features Watch Dog Timer for fault resiliency.

1.3 Applications

- PC motherboards
- Serial ATA drive add on cards
- Serial ATA RAID controllers

1.4 References

For more details about the Serial ATA technology, the reader is referred to the following industry specifications:

- Serial ATA / High Speed Serialized AT Attachment specification, Revision 1.0
- PCI Local Bus Specification Revision 2.2
- Advanced Power Management Specification Revision 1.0
- PCI IDE Controller Specification Revision 1.0
- Programming Interface for Bus Master IDE Controller, Revision 1.0

1.5 Functional Description

SiI3112A is a PCI-to-Serial ATA controller chip that transfers data between the PCI bus and storage media (e.g. hard disk drive, etc). The SiI3112A consists of the following functional blocks:

- PCI Interface. Provides the interface to any system that has a PCI bus. Instructions and system clocks are based on this interface.
- Serial ATA Interface. Two separate channels (Primary and Secondary) to access storage media such as hard disk drive, floppy disk drive, CD-ROM.

1.6 Functional Block Diagram

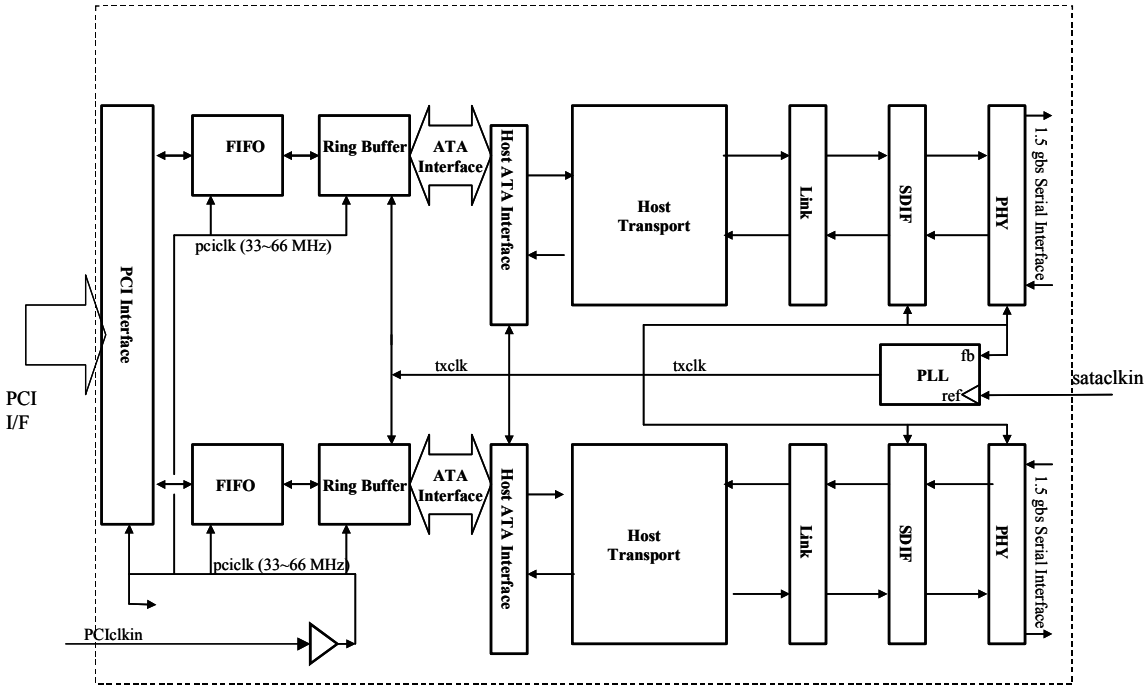


Figure 1-1 : SiI3112A Block Diagram

1.7 PCI Interface

The SiI3112A PCI interface is compliant with the PCI Local Bus Specification (Revision 2.2). The SiI3112A can act as a PCI master and a PCI slave, and contains the SiI3112A PCI configuration space and internal registers. When the SiI3112A needs to access shared memory, it becomes the bus master of the PCI bus and completes the memory cycle without external intervention. In the mode when it acts as a bridge between the PCI bus and the Serial ATA bus it will behave as a PCI slave.

1.8 PCI Initialization

Generally, when a system initializes a module containing a PCI device, the configuration manager reads the configuration space of each PCI device on the PCI bus. Hardware signals select a specific PCI device based on a bus number, a slot number, and a function number. If a device that is addressed (via signal lines) responds to the configuration cycle by claiming the bus, then that function's configuration space is read out from the device during the cycle. Since any PCI device can be a multifunction device, every supported function's configuration space needs to be read from the device. Based on the information read, the configuration manager will assign system resources to each supported function within the device. Sometimes new information needs to be written into the function's configuration space. This is accomplished with a configuration write cycle.

1.9 PCI Bus Operations

SiI3112A behaves either as a PCI master or a PCI slave device at any time and switches between these modes as required during device operation.

As a PCI slave, the SiI3112A responds to the following PCI bus operations:

- I/O Read
- I/O Write
- Configuration Read
- Configuration Write
- Memory Read
- Memory Write

  All other PCI cycles are ignored by the SiI3112A.

As a PCI master, the SiI3112A generates the following PCI bus operations:

- Memory Read Multiple
- Memory Read
- Memory Write

1.10 PCI Configuration Space

This section describes how the SiI3112A implements the required PCI configuration register space. The intent of PCI configuration space definition is to provide an appropriate set of configuration registers that satisfy the needs of current and anticipated system configuration mechanisms, without specifying those mechanisms or otherwise placing constraints on their use. These registers allow for:

- Full device relocation (including interrupt binding)
- Installation, configurations, and booting without user interventions
- System address map construction by device-independent software

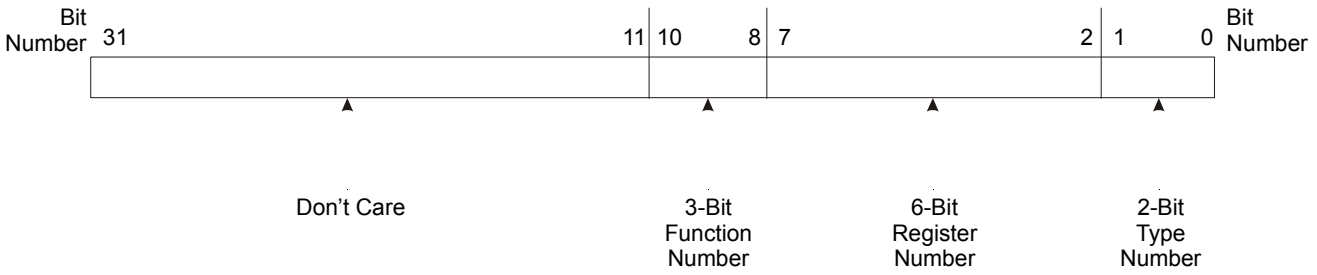


Figure 1-2: Address Lines During Configuration Cycle

SiI3112A only responds to Type 0 configuration cycles. Type 1 cycles, which pass a configuration request on to another PCI bus, are ignored.

The address phase during a SiI3112A configuration cycle indicates the function number and register number being addressed which can be decoded by observing the status of the address lines AD[31:0].

The value of the signal lines AD[7:2] during the address phase of configuration cycles selects the register of the configuration space to access. Valid values are between 0 and 15, inclusive. Accessing registers outside this range results in an all-0s value being returned on reads, and no action being taken on writes.

The Class Code register contains the Class Code, Sub-Class Code, and Register-Level Programming Interface registers.

All writable bits in the configuration space are reset to 0 by the hardware reset, PCI RESET (RST#) asserted. After reset, SiI3112A is disabled and will only respond to PCI configuration write and PCI configuration read cycles.

1.11 Deviations from the Specification

The SiI3112A product has been developed and tested to the specification listed in this document. As a result of testing and customer feedback, we may become aware of deviations to the specification that could affect the component's operation. To ensure awareness of these deviations by anyone considering the use of the SiI3112A, we have included an Errata section at the end of this specification. Please ensure that the Errata section is carefully reviewed. It is also important that you have the most current version of this specification. If there are any questions, please contact Silicon Image, Inc.

2 Electrical Characteristics

2.1 Device Electrical Characteristics

Specifications are for Commercial Temperature range, 0°C to +70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDDO	I/O Supply Voltage	4.0	V
VDDI, VDDD	Analog Supply Voltage Digital Supply Voltage	2.15	V
V_{IN}	Input Voltage	-0.3 ~ VDD+0.3	V
I_{OUT}	DC Output Current	16	mA
θ_{JA}	Thermal Resistance (Junction to Ambient)	39	°C/W
T_{STG}	Storage Temperature	-65 ~ 150	°C

Table 2-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDDI , VDDD	Supply Voltage (Digital, Analog)			1.71	1.8	1.89	V
VDDO	Supply Voltage(I/O)	-	-	3.0	3.3	3.6	V
$IDD_{1.8V}$	1.8V Supply Current				236[1]	285[2]	mA
$IDD_{3.3V}$	3.3V Supply Current	C_{LOAD}= 20pF			12[1]	30[2]	mA
V_{IH}	Input High Voltage	-	3.3V PCI	0.5xVDD	-	-	V
		-	Non-PCI	2.0	-	-	
V_{IL}	Input Low Voltage	-	3.3V PCI	-	-	0.3xVDD	V
		-	Non-PCI	-	-	0.8	
V+	Input High Voltage	-	Schmitt	-	1.8	2.3	V
V-	Input Low Voltage	-	Schmitt	0.5	0.9	-	V
V_H	Hysteresis Voltage	-	Schmitt	0.4	-	-	V
I_{IH}	Input High Current	V_{IN} = VDD	-	-10	-	10	µA
I_{IL}	Input Low Current	V_{IN} = VSS	-	-10	-	10	µA
V_{OH}	Output High Voltage	-	-	2.4	-	-	V
V_{OL}	Output Low Voltage	-	-	-	-	0.4	V
I_{OZ}	3-State Leakage Current	-	-	-10	-	10	µA

Notes: [1] Using the random data pattern (read/write operation) at 1.8V or 3.3V power supply, PCI interface = 33MHz
[2] Using the maximum toggling data pattern (read/write operation) at 1.89V or 3.6V power supply , PCI interface = 66MHz

Table 2-2 DC Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{DOUT_00}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 00	400	500	600	mV
V_{DOUT_01}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 01	500	600	700	mV
V_{DOUT_10}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 10	550	700	800	mV
V_{DOUT_11}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 11	650	800	900	mV
V_{DIN}	RX+/RX- differential peak-to-peak input sensitivity		325			mV
V_{DIH}	RX+/RX- differential Input common-mode voltage		200	300	450	mV
V_{DOH}	TX+/TX-differential Output common-mode voltage		200	300	450	mV
Z_{DIN}	Differential input impedance	REXT = 1k 1% for 25MHz SerDes Ref Clk REXT = 4.99k 1% for 100MHz SerDes Ref Clk	85	100	115	ohms
Z_{DOUT}	Differential output impedance	REXT = 1k 1% for 25MHz SerDes Ref Clk REXT = 4.99k 1% for 100MHz SerDes Ref Clk	85	100	115	ohms

Table 2-3 SATA Interface DC Specifications

2.2 SATA Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$T_{TX\_RISE\_FALL}$	Rise and Fall time at transmitter	20%-80%	133		274	ps
T_{TX_SKEW}	Tx differential skew				20	ps
$T_{TX\_DC\_FREQ}$	Tx DC clock frequency skew		-350		+350	ppm
$T_{TX\_AC\_FREQ}$	Tx AC clock frequency skew	SerDes Ref Clk = SSC AC modulation, subject to the "Downspread SSC" triangular modulation (30-33KHz) profile per 6.6.4.5 in SATA 1.0 specification	-5000		+0	ppm

Table 2-4 SATA Interface Timing Specifications

2.3 SATA Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
RJ_{5UI}	5UI later Random Jitter	Measured at Tx output pins 1sigma deviation		3.6		ps rms
RJ_{250UI}	250UI later Random Jitter	Measured at Tx output pins 1sigma deviation		4.7		ps rms
DJ_{5UI}	5UI later Deterministic Jitter	Measured at Tx output pins peak to peak phase variation Random data pattern		20		ps
DJ_{250UI}	250UI later Deterministic Jitter	Measured at Tx output pins peak to peak phase variation Random data pattern		25		ps

Table 2-5 SATA Interface Transmitter Output Jitter Characteristics

2.4 CLKI SerDes Reference Clock Input Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T_{CLKI_FREQ}	Norminal Frequency	REXT = 1k 1% REXT = 4.99k 1%		25 100		MHz
T_{CLKI_J}	CLKI frequency tolerance		-100		+100	ppm
$T_{CLKI\_RISE\_FALL}$	Rise and Fall time at CLKI	25MHz reference clock, 20%-80% 100MHz reference clock, 20%-80%			4 2	ns
$T_{CLKI\_RC\_DUTY}$	CLKI duty cycle	20%-80%	40		60	%

Table 2-6 CLKI SerDes Reference Clock Input Requirements

2.5 PCI 33 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	2.0	11.0	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	2.0	11.0	ns
T_{ON}	Float to Active Delay	2.0	-	ns
T_{OFF}	Active to Float Delay	-	28.0	ns
T_{SU}	Input Setup Time – Bussed Signals	7.0	-	ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	10.0	-	ns
T_{H}	Input Hold Time	0.0	-	ns

Table 2-7 PCI 33 MHz Timing Specifications

2.6 PCI 66 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	2.0	6.0	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	2.0	6.0	ns
T_{ON}	Float to Active Delay	2.0		ns
T_{OFF}	Active to Float Delay		14.0	ns
T_{SU}	Input Setup Time – Bussed Signals	3.0		ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	5.0		ns
T_{H}	Input Hold Time	0.0		ns

Table 2-8 PCI 66 MHz Timing Specifications

3 Pin Definition

3.1 Sil3112A Pin Listing

This section describes the pin-out of the SiI3112A PCI-to-Serial ATA host controller. Table 3-1 gives the pin numbers, pin names, pin types, drive types where applicable, internal resistors where applicable, and descriptions.

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
1	VSS	GND	-	-	Ground
2	SCAN_EN	I	-	PD – 60k	Internal Scan Enable
3	VDDO	PWR			3.3Power
4	NC				
5	GNDD	GND	-	-	Digital Ground
6	VDDD	PWR	-	-	1.8V SerDes Power
7	GNDD	GND	-	-	Digital Ground
8	GNDA	GND	-	-	Analog Ground
9	RxP2	I			Channel 2 Differential Receive +ve
10	RxN2	I			Channel 2 Differential Receive -ve
11	GNDA	GND	-	-	Analog Ground
12	VDDD	PWR	-	-	1.8V SerDes Power
13	GNDD	GND	-	-	Digital Ground
14	GNDA	GND	-	-	Analog Ground
15	TxN2	O			Channel 2 Differential Transmit -ve
16	TxP2	O			Channel 2 Differential Transmit +ve
17	GNDA	GND	-	-	Analog Ground
18	GNDD	GND	-	-	Digital Ground
19	VDDD	PWR	-	-	1.8V SerDes Power
20	GNDD	GND	-	-	Digital Ground
21	GNDA	GND	-	-	Analog Ground
22	TxP1	O			Channel 1 Differential Transmit +ve
23	TxN1	O			Channel 1 Differential Transmit -ve
24	GNDA	GND	-	-	Analog Ground
25	VDDD	PWR	-	-	1.8V SerDes Power
26	GNDD	GND	-	-	Digital Ground
27	GNDA	GND	-	-	Analog Ground
28	RxN1	I			Channel 1 Differential Receive -ve
29	RxP1	I			Channel 1 Differential Receive +ve
30	GNDA	GND	-	-	Analog Ground
31	GNDD	GND	-	-	Digital Ground
32	VDDD	PWR	-	-	1.8V SerDes Power

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
33	REXT	I			External Reference Resistor Input
34	GNDA	GND	-	-	Analog Ground
35	XTALI/CLKI	I			Crystal Oscillator Input or external clock input
36	XTALO	O			Crystal Oscillator Output
37	VDDO	PWR			3.3V supply for Crystal Oscillator
38	VSS	GND	-	-	Ground
39	VDDI	PWR	-	-	1.8V Volt Internal Core Power
40	EEPROM_SDAT	I/O		PU – 70k	EEPROM Serial Data
41	EEPROM_SCLK	I/O		PU – 70k	EEPROM Serial Clock
42	FL_ADDR[00] / IDE_CFG	I/O		PU – 70k	Flash Memory Address 0 / IDE-RAID Configuration
43	FL_ADDR[01] / BA5_EN	I/O		PU – 70k	Flash Memory Address 1 / Base Address Register 5 Enable
44	FL_ADDR[02]	O			Flash Memory Address 2
45	FL_WR_N	O		-	Flash Memory Write Strobe
46	VDDO	PWR	-	-	3.3 Volt Power
47	VSS	GND	-	-	Ground
48	FL_RD_N	O		-	Flash Memory Read Strobe
49	FL_ADDR[03]	O			Flash Memory Address 3
50	FL_ADDR[04]	O			Flash Memory Address 4
51	FL_ADDR[05]	O			Flash Memory Address 5
52	FL_ADDR[06]	O			Flash Memory Address 6
53	FL_ADDR[07]	O			Flash Memory Address 7
54	FL_ADDR[08]	O			Flash Memory Address 8
55	FL_ADDR[09]	O			Flash Memory Address 9
56	VDDI	PWR	-	-	1.8V Internal core Power
57	VSS	GND	-	-	Ground
58	FL_ADDR[10]	O			Flash Memory Address 10
59	FL_ADDR[11]	O			Flash Memory Address 11
60	FL_ADDR[12]	O			Flash Memory Address 12
61	FL_ADDR[13]	O			Flash Memory Address 13
62	FL_ADDR[14]	O			Flash Memory Address 14
63	FL_ADDR[15]	O		PU – 70k	Flash Memory Address 15
64	FL_ADDR[16]	O		PU – 70k	Flash Memory Address 16
65	FL_ADDR[17]	O		PU – 70k	Flash Memory Address 17
66	FL_ADDR[18]	O		PU – 70k	Flash Memory Address 18
67	TEST_MODE	I	-	PD – 60k	Test Mode Enable
68	FL_DATA[00]	I/O		PU – 70k	Flash Memory Data 0
69	FL_DATA[01]	I/O		PU – 70k	Flash Memory Data 1
70	FL_DATA[02]	I/O		PU – 70k	Flash Memory Data 2

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
71	FL_DATA[03]	I/O		PU – 70k	Flash Memory Data 3
72	VDDO	PWR	-	-	3.3 Volt Power
73	VSS	GND	-	-	Ground
74	FL_DATA[04]	I/O		PU – 70k	Flash Memory Data 4
75	FL_DATA[05]	I/O		PU – 70k	Flash Memory Data 5
76	FL_DATA[06]	I/O		PU – 70k	Flash Memory Data 6
77	FL_DATA[07]	I/O		PU – 70k	Flash Memory Data 7
78	VSS	GND	-	-	Ground
79	VDDI	PWR	-	-	1.8V Internal core Power
80	VSS	GND	-	-	Ground
81	VDDI	PWR	-	-	1.8V Internal core Power
82	PCI_INTA_N	OD	PCI	-	PCI Interrupt
83	PCI_RST_N	I-Schmitt	-	-	PCI Reset
84	PCI_CLK	I	-	-	PCI Clock
85	PCI_GNT_N	I	-	-	PCI Bus Grant
86	PCI_REQ_N	T	PCI	-	PCI Bus Request
87	VDDO	PWR	-	-	3.3 Volt Power
88	VSS	GND	-	-	Ground
89	PCI_AD31	I/O	PCI	-	PCI Address/Data
90	PCI_AD30	I/O	PCI	-	PCI Address/Data
91	PCI_AD29	I/O	PCI	-	PCI Address/Data
92	PCI_AD28	I/O	PCI	-	PCI Address/Data
93	PCI_AD27	I/O	PCI	-	PCI Address/Data
94	PCI_AD26	I/O	PCI	-	PCI Address/Data
95	PCI_AD25	I/O	PCI	-	PCI Address/Data
96	PCI_AD24	I/O	PCI	-	PCI Address/Data
97	PCI_CBE3	I/O	PCI	-	PCI Command/Byte Enable
98	VDDI	PWR	-	-	1.8 Volt Core Power
99	VSS	GND	-	-	Ground
100	PCI_IDSEL	I	-	-	PCI ID Select
101	PCI_AD23	I/O	PCI	-	PCI Address/Data
102	PCI_AD22	I/O	PCI	-	PCI Address/Data
103	PCI_AD21	I/O	PCI	-	PCI Address/Data
104	PCI_AD20	I/O	PCI	-	PCI Address/Data
105	PCI_AD19	I/O	PCI	-	PCI Address/Data
106	PCI_AD18	I/O	PCI	-	PCI Address/Data
107	PCI_AD17	I/O	PCI	-	PCI Address/Data
108	VDDO	PWR	-	-	3.3 Volt Power
109	VSS	GND	-	-	Ground
110	PCI_AD16	I/O	PCI	-	PCI Address/Data

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
111	PCI_CBE2	I/O	PCI	-	PCI Command/Byte Enable
112	PCI_FRAME_N	I/O	PCI	-	PCI Frame
113	PCI_IRDY_N	I/O	PCI	-	PCI Initiator Ready
114	PCI_PERR_N	I/O	PCI	-	PCI Parity Error
115	PCI_STOP_N	I/O	PCI	-	PCI Stop
116	PCI_DEVSEL_N	I/O	PCI	-	PCI Device Select
117	PCI_TRDY_N	I/O	PCI	-	PCI Target Ready
118	VDDI	PWR	-	-	1.8 Volt Core Power
119	VSS	GND	-	-	Ground
120	PCI_SERR_N	OD	PCI	-	PCI System Error
121	PCI_PAR	I/O	PCI	-	PCI Parity
122	PCI_CBE1	I/O	PCI	-	PCI Command/Byte Enable
123	PCI_AD15	I/O	PCI	-	PCI Address/Data
124	PCI_AD14	I/O	PCI	-	PCI Address/Data
125	PCI_AD13	I/O	PCI	-	PCI Address/Data
126	PCI_AD12	I/O	PCI	-	PCI Address/Data
127	PCI_AD11	I/O	PCI	-	PCI Address/Data
128	VDDO	PWR	-	-	3.3 Volt Power
129	VSS	GND	-	-	Ground
130	PCI_AD10	I/O	PCI	-	PCI Address/Data
131	PCI_M66EN	I	-	-	PCI 66 MHz Enable
132	PCI_AD09	I/O	PCI	-	PCI Address/Data
133	PCI_AD08	I/O	PCI	-	PCI Address/Data
134	PCI_CBE0	I/O	PCI	-	PCI Command/Byte Enable
135	PCI_AD07	I/O	PCI	-	PCI Address/Data
136	PCI_AD06	I/O	PCI	-	PCI Address/Data
137	PCI_AD05	I/O	PCI	-	PCI Address/Data
138	PCI_AD04	I/O	PCI	-	PCI Address/Data
139	PCI_AD03	I/O	PCI	-	PCI Address/Data
140	PCI_AD02	I/O	PCI	-	PCI Address/Data
141	PCI_AD01	I/O	PCI	-	PCI Address/Data
142	PCI_AD00	I/O	PCI	-	PCI Address/Data
143	MEM_CS_N	O		-	Memory Chip Select
144	VDDO	PWR	-	-	3.3 Volt Power

Table 3-1 Sil3112A Pin Listing

Pin Type	Pin Description
I	Input Pin with LVTTL Thresholds
I-Schmitt	Input Pin with Schmitt Trigger
O	Output Pin
T	Tri-state Output Pin
I/O	Bi-directional Pin
OD	Open Drain Output Pin

Table 3-2 Pin Types

PCI pins are 5V tolerant.

3.2 Sil3112A Pin Diagram

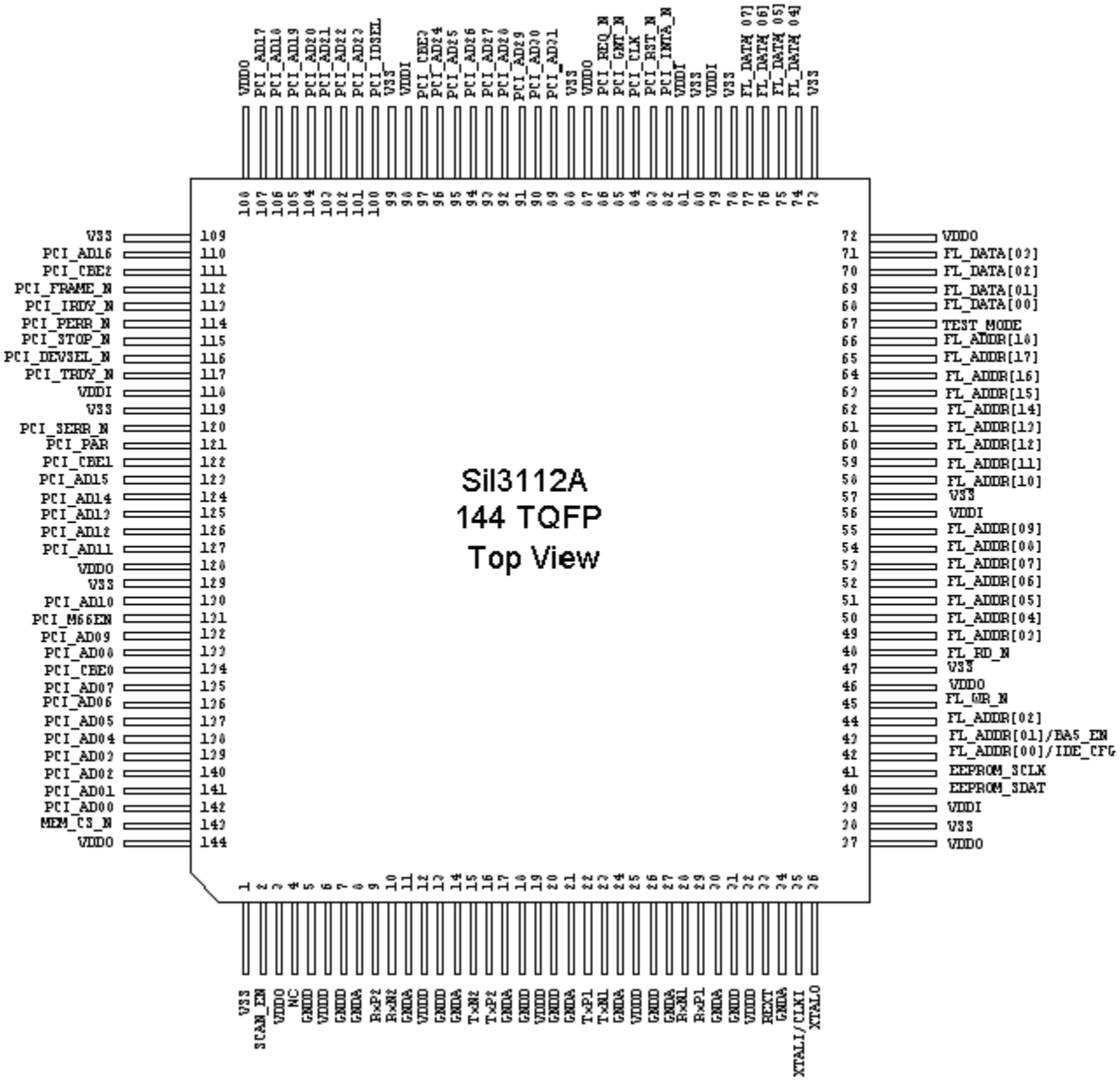


Figure 3-1. Sil3112A Pin Diagram

3.3 Sil3112A Pin Descriptions

3.3.1 PCI 66MHz 32-bit

PCI Address and Data

Pin Names: PCI_AD[31..0]
Pin Numbers: 89~96, 101~107, 110, 123~127,132, 133, 135~142
Address and Data buses are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the first clock cycle in which PCI_FRAME_N signal is asserted. During the address phase, PCI_AD[31:0] contain a physical address (32 bits). For I/O, this can be a byte address. For configuration and memory it is a DWORD address. During data phases, PCI_AD[7:0] contain the least significant byte (LSB) and PCI_AD[31:24] contain the most significant byte (MSB). Write data is stable and valid when PCI_IRDY_N is asserted; read data is stable and valid when PCI_TRDY_N is asserted. Data is transferred during those clocks where both PCI_IRDY_N and PCI_TRDY_N are asserted.

PCI Command and Byte Enables

Pin Names: PCI_CBE[3..0]
Pin Numbers: 97, 111, 122, 134
Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, PCI_CBE[3:0]_N define the bus command. During the data phase, PCI_CBE[3:0]_N are used as Byte Enables. Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.

PCI ID Select

Pin Name: PCI_IDSEL
Pin Number: 100
This signal is used as a chip select during configuration read and write transactions.

PCI Frame Cycle

Pin Name: PCI_FRAME_N
Pin Number: 112
Cycle Frame is driven by the current master to indicate the beginning and duration of an access. PCI_FRAME_N is asserted to indicate that a bus transaction is beginning. While PCI_FRAME_N is asserted, data transfers continue. When PCI_FRAME_N is de-asserted, the transaction is in the final data phase or has completed.

PCI Initiator Ready

Pin Name: PCI_IRDY_N
Pin Number: 113
Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with PCI_TRDY_N. A data phase is completed on any clock when both PCI_IRDY_N and PCI_TRDY_N are sampled as asserted. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together.

PCI Target Ready

Pin Name: PCI_TRDY_N
Pin Number: 117
Target Ready indicates the target agent's ability to complete the current data phase of the transaction. PCI_TRDY_N is used with PCI_IRDY_N. A data phase is completed on any clock when both PCI_TRDY_N and PCI_IRDY_N are sampled asserted. During a read, PCI_TRDY_N indicates that valid data is present on PCI_AD[31:0]. During a write, it indicates the target is prepared to accept data.

PCI Device Select

Pin Name: PCI_DEVSEL_N
Pin Number: 116
Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, PCI_DEVSEL_N indicates to a master whether any device on the bus has been selected.

PCI Stop

Pin Name: PCI_STOP_N
Pin Number: 115
PCI_STOP_N indicates the current target is requesting that the master stop the current transaction.

PCI Parity Error

Pin Name: PCI_PERR_N
Pin Number: 114
PCI_PERR_N indicates a data parity error between the current master and target on PCI. On a write transaction, the target always signals data parity errors back to the master on PCI_PERR_N. On a read transaction, the master asserts PCI_PERR_N to indicate to the system that an error was detected.

PCI System Error

Pin Name: PCI_SERR_N
Pin Number: 120
System Error is for reporting address parity errors, data parity errors on Special Cycle Command, or any other system error where the result will be catastrophic. The PCI_SERR_N is a pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of PCI_SERR_N is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of PCI_SERR_N to the de-asserted state is accomplished by a weak pull-up. Note that if an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

PCI Parity

Pin Name: PCI_PAR
Pin Number: 121
PCI_PAR is even parity across PCI_AD[31:0] and PCI_CBE[3:0]_N. Parity generation is required by all PCI agents. PCI_PAR is stable and valid one clock after the address phase. For data phases PCI_PAR is stable and valid one clock after either PCI_IRDY_N is asserted on a write transaction or PCI_TRDY_N is asserted on a read transaction. Once PCI_PAR is valid, it remains valid until one clock after the completion of the current data phase. (PCI_PAR has the same timing as PCI_AD[31:0] but delayed by one clock.)

PCI Request

Pin Name: PCI_REQ_N
Pin Number: 86
This signal indicates to the arbiter that this agent desires use of the PCI bus.

PCI Grant

Pin Name: PCI_GNT_N
Pin Number: 85
This signal indicates to the agent that access to the PCI bus has been granted. In response to a PCI request, this is a point-to-point signal. Every master has its own PCI_GNT_N, which must be ignored while PCI_RST_N is asserted.

PCI Interrupt A

Pin Name: PCI_INTA_N
Pin Number: 82
Interrupt A is used to request an interrupt on the PCI bus. PCI_INTA_N is open collector and is an open drain output.

PCI Clock Signal

Pin Names: PCI_CLK
Pin Number: 84
Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals (except PCI_RST_N, and PCI_INTA_N) are sampled on the rising edge of PCI_CLK. All other timing parameters are defined with respect to this edge.

PCI Reset

Pin Name: PCI_RST_N
Pin Number: 83
PCI_RST_N is an active low input that is used to set the internal registers to their initial state. PCI_RST_N is typically the system power-on reset signal as distributed on the PCI bus.

PCI M66EN

Pin Name: PCI_M66EN
Pin Number: 131
This pin configures the PCI bus operating frequency. When low, the PCI bus operates from 0 to 33 MHz. When high, the PCI bus operates from 33MHz to 66MHz.

3.3.2 Miscellaneous I/O

Ground

Pin Name: VSS
Pin Number: 1, 38, 47, 57, 73, 78, 80, 88, 99, 109,119, 129
Ground reference point to power supply.

TEST

Pin Name: TEST_MODE
Pin Number: 67
This pin is used, in conjunction with other pins, to enable various test functions within the device.

Power Supply

Pin Name(s): VDDO
Pin Number(s): 3, 37, 46, 72, 87, 108, 128, 144
Power Supply Input (3.3 +/- 0.3 Volt)

Pin Name(s): VDDI
Pin Number(s): 39, 56, 79, 81, 98, 118
Power Supply Input for internal core (1.8 +/- 0.09 Volt)

Internal Scan Test

Pin Name: SCAN_EN
Pin Number: 2
This pin, when active (high), will place all scan flip-flops into scan mode for chip testing. This pin must be left open or tied to ground for normal operation.

Flash Signals

Pin Name: FL_ADDR[00] / IDE_CFG
Pin Number: 42
When PCI_RST_N is deasserted, this pin is an output and represents flash memory address bit 0 During reset, it is sampled to configure Mass Storage class or RAID mode in the PCI Class Code register. A high on this pin sets Mass Storage class, a low sets RAID mode. The configuration state is latched internally when PCI_RST_N is deasserted. This pad is internally pulled high to enable Mass Storage class if left unconnected.

Pin Name: FL_ADDR[01] / BA5_EN
Pin Number: 43
When PCI_RST_N is deasserted, this pin is an output and represents flash memory address bit 1 During reset, it is sampled to configure Base address register 5. A high on this pin enables base address register 5, a low disables base address register 5. The configuration state is latched internally when PCI_RST_N is deasserted. This pin is internally pulled high to enable Base address register 5 when left unconnected.

Pin Name: FL_ADDR[02-18]
Pin Numbers: 44, 49~55, 58~66
Flash Memory address bits; 19 total for 512K address space. Flash address pins 15 to 18 are used to select internal test modes in conjunction with the TEST_MODE pin; they have internal pull-downs and must be unconnected or pulled down.

Pin Name: FL_DATA[00-07]
Pin Numbers: 68~71, 74~77
8-bit Flash memory data bus.

Pin Name: FL_RD_N
Pin Number: 48
Flash read enable signal, active low

Pin Name: FL_WR_N
Pin Number: 45
Flash write enable signal, active low

Memory Chip Select

Pin Name: MEM_CS_N
Pin Number: 143
This pin is used to select and enable the external memory. It is active low.

Serial Interface Signals

Pin Name: EEPROM_SDAT
Pin Number: 40
Serial Interface data line

Pin Name: EEPROM_SCLK
Pin Number: 41
Serial Interface clock

3.3.3 Serial ATA Signals

Power Supply & Ground

Pin Name: VDDD
Pin Numbers: 6, 12, 19, 25, and 32
SerDes 1.8 V Power supply Pins

Pin Name: GNDD
Pin Numbers: 5, 7, 13, 18, 20, 26, and 31
SerDes Digital Ground

Pin Name: GNDA
Pin Numbers: 8, 11, 14, 17, 21, 24, 27, 30, and 34
SerDes Analog Ground

High Speed Serial Signals

Pin Name: RxN1
Pin Number: 28
Channel 1 high-speed differential receive negative side.

Pin Name: RxP1
Pin Number: 29
Channel 1 high-speed differential receive positive side. Loading an internal register through the flash or EEPROM during the initialization sequence could reverse RxP1 and RxN1 pinouts.

Pin Name: TxN1
Pin Number: 23
Channel 1 high speed differential transmit negative side

Pin Name: TxP1
Pin Number: 22
Channel 1 high speed differential transmit positive side

Pin Name: RxN2
Pin Number: 10
Channel 2 high-speed differential receive negative side.

Pin Name: RxP2
Pin Number: 9
Channel 2 high-speed differential receive positive side. Loading an internal register through the flash or EEPROM during the initialization sequence could reverse RxP2 and RxN2 pinouts.

Pin Name: TxN2
Pin Number: 15
Channel 2 high speed differential transmit negative side

Pin Name: TxP2
Pin Number: 16
Channel 2 high speed differential transmit positive side

Other SerDes Signals

Pin Name: XTALO
Pin Number: 36
Crystal oscillator pin for SerDes reference clock. A 25MHz crystal must be used.

Pin Name: XTALI/CLKI
Pin Number: 35
Crystal oscillator pin for SerDes reference clock. When external clock source is selected, the external clock (either 25MHz or 100 MHz) will come in through this pin. The clock precision requirement is ±100ppm.

Pin Name: REXT
Pin Number: 33
External reference resistor pin for termination calibration. This pin provides the addition function of selecting frequency of the clock source . For 25MHz crystal/external clock, a 1K, 1% resistor is connected to ground. To use 100MHz external clock, a 4.99K, 1% resistor is connected to ground.

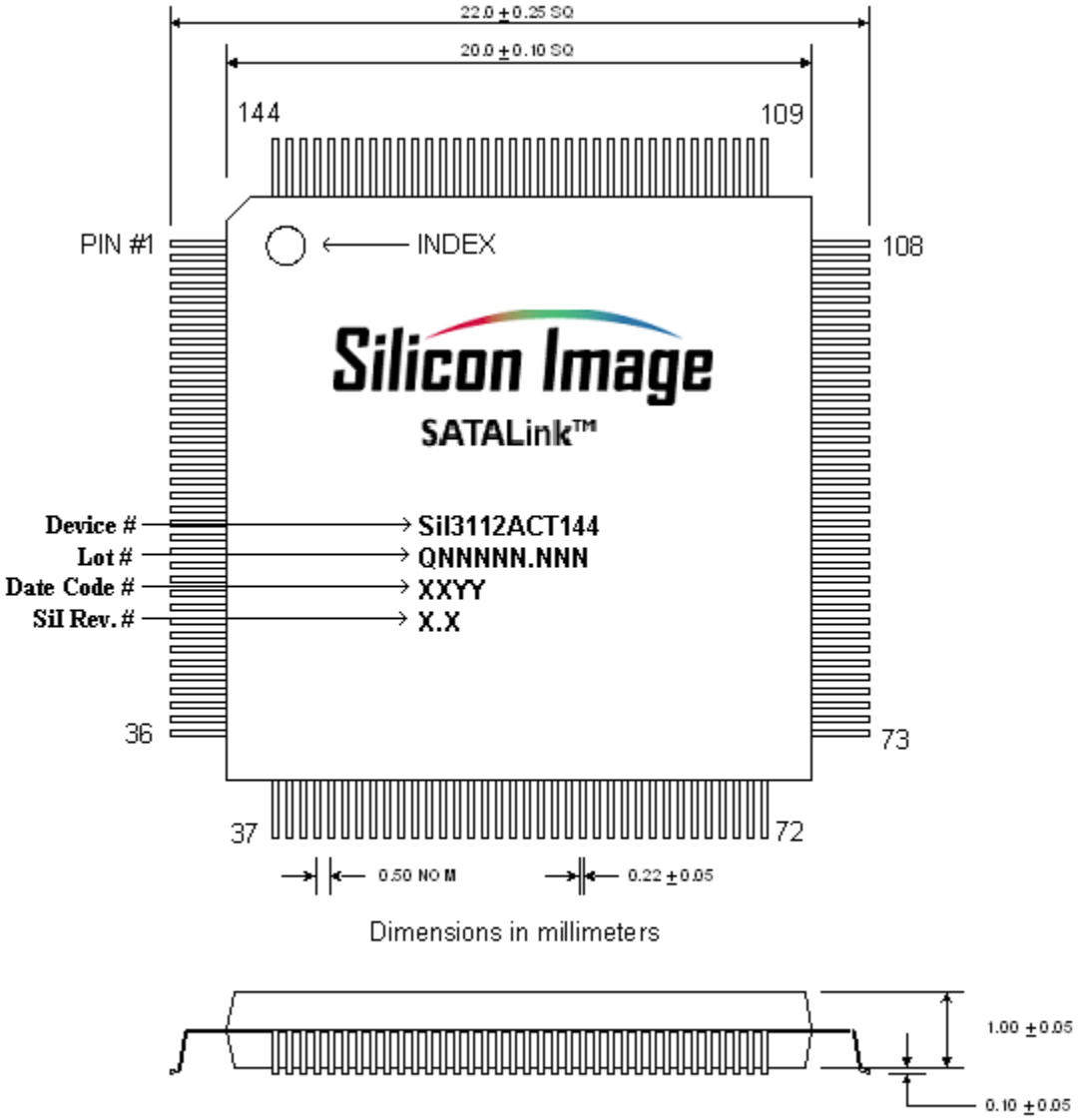


Figure 3-2: Package Drawing – 144 TQFP

4 Block Diagram

The SiI3112A contains the major logic modules shown below.

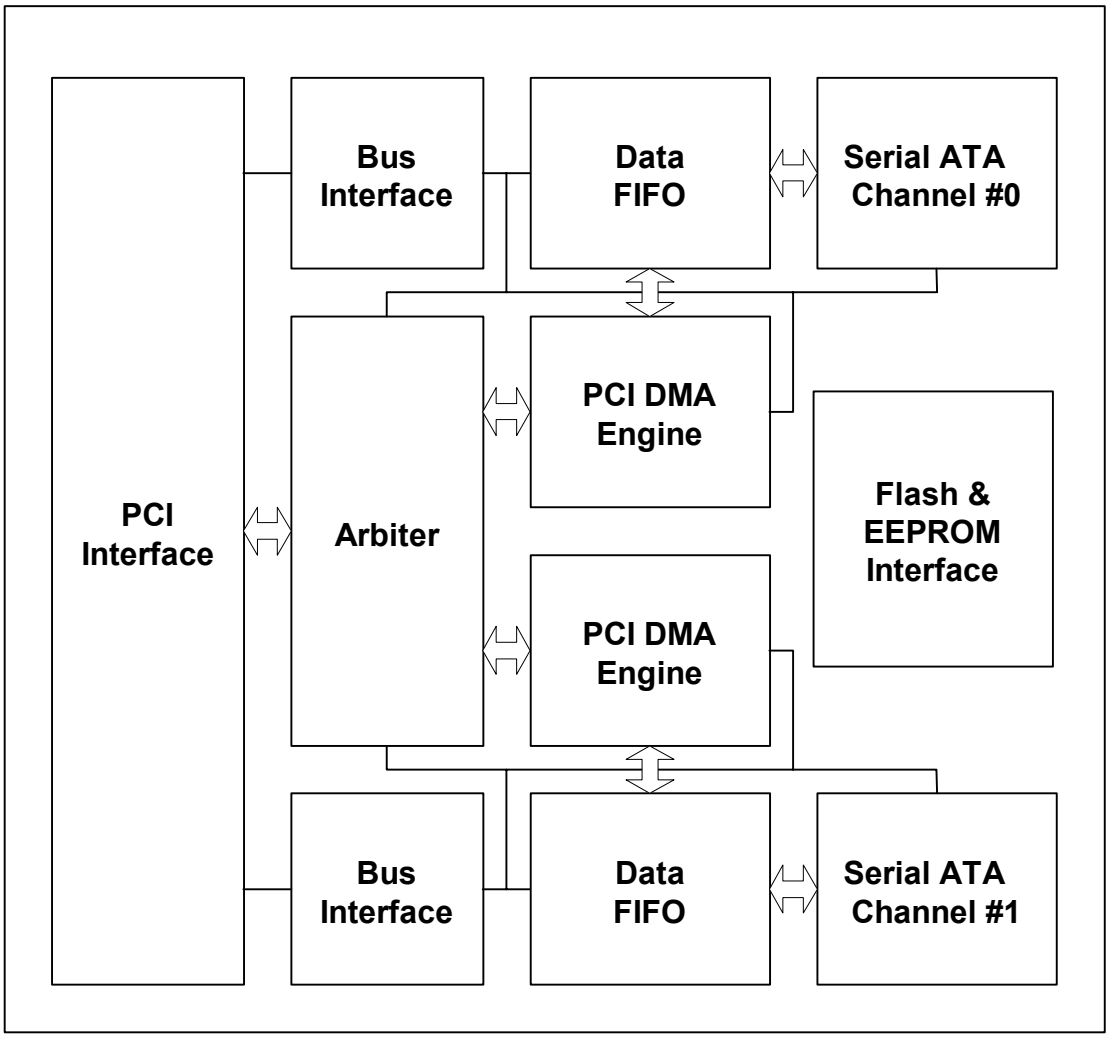


Figure 4-1: SiI3112A Block Diagram

5 Auto-Initialization

The SiI3112A supports an external FLASH and/or EEPROM device for BIOS extensions and user-defined PCI configuration header data.

5.1 Auto-Initialization from FLASH

The SiI3112A initiates the FLASH detection and configuration space loading sequence upon the release of PCI_RST_N. It begins by reading the highest two addresses ($7FFFF_H$ and $7FFFE_H$), checking for the correct data signature pattern – AA_H and 55_H, respectively. If the data signature pattern is correct, the SiI3112A continues to sequence the address downward, reading a total of sixteen bytes. If the Data Signature is correct (55_H at $7FFFC_H$), the last twelve bytes are loaded into the PCI Configuration Space registers.

Note: If both Flash and EEPROM are installed, the PCI Configuration Space registers will be loaded with EEPROM's data. While the sequence is active, the SiI3112A responds to all PCI bus accesses with a Target Retry.

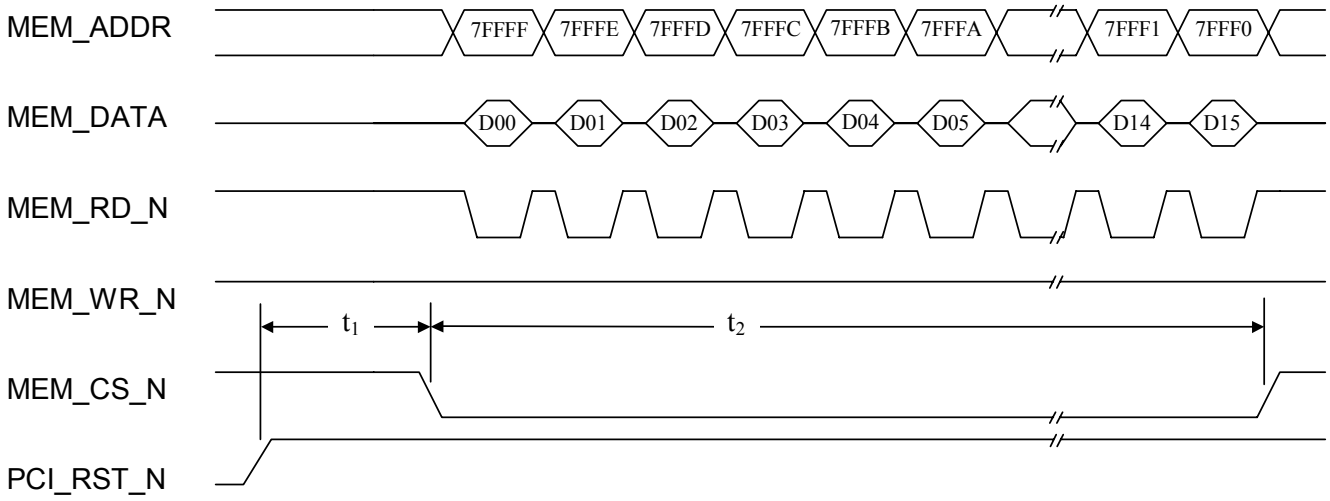


Figure 5-1 Auto-Initialization from Flash Timing

Parameter	Value	Description
t_1	660 ns	PCI reset to Flash Auto-Initialization cycle begin
t_2	9600 ns	Flash Auto-Initialization cycle time

Table 5-1 Auto-Initialization from Flash Timing

Address	Data Byte	Description
$7FFFF_H$	D00	Data Signature = AA_H
$7FFFE_H$	D01	Data Signature = 55_H
$7FFFD_H$	D02	AA = 120 ns FLASH device / Else, 240 ns FLASH device
$7FFFC_H$	D03	Data Signature = 55_H
$7FFFB_H$	D04	PCI Device ID [23:16]
$7FFFA_H$	D05	PCI Device ID [31:24]
$7FFF9_H$	D06	PCI Class Code [15:08]
$7FFF8_H$	D07	PCI Class Code [23:16]
$7FFF7_H$	D08	PCI Sub-System Vendor ID [07:00]
$7FFF6_H$	D09	PCI Sub-System Vendor ID [15:08]
$7FFF5_H$	D10	PCI Sub-System ID [23:16]
$7FFF4_H$	D11	PCI Sub-System ID [31:24]
$7FFF3_H$	D12	SerialATA PHY Config [07:00] (default: 0xF1)
$7FFF2_H$	D13	SerialATA PHY Config [15:08] (default: 0x80)
$7FFF1_H$	D14	SerialATA PHY Config [23:16] (default: 0x00)
$7FFF0_H$	D15	SerialATA PHY Config [31:24] (default: 0x00)

Table 5-2 Flash Data Description

5.2 Auto-Initialization from EEPROM

The SiI3112A initiates the EEPROM detection and configuration space loading sequence after the FLASH read sequence. The SiI3112A supports up to 256 byte EEPROM with a 2-wire serial interface. The sequence of operations consists of the following.

1) START condition defined as a high-to-low transition on SDAT while SCLK is high.
2) Control byte = 1010 (Control Code) + 000 (Chip Select) + 0 (Write Address)
3) Acknowledge
4) Starting address field = 00000000.
5) Acknowledge
6) Sequential data bytes separated by Acknowledges.
7) STOP condition.

While the sequence is active, the SiI3112A responds to all PCI bus accesses with a Target Retry.

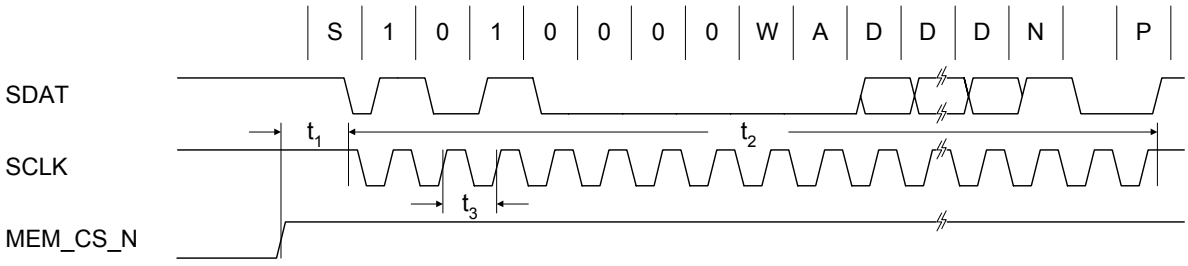


Figure 5-2: Auto-Initialization from EEPROM Timing

Parameter	Value	Description
t_1	26.00 µs	End of Auto-Initialization from FLASH to start of Auto-Initialization from EEPROM
t_2	2.66 ms	Auto-Initialization from EEPROM cycle time
t_3	19.26 µs	EEPROM serial clock period

Table 5-3 Auto-Initialization from EEPROM Timing

Parameter	Description
S	START condition
W	R/W 0 = Write Command, 1 = Read Command
A	Acknowledge
D	Serial data
N	No-Acknowledge
P	STOP condition

Table 5-4 Auto-Initialization from EEPROM Timing Symbols

Address	Data Byte	Description
00_H	D00	Memory Present Pattern = AA_H
01_H	D01	Memory Present Pattern = 55_H
02_H	D02	Data Signature = AA_H
03_H	D03	Data Signature = 55_H
04_H	D04	PCI Device ID [23:16]
05_H	D05	PCI Device ID [31:24]
06_H	D06	PCI Class Code [15:08]
07_H	D07	PCI Class Code [23:16]
08_H	D08	PCI Sub-System Vendor ID [07:00]
09_H	D09	PCI Sub-System Vendor ID [15:08]
$0A_H$	D10	PCI Sub-System ID [23:16]
$0B_H$	D11	PCI Sub-System ID [31:24]
$0C_H$	D12	SerialATA PHY Config [07:00] (default: 0xF1)
$0D_H$	D13	SerialATA PHY Config [15:08] (default: 0x80)
$0E_H$	D14	SerialATA PHY Config [23:16] (default: 0x00)
$0F_H$	D15	SerialATA PHY Config [31:24] (default: 0x00)

Table 5-5 EEPROM Data Description

6 Register Definitions

This section describes the registers within the SiI3112A.

6.1 PCI Configuration Space

The PCI Configuration Space registers define the operation of the SiI3112A on the PCI bus. These registers are accessible only when the SiI3112A detects a Configuration Read or Write operation, with its IDSEL asserted, on the 32-bit PCI bus.

Table 6-1 outlines the PCI Configuration space for the SiI3112A.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Device ID		Vendor ID		R/W
04_H	PCI Status		PCI Command		R/W
08_H	PCI Class Code			Revision ID	R/W
$0C_H$	BIST	Header Type	Latency Timer	Cache Line Size	R/W
10_H	Base Address Register 0				R/W
14_H	Base Address Register 1				R/W
18_H	Base Address Register 2				R/W
$1C_H$	Base Address Register 3				R/W
20_H	Base Address Register 4				R/W
24_H	Base Address Register 5				R/W
28_H	Reserved				-
$2C_H$	Subsystem ID		Subsystem Vendor ID		R/W
30_H	Expansion ROM Base Address				R/W
34_H	Reserved			Capabilities Ptr	R
38_H	Reserved				R/W
$3C_H$	Max Latency	Min Grant	Interrupt Pin	Interrupt Line	R/W
40_H	Reserved			Configuration	R/W
44_H	Software Data Register				R/W
48_H	Reserved				-
$4C_H$	Reserved				-
50_H	Reserved				-

Table 6-1 SiI3112A PCI Configuration Space

Address Offset	Register Name				Access Type
	31 16		15 00		
54_H	Reserved				-
58_H	Reserved				-
$5C_H$	Reserved				-
60_H	Power Management Capabilities		Next Item Pointer	Capability ID	R/W
64_H	Data	Reserved	Functions Control and Status		R/W
68_H	Reserved				-
$6C_H$	Reserved				-
70_H	Reserved	PCI Bus Master Status – IDE0	Reserved	PCI Bus Master Command – IDE0	R/W
74_H	PRD Table Address – IDE0				R/W
78_H	Reserved	PCI Bus Master Status – IDE1	Reserved	PCI Bus Master Command – IDE1	R/W
$7C_H$	PRD Table Address – IDE1				R/W
80_H	Reserved			IDE0 Data Transfer Mode	R/W
84_H	Reserved			IDE1 Data Transfer Mode	R/W
88_H	System Configuration Status		System Command		R/W
$8C_H$	System Software Data				R/W
90_H	FLASH Memory Address – Command + Status				R/W
94_H	Reserved			Flash Memory Data	R/W
98_H	EEPROM Memory Address – Command + Status				R/W
$9C_H$	Reserved			EEPROM Memory Data	R/W
$A0_H$	Reserved		IDE0 Config + Status	IDE0 Cmd + Status	R/W
$A4_H$	Reserved				R/W
$A8_H$	Reserved				R/W
AC_H	Reserved				R/W
$B0_H$	Reserved		IDE1 Config + Status	IDE1 Cmd + Status	R/W
$B4_H$	Reserved				R/W
$B8_H$	Reserved				R/W
BC_H	Reserved				R/W
$C0_H$	BA5 Indirect Address				R/W
$C4_H$	BA5 Indirect Access				R/W

Table 6-1 Sil3112A PCI Configuration Space (continued)

6.1.1 Device ID – Vendor ID

Address Offset: 00_H
Access Type: Read /Write
Reset Value: 0x3112_1095

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device ID																Vendor ID															

This register defines the Device ID and Vendor ID associated with the SiI3112A. The register bits are defined below.

- **Bit [31:16]**: Device ID (R/W) – Device ID. This value in this bit field is determined by any one of three options:
  - 1) This field defaults to 0x3112 to identify the device as a Silicon Image SiI3112A.
  - 2) loaded from an external memory device : If an external memory device – FLASH or EEPROM – is present with the correct signature, the Device ID is loaded from that device after reset. See section 5 Auto-Initialization on page 31.
  - 3) system programmable : If Bit 0 of the Configuration register (40_H) is set, the bytes are system programmable.
- **Bit [15:00]**: Vendor ID (R) – Vendor ID. This field defaults to 0x1095 to identify the vendor as Silicon Image.

6.1.2 PCI Status – PCI Command

Address Offset: 04_H
Access Type: Read/Write/Write-One-to-Clear
Reset Value: 0x02B0_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Det Par Err	Sig Sys Err	Rcvd M Abort	Rcvd T Abort	Sig T Abort	Devsel Timing		Det M Data Par Err	Fast B-to-B	Reserved	66 MHz Capable	Capabilities List	Reserved										Fast B-to-B	SERR Enable	Address Stepping	Par Error	VGA Palette	Memory Wr & Inv	Special Cycles	Bus Master	Memory Space	IO Space

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit 31**: Det. Par Err (R/W1C) – Detected Parity Error. This bit set indicates that the SiI3112A detected a parity error on the PCI bus-address or data parity error-while responding as a PCI target.
- **Bit 30**: Sig. Sys Err (R/W1C) – Signaled System Error. This bit set indicates that the SiI3112A signaled SERR on the PCI bus.
- **Bit 29**: Rcvd M Abort (R/W1C) – Received Master Abort. This bit set indicates that the SiI3112A terminated a PCI bus operation with a Master Abort.
- **Bit 28**: Rcvd T Abort (R/W1C) – Received Target Abort. This bit set indicates that the SiI3112A received a Target Abort termination.
- **Bit 27**: Sig. T Abort (R/W1C) – Signaled Target Abort. This bit set indicates that the SiI3112A terminated a PCI bus operation with a Target Abort.
- **Bit [26:25]**: Devsel Timing (R) – Device Select Timing. This bit field indicates the DEVSEL timing supported by the SiI3112A. The hardwired value is 01_B for Medium decode timing.
- **Bit 24**: Det M Data Par Err (R/W1C) – Detected Master Data Parity Error. This bit set indicates that the SiI3112A, as bus master, detected a parity error on the PCI bus. The parity error may be either reported by the target device via PERR# on a write operation or by the SiI3112A on a read operation.
- **Bit 23**: Fast B-to-B Capable (R) – Fast Back-to-Back Capable. This bit is hardwired to 1 to indicate that the SiI3112A is Fast Back-to-Back capable as a PCI target.
- **Bit 22**: Reserved (R).
- **Bit 21**: 66 MHz Capable (R) – 66 MHz PCI Operation Capable. This bit is hardwired to 1 to indicate that the SiI3112A is 66 MHz capable.
- **Bit 20**: Capabilities List (R) – PCI Capabilities List. This bit is hardwired to 1 to indicate that the SiI3112A has a PCI Power Management Capabilities register linked at offset 34_H.

- **Bit [19:10]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit 09**: Fast B-to-B Enable (R) – Fast Back-to-Back Enable. This bit is hardwired to 0 to indicate that the SiI3112A does not support Fast Back-to-Back operations as bus master.
- **Bit 08**: SERR Enable (R/W) – SERR Output Enable. This bit set enables the SiI3112A to drive the PCI SERR# pin when it detects an address parity error. The Parity Error Response bit (06) must also be set to enable SERR# reporting.
- **Bit 07**: Address Stepping (R) – Address Stepping Enable. This bit is hardwired to 0 to indicate that the SiI3112A does not support Address Stepping.
- **Bit 06**: Par Error Response (R/W) – Parity Error Response Enable. This bit set enables the SiI3112A to respond to parity errors on the PCI bus. If this bit is cleared, the SiI3112A will ignore PCI parity errors.
- **Bit 05**: VGA Palette (R) – VGA Palette Snoop Enable. This bit is hardwired to 0 to indicate that the SiI3112A does not support VGA Palette Snooping.
- **Bit 04**: Mem Wr & Inv (R) – Memory Write and Invalidate Enable. This bit is hardwired to 0 to indicate that the SiI3112A does not support Memory Write and Invalidate.
- **Bit 03**: Special Cycles (R) – Special Cycles Enable. This bit is hardwired to 0 to indicate that the SiI3112A does not respond to Special Cycles.
- **Bit 02**: Bus Master (R/W) – Bus Master Enable. This bit set enables the SiI3112A to act as PCI bus master.
- **Bit 01**: Memory Space (R/W) – Memory Space Enable. This bit set enables the SiI3112A to respond to PCI memory space access.
- **Bit 00**: IO Space (R/W) – IO Space Enable. This bit set enables the SiI3112A to respond to PCI IO space access.

6.1.3 PCI Class Code – Revision ID

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0180_0001 or 0x0104_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PCI Class Code																PCI Prog Int				IDE1 Mode Prog	IDE1 Pwr-Up Mode	IDE0 Mode Prog	IDE0 Pwr-Up Mode	Revision ID							

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:08]**: PCI Class Code (R) – PCI Class Code. This value in this bit field is determined by any one of three options:
  - 1) the default value, set by an external jumper on the FL_ADDR[00]/IDE_CFG pin:
    - If IDE_CFG = 0, the value is 010400h for RAID mode
    - If IDE_CFG = 1, the value is 018000h for Mass Storage class
  - 2) loaded from an external memory device : If an external memory device – FLASH or EEPROM – is present with the correct signature, the PCI Class Code is loaded from that device after reset. See section 5 Auto-Initialization on page 31.
  - 3) system programmable : If Bit 0 of the Configuration register (40_H) is set the three bytes are system programmable.
- **Bit [07:00]**: Revision ID (R) – Chip Revision ID. This bit field is hardwired to indicate the revision level of the chip design; revision 01_H is defined for SiI3112A rev 1.1 and revision 02_H is defined for SiI3112A rev 1.21.

6.1.4 BIST – Header Type – Latency Timer – Cache Line Size

Address Offset: $0C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BIST								Header Type								Latency Timer								Cache Line Size							

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: BIST (R). This bit field is hardwired to 00_H.
- **Bit [23:16]**: Header Type (R). This bit field is hardwired to 00_H.
- **Bit [15:08]**: Latency Timer (R/W). This bit field is used to specify the time in number of PCI clocks, the SiI3112A as a master is still allowed to control the PCI bus after its GRANT_L is deasserted. The lower four bits [0B:08] are hardwired to 0_H, resulting in a time granularity of 16 clocks.
- **Bit [07:00]**: Cache Line Size (R/W). This bit field is used to specify the system cacheline size in terms of 32-bit words. The upper 2 bits are not used, resulting a maximum size of 64 32-bit words. With the SiI3112A as a master, initiating a read transaction, it issues PCI command Read Multiple in place, when empty space in its FIFO is larger than the value programmed in this register.

6.1.5 Base Address Register 0

Address Offset: 10_H
Access Type: Read/Write
Reset Value: 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 0																													Not Used		

This register defines the addressing of various control functions within the SiI3112A. The register bits are defined below.

- **Bit [31:03]**: Base Address Register 0 (R/W). This register defines the I/O Space base address for the IDE Channel #0 task file registers.
- **Bit [02:00]**: Base Address Register 0 (R). This bit field is not used and is hardwired to 001_B

6.1.6 Base Address Register 1

Address Offset: 14_H
Access Type: Read/Write
Reset Value: 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 1																														Not Used	

This register defines the addressing of various control functions within the SiI3112A. The register bits are defined below.

- **Bit [31:02]**: Base Address Register 1 (R/W). This register defines the I/O Space base address for the IDE Channel #0 Device Control- Alternate Status register.
- **Bit [01:00]**: Base Address Register 1 (R). This bit field is not used and is hardwired to 01_B.

6.1.7 Base Address Register 2

Address Offset: 18_H
Access Type: Read/Write
Reset Value: 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 2																													Not Used		

This register defines the addressing of various control functions within the SiI3112A. The register bits are defined below.

- **Bit [31:03]**: Base Address Register 2 (R/W). This register defines the I/O Space base address for the IDE Channel #1 task file registers.
- **Bit [02:00]**: Base Address Register 2 (R). This bit field is not used and is hardwired to 001_B.

6.1.8 Base Address Register 3

Address Offset: $1C_H$
Access Type: Read/Write
Reset Value: 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 3																														Not Used	

This register defines the addressing of various control functions within the SiI3112A. The register bits are defined below.

- **Bit [31:02]**: Base Address Register 3 (R/W). This register defines the I/O Space base address for the IDE Channel #1 Device Control- Alternate Status register.
- **Bit [01:00]**: Base Address Register 3 (R). This bit field is not used and is hardwired to 01_B.

6.1.9 Base Address Register 4

Address Offset: 20_H
Access Type: Read/Write
Reset Value: 0x0000_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 4																												Not Used			

This register defines the addressing of various control functions within the SiI3112A. The register bits are defined below.

- **Bit [31:04]**: Base Address Register 4 (R/W). This register defines the I/O Space base address for the PCI bus master registers.
- **Bit [03:00]**: Base Address Register 4 (R). This bit field is not used and is hardwired to 0001_B.

6.1.10 Base Address Register 5

Address Offset: 24_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 5																							Not Used								

This register defines the addressing of various control functions within the SiI3112A. This register is enabled when input BA5_EN is set to one (see description for pin FL_ADDR[01]/BA5_EN in section 3.3.2 on page 26). The register bits are defined below.

- **Bit [31:09]**: Base Address Register 5 (R/W). This register defines the Memory Space base address for all Silicon Image driver specific functions.
- **Bit [08:00]**: Base Address Register 5 (R). This bit field is not used and is hardwired to 00_H.

6.1.11 Subsystem ID – Subsystem Vendor ID

Address Offset: $2C_H$
Access Type: Read/Write
Reset Value: 0x3112_1095

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Subsystem ID																Subsystem Vendor ID															

This register defines the Subsystem ID fields associated with the PCI bus. The register bits are defined below.

- **Bit [31:16]**: Subsystem ID (R) – Subsystem ID.

The value in this bit field is determined by any one of three options:

  - 1) the default value of 0x3112
  - 2) loaded from an external memory device : If an external memory device – FLASH or EEPROM – is present with the correct signature, the Subsystem ID is loaded from that device after reset. See section 5 Auto-Initialization on page 31.
  - 3) system programmable : If Bit 0 of the Configuration register (40_H) is set the two bytes are system programmable.

- **Bit [15:00]**: Subsystem Vendor ID (R) – Subsystem Vendor ID.

The value in this bit field is determined by any one of three options:

  - 1) the default value of 0x1095
  - 2) loaded from an external memory device : If an external memory device – FLASH or EEPROM – is present with the correct signature, the Subsystem Vendor ID is loaded from that device after reset. See section 5 Auto-Initialization on page 31.
  - 3) system programmable : If Bit 0 of the Configuration register (40_H) is set the two bytes are system programmable.

6.1.12 Expansion ROM Base Address

Address Offset: 30_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Expansion ROM Base Address													Not Used																		Exp ROM Enable

This register defines the Expansion ROM base address associated with the PCI bus. The register bits are defined below.

- **Bit [31:19]**: Expansion ROM Base Address (R/W) – Expansion ROM Base Address. This bit field defines the upper bits of the Expansion ROM base address.
- **Bit [18:01]**: Not Used (R). This bit field is hardwired to 00000_H. The minimum Expansion ROM address range is 512K bytes.
- **Bit [00]**: Exp ROM Enable (R/W) – Expansion ROM Enable. This bit is set to enable the Expansion ROM access.

6.1.13 Capabilities Pointer

Address Offset: 34_H
Access Type: Read
Reset Value: 0x0000_0060

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Capabilities Pointer							

This register defines the link to a list of new capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:00]**: Capabilities Pointer (R) – Capabilities Pointer. This bit field defaults to 60_H to define the address for the 1st entry in a list of PCI Power Management capabilities.

6.1.14 Max Latency – Min Grant – Interrupt Pin – Interrupt Line

Address Offset: $3C_H$
Access Type: Read/Write
Reset Value: 0x0000_0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Max Latency								Min Grant								Interrupt Pin								Interrupt Line							

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: Max Latency (R) – Maximum Latency. This bit field is hardwired to 00_H.
- **Bit [23:16]**: Min Grant (R) – Minimum Grant. This bit field is hardwired to 00_H.
- **Bit [15:08]**: Interrupt Pin (R) – Interrupt Pin Used. This bit field is hardwired to 01_H to indicate that the SiI3112A uses the INTA# interrupt.

- **Bit [07:00]**: Interrupt Line (R/W) – Interrupt Line. This bit field is used by the system to indicate interrupt line routing information. The SiI3112A does not use this information.

6.1.15 Configuration

Address Offset: 40_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																														BA5 Ind Acc Ena	PCI Hdr Wr Ena

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:02]**: Reserved (R). This bit field is hardwired to 00000000_H.
- **Bit [01]**: BA5 Ind Acc Ena (R/W) – BA5 Indirect Access Enable. This bit is set to enable indirect access to BA5 address space using Configuration Space registers $C0_H$ and $C4_H$ (BA5 Indirect Address and BA5 Indirect Access).
- **Bit [00]**: PCI Hdr Wr Ena (R/W) – PCI Configuration Header Write Enable. This bit is set to enable write access to the following registers in the PCI Configuration Header: Device ID ($03\text{-}02_H$), PCI Class Code ($09\text{-}0B_H$), Subsystem Vendor ID ($2D\text{-}2C_H$), and Subsystem ID ($2F\text{-}2E_H$).

6.1.16 Software Data Register

Address Offset: 44_H
Access Type: Read/Write
Reset Value: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Software Data																															

This register is used by the software for non-resettable data storage. The contents are unknown on power-up and are never cleared by any type of reset.

6.1.17 Power Management Capabilities

Address Offset: 60_H
Access Type: Read Only
Reset Value: 0x0622_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PME Support					PPM D2 Support	PPM D1 Support	Auxiliary Current			Dev Special Init	Reserved	PME Clock	PPM Rev			Next Item Pointer								Capability ID							

This register defines the power management capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:27]**: PME Support (R) – Power Management Event Support. This bit field is hardwired to 00_H to indicate that the SiI3112A does not support PME.
- **Bit [26]**: PPM D2 Support (R) – PCI Power Management D2 Support. This bit is hardwired to 1 to indicate support for the D2 Power Management State.
- **Bit [25]**: PPM D1 Support (R) – PCI Power Management D1 Support. This bit is hardwired to 1 to indicate support for the D1 Power Management State.
- **Bit [24:22]**: Auxiliary Current (R) – Auxiliary Current. This bit field is hardwired to 000_B.
- **Bit [21]**: Dev Special Init (R) – Device Special Initialization. This bit is hardwired to 1 to indicate that the SiI3112A requires special initialization
- **Bit [20]**: Reserved (R). This bit is reserved and returns zero on a read.
- **Bit [19]**: PME Clock (R) – Power Management Event Clock. This bit is hardwired to 0. The SiI3112A does not support PME.
- **Bit [18:16]**: PPM Rev (R) – PCI Power Management Revision. This bit field is hardwired to 010_B to indicate compliance with the PCI Power Management Interface Specification revision 1.1.
- **Bit [15:08]**: Next Item Pointer (R) – PCI Additional Capability Next Item Pointer. This bit field is hardwired to 00_H to indicate that there are no additional items on the Capabilities List.
- **Bit [07:00]**: Capability ID (R) – PCI Additional Capability ID. This bit field is hardwired to 01_H to indicate that this Capabilities List is a PCI Power Management definition.

6.1.18 Power Management Control + Status

Address Offset: 64_H
Access Type: Read/Write
Reset Value: 0x6400_4000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PPM Data								Reserved								PME Status	PPM Data Scale		PPM Data Sel				PME Ena	Reserved						PPM Power State	

This register defines the power management capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: PPM Data (R) – PCI Power Management Data. This bit field is hardwired to 0x64.
- **Bit [23:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [15]**: PME Status (R) – PME Status. This bit is hardwired to 0. The SiI3112A does not support PME.
- **Bit [14:13]**: PPM Data Scale (R) – PCI Power Management Data Scale. This bit field is hardwired to 10_B to indicate a scaling factor of ten milliwatts.
- **Bit [12:09]**: PPM Data Sel (R/W) – PCI Power Management Data Select. This bit field is set by the system to indicate which data field is to be reported through the PPM Data bits (although current implementation hardwires the PPM Data to indicate 1 Watt).
- **Bit [08]**: PME Ena (R) – PME Enable. This bit is hardwired to 0. The SiI3112A does not support PME.
- **Bit [07:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: PPM Power State (R/W) – PCI Power Management Power State. This bit field is set by the system to dictate the current Power State: 00 = D0 (Normal Operation), 01 = D1, 10 = D2, and 11 = D3 (Hot).

6.1.19 PCI Bus Master – IDE0

Address Offset: 70_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE0 DMA Comp	PBM Error	PBM Active	Reserved								Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #0 in the SiI3112A. The register bits are also mapped to Base Address 4, Offset 00_H, Base Address 5, Offset 00_H, and Base Address 5, Offset 10_H. See section 6.7.1 for bit definitions.

6.1.20 PRD Table Address – IDE0

Address Offset: 74_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE0																														Reserved	

This register defines the PRD Table Address register for IDE Channel #0 in the SiI3112A. The register bits are also mapped to Base Address 4, Offset 04_H and Base Address 5, Offset 04_H. See section 6.7.2 for bit definitions.

6.1.21 PCI Bus Master – IDE1

Address Offset: 78_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE1 DMA Comp	PBM Error	PBM Active	Reserved								Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #1 in the SiI3112A. The register bits are also mapped to Base Address 4, Offset 08_H, Base Address 5, Offset 08_H, and Base Address 5, Offset 18_H. See section 6.7.3 for bit definitions.

6.1.22 PRD Table Address – IDE1

Address Offset: $7C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE1																														Reserved	

This register defines the PRD Table Address register for IDE Channel #1 in the SiI3112A. The register bits are also mapped to Base Address 4, Offset $0C_H$ and Base Address 5, Offset $0C_H$. See section 6.7.4 for bit definitions.

6.1.23 Data Transfer Mode – IDE0

Address Offset: 80_H
Access Type: Read/Write
Reset Value: 0x0000_0022

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Reserved		IDE0 Device 1 Transfer Mode		Reserved		IDE0 Device 0 Transfer Mode	

This register defines the transfer mode register for IDE Channel #0 in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $B4_H$. See section 6.7.34 for bit definitions.

6.1.24 Data Transfer Mode – IDE1

Address Offset: 84_H
Access Type: Read/Write
Reset Value: 0x0000_0022

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Reserved		IDE1 Device 1 Transfer Mode		Reserved		IDE1 Device 0 Transfer Mode	

This register defines the transfer mode register for IDE Channel #1 in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $F4_H$. See section 6.7.44 for bit definitions.

6.1.25 System Configuration Status – Command

Address Offset: 88_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE1 Int Block	IDE0 Int Block	Reserved					BA5_EN	Reserved								IDE0 Module Rst	IDE1 Module Rst	FF0 Module Rst	FF1 Module Rst	Reserved		ARB Module Rst	PBM Module Rst

This register defines the system configuration status and command register for the SiI3112A. The register bits are also mapped to Base Address 5, Offset 48_H. See Section 6.7.13 for bit definitions.

6.1.26 System Software Data Register

Address Offset: $8C_H$
Access Type: Read/Write
Reset Value: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
System Software Data																															

This register is used by the software for non-resettable data storage. The contents are unknown on power-up and are never cleared by any type of reset. The register bits are also mapped to Base Address 5, Offset $4C_H$. See Section 6.7.14 for bit definitions.

6.1.27 FLASH Memory Address – Command + Status

Address Offset: 90_H
Access Type: Read/Write
Reset Value: 0x0800_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved				Mem Init Done	Mem Init	Mem Access Start	Mem Access Type	Reserved					Memory Address																		

This register defines the address and command/status register for FLASH memory interface in the SiI3112A. The register bits are also mapped to Base Address 5, Offset 50_H. See section 6.7.15 for bit definitions.

6.1.28 FLASH Memory Data

Address Offset: 94_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Memory Data							

This register defines the data register for FLASH memory interface in the SiI3112A. The register bits are also mapped to Base Address 5, Offset 54_H. See Section 6.7.16 for bit definitions.

6.1.29 EEPROM Memory Address – Command + Status

Address Offset: 98_H
Access Type: Read/Write
Reset Value: 0x0800_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved			Mem Error	Mem Init Done	Mem Init	Mem Access Start	Mem Access Type	Reserved								Mem Address															

This register defines the address and command/status register for EEPROM memory interface in the SiI3112A. The register bits are also mapped to Base Address 5, Offset 58_H. See Section 6.7.17 for bit definitions.

6.1.30 EEPROM Memory Data

Address Offset: $9C_H$
Access Type: Read/Write
Reset Value: 0x0000_00XX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Memory Data							

This register defines the data register for EEPROM memory interface in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $5C_H$. See Section 6.7.18 for bit definitions.

6.1.31 IDE0 Task File Configuration + Status

Address Offset: $A0_H$
Access Type: Read/Write
Reset Value: 0x6515_0101

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																Reserved	Watchdog Int Ena	Watchdog Ena	Watchdog Timeout	Interrupt Status	Virtual DMA Int	IORDY Monitoring	Reserved						Channel Rst	Buffered Cmd	Reserved

This register defines the task file configuration and status register for IDE Channel #0 in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $A0_H$. See section 6.7.33 for bit definitions.

6.1.32 IDE1 Task File Configuration + Status

Address Offset: $B0_H$
Access Type: Read/Write
Reset Value: 0x6515_0101

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																Reserved	Watchdog Int Ena	Watchdog Ena	Watchdog Timeout	Interrupt Status	Virtual DMA Int	IORDY Monitoring	Reserved						Channel Rst	Buffered Cmd	Reserved

This register defines the task file configuration and status register for IDE Channel #1 in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $E0_H$. See Section 6.7.43 for bit definitions.

6.1.33 BA5 Indirect Address

Address Offset: $C0_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																							Address								

This register permits the indirect addressing of registers normally referenced using Base Address 5. Any register that is not accessible by any means other that via Base Address 5 is indirectly addressable. The following BA5 address ranges are not indirectly accessible, but are accessible either in Configuration Space or via other Base Address registers: 00-$1C_H$, 80-$8C_H$, C0-CC_H.

6.1.34 BA5 Indirect Access

Address Offset: $C4_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
As defined for indirectly accessed register																															

This register provides the indirect access addressed by the BA5 Indirect Address register. The use of indirect access must be enabled by setting bit 1 of the Configuration register (40_H).

6.2 Internal Register Space – Base Address 0

These registers are 32-bits wide and define the internal operation of the SiI3112A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	IDE0 TF Starting Sector Number	IDE0 TF Sector Count	IDE0 TF Features IDE0 TF Error	IDE0 TF Data	R/W
04_H	IDE0 TF Command+Status	IDE0 TF Device+Head	IDE0 TF Cylinder High	IDE0 TF Cylinder Low	R/W

Table 6-2 SiI3112A Internal Register Space – Base Address 0

6.2.1 IDE0 Task File Register 0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Starting Sector Number								IDE0 Task File Sector Count								IDE0 Task File Features (W) IDE0 Task File Error (R)								IDE0 Task File Data							

This register defines four of the IDE Channel #0 Task File registers in the SiI3112A. The register bits are also mapped to Base Address 5, Offset 80_H. See section 6.7.25 for bit definitions.

6.2.2 IDE0 Task File Register 1

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Command + Status								IDE0 Task File Device+Head								IDE0 Task File Cylinder High								IDE0 Task File Cylinder Low							

This register defines four of the IDE Channel #0 Task File registers in the SiI3112A. The register bits are also mapped to Base Address 5, Offset 84_H. See section 6.7.26 for bit definitions.

6.3 Internal Register Space – Base Address 1

These registers are 32-bits wide and define the internal operation of the SiI3112A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	IDE0 TF Device Control Auxiliary Status	Reserved	Reserved	R/W

Table 6-3 SiI3112A Internal Register Space – Base Address 1

6.3.1 IDE0 Task File Register 2

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE0 Task File Device Control IDE0 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #0 Task File registers in the SiI3112A. The register bits are also mapped to Base Address 5, Offset 88_H. See Section 6.7.27 for bit definitions.

6.4 Internal Register Space – Base Address 2

These registers are 32-bits wide and define the internal operation of the SiI3112A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	IDE1 TF Starting Sector Number	IDE1 TF Sector Count	IDE1 TF Features IDE1 TF Error	IDE1 TF Data	R/W
04_H	IDE1 TF Command+Status	IDE1 TF Device+Head	IDE1 TF Cylinder High	IDE1 TF Cylinder Low	R/W

Table 6-4 SiI3112A Internal Register Space – Base Address 2

6.4.1 IDE1 Task File Register 0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Starting Sector Number								IDE1 Task File Sector Count								IDE1 Task File Features (W) IDE1 Task File Error (R)								IDE1 Task File Data							

This register defines four of the IDE Channel #1 Task File registers in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $C0_H$. See section 6.7.35 for bit definitions.

6.4.2 IDE1 Task File Register 1

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Command + Status								IDE1 Task File Device+Head								IDE1 Task File Cylinder High								IDE1 Task File Cylinder Low							

This register defines four of the IDE Channel #1 Task File registers in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $C4_H$. See section 6.7.36 for bit definitions.

6.5 Internal Register Space – Base Address 3

These registers are 32-bits wide and define the internal operation of the SiI3112A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	IDE1 TF Device Control Auxiliary Status	Reserved	Reserved	R/W

Table 6-5 SiI3112A Internal Register Space – Base Address 3

6.5.1 IDE1 Task File Register 2

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE1 Task File Device Control IDE1 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #1 Task File registers in the SiI3112A. The register bits are also mapped to Base Address 5, Offset $C8_H$. See section 6.7.37 for bit definitions.

6.6 Internal Register Space – Base Address 4

These registers are 32-bits wide and define the internal operation of the SiI3112A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI I/O space.

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	PCI Bus Master Status – IDE0	Software Data	PCI Bus Master Command – IDE0	R/W
04_H	PRD Table Address – IDE0				R/W
08_H	Reserved	PCI Bus Master Status – IDE1	Reserved	PCI Bus Master Command – IDE1	R/W
$0C_H$	PRD Table Address – IDE1				R/W

Table 6-6 SiI3112A Internal Register Space – Base Address 4

6.6.1 PCI Bus Master – IDE0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_XX00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE0 DMA Comp	PBM Error	PBM Active	IDE Watchdog	IDE1 DMA Comp	Software						Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #0 in the SiI3112A. See Section 6.7.1 for bit definitions.

6.6.2 PRD Table Address – IDE0

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE0																														Reserved	

This register defines the PRD Table Address register for IDE Channel #0 in the SiI3112A. The register bits are also mapped to PCI Configuration Space, Offset 74_H and Base Address 5, Offset 04_H. See Section 6.7.2 for bit definitions.

6.6.3 PCI Bus Master – IDE1

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE1 DMA Comp	PBM Error	PBM Active	Reserved								Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #1 in the SiI3112A. See Section 6.7.3 for bit definitions.

6.6.4 PRD Table Address – IDE1

Address Offset: $0C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE1																														Reserved	

This register defines the PRD Table Address register for IDE Channel #1 in the SiI3112A. The register bits are also mapped to PCI Configuration Space, Offset $7C_H$ and Base Address 5, Offset $0C_H$. See Section 6.7.4 for bit definitions.

6.7 Internal Register Space – Base Address 5

These registers are 32-bits wide and define the internal operation of the SiI3112A. The access types are defined as follows: R=read, W=write, and C=clearable by some write operation. Access to this register is through the PCI Memory space. The Base Address 5 can be disabled by setting input BA5_EN to low

Address Offset	Register Name				Access Type
	31 16		15 00		
00_H	Reserved	PCI Bus Master Status – IDE0	Software Data	PCI Bus Master Command – IDE0	R/W
04_H	PRD Table Address – IDE0				R/W
08_H	Reserved	PCI Bus Master Status – IDE1	Reserved	PCI Bus Master Command – IDE1	R/W
$0C_H$	PRD Table Address – IDE1				R/W
10_H	PCI Bus Master Status – IDE1	PCI Bus Master Status2 – IDE0	Software Data	PCI Bus Master Command2 – IDE0	R/W
14_H	Reserved				-
18_H	Reserved	PCI Bus Master Status2 – IDE1	Reserved	PCI Bus Master Command2 – IDE1	R/W
$1C_H$	Reserved				-
20_H	PRD Address – IDE0				R
24_H	PCI Bus Master Byte Count – IDE0				R
28_H	PRD Address – IDE1				R
$2C_H$	PCI Bus Master Byte Count – IDE1				R
30_H	Reserved				-
34_H	Reserved				-
38_H	Reserved				-
$3C_H$	Reserved				-
40_H	FIFO Valid Byte Count – IDE0		FIFO Wr Request Control – IDE0	FIFO Rd Request Control – IDE0	R/W
44_H	FIFO Valid Byte Count – IDE1		FIFO Wr Request Control – IDE1	FIFO Rd Request Control – IDE1	R/W
48_H	System Configuration Status		System Command		R/W
$4C_H$	System Software Data				R/W
50_H	FLASH Memory Address – Command and Status				R/W
54_H	Reserved		GPIO Control	Flash Memory Data	R/W
58_H	EEPROM Memory Address – Command and Status				R/W
$5C_H$	Reserved			EEPROM Memory Data	R/W
60_H	FIFO Port – IDE0				R/W

Address Offset	Register Name				Access Type
	31 16		15 00		
64_H	Reserved				-
68_H	FIFO Byte1 Write Pointer – IDE0	FIFO Byte1 Read Pointer – IDE0	FIFO Byte0 Write Pointer – IDE0	FIFO Byte0 Read Pointer – IDE0	R
$6C_H$	FIFO Byte3 Write Pointer – IDE0	FIFO Byte3 Read Pointer – IDE0	FIFO Byte2 Write Pointer – IDE0	FIFO Byte2 Read Pointer – IDE0	R
70_H	FIFO Port – IDE1				R/W
74_H	Reserved				-
78_H	FIFO Byte1 Write Pointer – IDE1	FIFO Byte1 Read Pointer – IDE1	FIFO Byte0 Write Pointer – IDE1	FIFO Byte0 Read Pointer – IDE1	R
$7C_H$	FIFO Byte3 Write Pointer – IDE1	FIFO Byte3 Read Pointer – IDE1	FIFO Byte2 Write Pointer – IDE1	FIFO Byte2 Read Pointer – IDE1	R
80_H	IDE0 TF Starting Sector Number	IDE0 TF Sector Count	IDE0 TF Features IDE0 TF Error	IDE0 TF Data	R/W
84_H	IDE0 TF Command+Status	IDE0 TF Device+Head	IDE0 TF Cylinder High	IDE0 TF Cylinder Low	R/W
88_H	Reserved	IDE0 TF Device Control Auxiliary Status	Reserved	Reserved	R/W
$8C_H$	IDE0 Read Ahead Data				R/W
90_H	IDE0 TF Starting Sector Number2	IDE0 TF Sector Count2	IDE0 TF Features2 IDE0 TF Error2	Reserved	R/W
94_H	IDE0 TF Cmd+Sts2	IDE0 TF Device+Head2	IDE0 TF Cylinder High2	IDE0 TF Cylinder Low2	R/W
98_H	IDE0 TF Cylinder High 2 Ext	IDE0 TF Cylinder Low 2 Ext	IDE0 TF Starting Sector 2 Ext	IDE0 TF Sector Count 2 Ext	R/W
$9C_H$	IDE0 Virtual DMA/PIO Read Ahead Byte Count				R/W
$A0_H$	Reserved		IDE0 Config + Status	IDE0 Cmd + Status	R/W
$A4_H$	Reserved				R/W
$A8_H$	Reserved				R/W
AC_H	Reserved				R/W
$B0_H$	IDE0 Test Register				R/W
$B4_H$	Reserved			IDE0 Data Transfer Mode	R/W
$B8_H$	Reserved				-
BC_H	Reserved				-
$C0_H$	IDE1 TF Starting Sector Number	IDE1 TF Sector Count	IDE1 TF Features IDE1 TF Error	IDE1 TF Data	R/W
$C4_H$	IDE1 TF Command+Status	IDE1 TF Device+Head	IDE1 TF Cylinder High	IDE1 TF Cylinder Low	R/W

Address Offset	Register Name				Access Type
	31 16		15 00		
$C8_H$	Reserved	IDE1 TF Device Control Auxiliary Status	Reserved		R/W
CC_H	IDE1 Read Ahead Data				R/W
$D0_H$	IDE1 TF Starting Sector Number2	IDE1 TF Sector Count2	IDE1 TF Features2 IDE1 TF Error2	Reserved	R/W
$D4_H$	IDE1 TF Cmd+Sts2	IDE1 TF Device+Head2	IDE1 TF Cylinder High2	IDE1 TF Cylinder Low2	R/W
$D8_H$	IDE1 TF Cylinder High Ext 2	IDE1 TF Cylinder Low Ext 2	IDE1 TF Starting Sector Ext 2	IDE1 TF Sector Count Ext 2	R/W
DC_H	IDE1 Virtual DMA/PIO Read Ahead Byte Count				R/W
$E0_H$	Reserved		IDE1 Config + Status	IDE1 Cmd + Status	R/W
$E4_H$	Reserved				R/W
$E8_H$	Reserved				R/W
EC_H	Reserved				R/W
$F0_H$	IDE1 Test Register				R/W
$F4_H$	Reserved			IDE1 Data Transfer Mode	R/W
$F8_H$	Reserved				-
FC_H	Reserved				-
100_H	SControl (channel 0)				R/W
104_H	SStatus (channel 0)				R/W
108_H	SError (channel 0)				R/C
$10C_H$	Reserved				-
110_H	Reserved				-
114_H	Reserved				-
118_H	Reserved				-
$11C_H$	Reserved				-
120_H	Reserved				-
124_H	Reserved				-
128_H	Reserved				-
$12C_H$	Reserved				-
130_H	Reserved				-
134_H	Reserved				-
138_H	Reserved				-
$13C_H$	Reserved				-
140_H	SMisc (channel 0)				R/W

Address Offset	Register Name		Access Type
	31 16	15 00	
144_H	PHY Configuration		R/W
148_H	SIEN (channel 0)		R/W
$14C_H$	SFISCfg (channel 0)		R/W
150_H	Reserved		-
154_H	Reserved		-
158_H	Reserved		-
$15C_H$	Reserved		-
160_H	RxFIS0 (channel 0)		R
164_H	RxFIS1 (channel 0)		R
168_H	RxFIS2 (channel 0)		R
$16C_H$	RxFIS3 (channel 0)		R
170_H	RxFIS4 (channel 0)		R
174_H	RxFIS5 (channel 0)		R
178_H	RxFIS6 (channel 0)		R
$17C_H$	Reserved		-
180_H	SControl (channel 1)		R/W
184_H	SStatus (channel 1)		R/W
188_H	SError (channel 1)		R/C
$18C_H$	Reserved		-
190_H	Reserved		-
194_H	Reserved		-
198_H	Reserved		-
$19C_H$	Reserved		-
$1A0_H$	Reserved		-
$1A4_H$	Reserved		-
$1A8_H$	Reserved		-
$1AC_H$	Reserved		-
$1B0_H$	Reserved		-
$1B4_H$	Reserved		-
$1B8_H$	Reserved		-
$1BC_H$	Reserved		-
$1C0_H$	SMisc (channel 1)		R/W
$1C4_H$	PHY Configuration (same as 144_H)		R/W
$1C8_H$	SIEN (channel 1)		R/W
$1CC_H$	SFISCfg (channel 1)		R/W
$1D0_H$	Reserved		-

Address Offset	Register Name		Access Type
	31 16	15 00	
$1D4_H$	Reserved		-
$1D8_H$	Reserved		-
$1DC_H$	Reserved		-
$1E0_H$	RxFIS0 (channel 1)		R
$1E4_H$	RxFIS1 (channel 1)		R
$1E8_H$	RxFIS2 (channel 1)		R
$1EC_H$	RxFIS3 (channel 1)		R
$1F0_H$	RxFIS4 (channel 1)		R
$1F4_H$	RxFIS5 (channel 1)		R
$1F8_H$	RxFIS6 (channel 1)		R
$1FC_H$	Reserved		-

Table 6-7 SiI3112A Internal Register Space – Base Address 5

6.7.1 PCI Bus Master – IDE0

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_XX00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE0 DMA Comp	PBM Error	PBM Active	IDE Watchdog	IDE1 DMA Comp	Software						Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #0 in the SiI3112A. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20:19]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [18]**: IDE0 DMA Comp (R/W1C) – IDE0 DMA Completion Interrupt. During write DMA operation, This bit set indicates that the IDE0 interrupt has been asserted and all data has been written to system memory. During Read DMA, This bit set indicates that the IDE0 interrupt has been asserted. This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE0 interrupt line.
- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE0. This bit set indicates that a PCI bus error occurred while the SiI3112A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE0. This bit set indicates that the SiI3112A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.

- **Bit[15]** : IDE Watchdog Timer Status (R) – This bit is an Ored result of bit 12 in IDE0 Task File Timing + Configuration + Status and bit 12 of IDE1 Task File Timing + Configuration + Status registers. When set indicates that either IDE0 or IDE1 Watchdog timer has expired.
- **Bit[14]** : IDE1 Interrupt Status (R) – This bit is a copy of Bit[18] IDE1 DMA Completion Interrupt in PCI Bus Master – IDE1.
- **Bit [13:08]**: Software Data (R/W) – System Software Data Storage. This bit field is used for read/write data storage by the system. The properties of this bit field are detailed below.

Bit Location	Default	Description
[13:12]	XX_B	Not cleared by any reset
[11:10]	00_B	Cleared by PCI reset
[09:08]	XX_B	Cleared only by a D0-D3 power state change

Table 6-8 Software Data Byte, Base Address 5, Offset 00_H

- **Bit [07:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE0 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE0 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE0. This bit is set to enable PCI bus master operations for IDE Channel #0. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE0 Task File or PIO data registers will be terminated with Target-Abort.

6.7.2 PRD Table Address – IDE0

Address Offset: 04_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE0																														Reserved	

This register defines the PRD Table Address register for IDE Channel #0 in the SiI3112A. The register bits are defined below.

- **Bit [31:02]**: PRD Table Address (R/W) – Physical Region Descriptor Table Address. This bit field defines the Descriptor Table base address.
- **Bit [01:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

6.7.3 PCI Bus Master – IDE1

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	Reserved		IDE1 DMA Comp	PBM Error	PBM Active	Reserved								Reserved				PBM Rd-Wr	Reserved		PBM Enable

This register defines the PCI bus master register for IDE Channel #1 in the SiI3112A. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20:19]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [18]**: IDE1 DMA Comp (R/W1C) – IDE1 DMA Completion Interrupt. During write DMA operation, this bit set indicates that the IDE1 interrupt has been asserted and all data has been written to system memory. During Read DMA, this bit set indicates that the IDE1 interrupt has been asserted. This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE1 interrupt line.
- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE1. This bit set indicates that a PCI bus error occurred while the SiI3112A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE1. This bit set indicates that the SiI3112A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.
- **Bit [15:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:04]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE1 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE1 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE1. This bit is set to enable PCI bus master operations for IDE Channel #1. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE1 Task File or PIO data registers will be terminated with Target-Abort.

6.7.4 PRD Table Address – IDE1

Address Offset: $0C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Table Address – IDE1																														Reserved	

This register defines the PRD Table Address register for IDE Channel #1 in the SiI3112A. The register bits are defined below.

- **Bit [31:02]**: PRD Table Address (R/W) – Physical Region Descriptor Table Address. This bit field defines the Descriptor Table base address.
- **Bit [01:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

6.7.5 PCI Bus Master2 – IDE0

Address Offset: 10_H
Access Type: Read/Write
Reset Value: 0x0808_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 PBM Simplex	IDE1 PBM DMA Cap 0	IDE1 PBM DMA Cap 1	IDE1 Watchdog	IDE1 Buffer Empty	IDE1 DMA Comp	IDE1 PBM Error	IDE1 PBM Active	IDE0 PBM Simplex	IDE0 PBM DMA Cap 1	IDE0 PBM DMA Cap 0	IDE0 Watchdog	IDE0 Buffer Empty	IDE0 DMA Comp	IDE0 PBM Error	IDE0 PBM Active	IDE Watchdog	IDE1 DMA Comp	Software						Reserved	SATAINT1	Reserved	SATAINT0	PBM Rd-Wr	Reserved		PBM Enable

This register defines the second PCI bus master register for IDE Channel #0 in the SiI3112A. The system must access these register bits through this address to enable the Large Block Transfer Mode.

The register bits are defined below.

- **Bit [31:29]**: (R) These bits are copy of PCI Bus Master IDE1 bits [23:21].
- **Bit [28]**: IDE1 Watchdog (R) : This bit is a copy of bit 12 in IDE1 Task File Configuration + Status register.
- **Bit [27]**: IDE1 Buffer empty (R). This bit set indicates the IDE1 FIFO is empty.
- **Bit [26:24]**: (R) These bits are copy of PCI Bus Master IDE1 bits [18:16].
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20]**: IDE0 Watchdog (R) : This bit is a copy of bit 12 in IDE0 Task File Configuration + Status register.
- **Bit [19]** : IDE0 Buffer empty (R). This bit set indicates the IDE0 FIFO is empty.
- **Bit [18]**: IDE0 DMA Comp (R/W1C) – IDE0 DMA Completion Interrupt. During write DMA operation, this bit set indicates that the IDE0 interrupt has been asserted and all data has been written to system memory. During Read DMA, This bit set indicates that the IDE0 interrupt has been asserted. This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE0 interrupt line.
- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE0. This bit set indicates that a PCI bus error occurred while the SiI3112A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE0. This bit set indicates that the SiI3112A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.
- **Bit[15]** : IDE Watchdog Timer Status (R) – This bit is an Ored result of bit 12 in IDE1 Task File Timing + Configuration + Status and bit 12 of IDE0 Task File Timing + Configuration + Status registers. When set indicates that either IDE0 or IDE1 Watchdog timer has expired.
- **Bit[14]** : IDE1 DMA Completion Interrupt Status (R) – This bit is a copy of Bit[18] IDE1 DMA Completion Interrupt in PCI Bus Master – IDE1.
- **Bit [13:08]**: Software Data (R/W) – System Software Data Storage. This bit field is used for read/write data storage by the system. The properties of this bit field are detailed below.

Bit Location	Default	Description
[13:12]	XX_B	Not cleared by any reset
[11:10]	00_B	Cleared by PCI reset
[09:08]	XX_B	Cleared only by a D0-D3 power state change

Table 6-9 Software Data Byte, Base Address 5, Offset 10_H

- **Bit [07]**: Reserved (R). This bit is reserved and returns zeros on a read.

- **Bit [06]**: SATAINT1 – This bit is the logical OR of all Serial ATA interrupt sources for channel 1.
- **Bit [05]**: Reserved (R). This bit is reserved and returns zeros on a read.
- **Bit [04]**: SATAINT0 – This bit is the logical OR of all Serial ATA interrupt sources for channel 0.
- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE0 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE0 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE0. This bit is set to enable PCI bus master operations for IDE Channel #0. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE0 Task File or PIO data registers will be terminated with Target-Abort.

6.7.6 PCI Bus Master2 – IDE1

Address Offset: 18_H
Access Type: Read/Write
Reset Value: 0x0008_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								PBM Simplex	PBM DMA Cap 1	PBM DMA Cap 0	IDE1 Watchdog	IDE1 Buffer Empty	IDE1 DMA Comp	PBM Error	PBM Active	Reserved								Reserved			SATAINT1	PBM Rd-Wr	Reserved		PBM Enable

This register defines the second PCI bus master register for IDE Channel #1 in the SiI3112A. The system must access these register bits through this address to enable the Large Block Transfer Mode.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: PBM Simplex (R) – PCI Bus Master Simplex Only. This read-only bit field is hardwired to zero to indicate that both IDE channels can operate as PCI bus master at any time.
- **Bit [22]**: PBM DMA Cap 1 (R/W) – PCI Bus Master DMA Capable – Device 1. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [21]**: PBM DMA Cap 0 (R/W) – PCI Bus Master DMA Capable – Device 0. This bit field has no effect. The device is always capable of DMA as a PCI bus master.
- **Bit [20]**: IDE1 Watchdog (R) . This bit is a copy of bit 12 in IDE1 Task File Timing + Configuration + Status register.
- **Bit [19]** : IDE1 Buffer empty (R). This bit set indicates IDE1 FIFO is empty.
- **Bit [18]**: IDE1 DMA Comp (R/W1C) – IDE1 DMA Completion Interrupt. During write DMA operation, this bit set indicates that the IDE1 interrupt has been asserted and all data has been written to system memory. During Read DMA, this bit set indicates that the IDE1 interrupt has been asserted. This bit must be W1C by software when set during DMA operation (bit 0 is set). During normal operation, this bit reflects IDE1 interrupt line.
- **Bit [17]**: PBM Error (R/W1C) – PCI Bus Master Error – IDE1. This bit set indicates that a PCI bus error occurred while the SiI3112A was bus master. Additional information is available in the PCI Status register in PCI Configuration space.
- **Bit [16]**: PBM Active (R) – PCI Bus Master Active – IDE1. This bit set indicates that the SiI3112A is currently active in a data transfer as PCI bus master. This bit is cleared by the hardware when all data transfers have completed or PBM Enable bit is not set.
- **Bit [15:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:05]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [04]**: SATAINT1 – This bit is the logical OR of all Serial ATA interrupt sources for channel 1.
- **Bit [03]**: PBM Rd-Wr (R/W) – PCI Bus Master Read-Write Control. This bit is set to specify a DMA write operation from IDE1 to system memory. This bit is cleared to specify a DMA read operation from system memory to an IDE1 device.
- **Bit [02:01]**: Reserved (R). This bit field is reserved and returns zeros on a read.

- **Bit [00]**: PBM Enable (R/W) – PCI Bus Master Enable – IDE1. This bit is set to enable PCI bus master operations for IDE Channel #1. PCI bus master operations can be halted by clearing this bit, but will erase all state information in the control logic. If this bit is cleared while the PCI bus master is active, the operation will be aborted and the data discarded. While this bit is set, accessing IDE1 Task File or PIO data registers will be terminated with Target-Abort.

6.7.7 PRD Address – IDE0

Address Offset: 20_H
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Address																															

This register reflects the current DMA address and uses for diagnostic purposes only.

- **Bit [31:00]**: PRD Address (R) – This field is the current DMA0 Address.

6.7.8 PCI Bus Master Byte Count – IDE0

Address Offset: 24_H
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
End of Table	Byte Count High															Byte Count Low															

This register defines the byte count register in the PCI bus master logic for IDE Channel #0 in the SiI3112A. The register bits are defined below.

- **Bit [31]**: End of Table (R). This bit set indicates that this is the last entry in the PRD table.
- **Bit [30:16]** Byte Count High (R). This bit field is the PRD entry byte count extension for Large Block Transfer Mode. Under generic mode, this bit field is reserved and returns zeros on a read.
- **Bit [15:00]** Byte Count Low (R). This bit field reflects the current DMA0 byte count value.

6.7.9 PRD Address – IDE1

Address Offset: 28_H
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PRD Address																															

This register reflects the current DMA1 Address and uses for diagnostic purposes only.

- **Bit [31:00]**: PRD Address (R) – This field is the current DMA1 Address.

6.7.10 PCI Bus Master Byte Count – IDE1

Address Offset: $2C_H$
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
End of Table	Byte Count High															Byte Count Low															

This register defines the byte count register in the PCI bus master logic for IDE Channel #1 in the SiI3112A. The register bits are defined below.

- **Bit [31]**: End of Table (R). This bit set indicates that this is the last entry in the PRD table.
- **Bit [30:16]** Byte Count High (R). This bit field is the PRD entry byte count extension for Large Block Transfer Mode. Under generic mode, this bit field is reserved and returns zeros on a read.
- **Bit [15:00]** Byte Count Low (R). This bit field reflects the current DMA1 byte count value.

6.7.11 FIFO Valid Byte Count and Control – IDE0

Address Offset: 40_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved							FIFO Valid Byte Count – IDE0									Reserved					FIFO Wr Req Ctrl – IDE0			Reserved					FIFO Rd Req Ctrl – IDE0		

This register defines the FIFO valid byte count register and PCI bus request control for IDE Channel #0 in the SiI3112A. The register bits are defined below.

- **Bit [31:25]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [24:16]**: FIFO Valid Byte Count – IDE0 (R). This bit field provides the valid byte count for the data FIFO for IDE Channel #0. A value of 000_H indicates empty, while a value of 100_H indicates a full FIFO with 256 bytes.
- **Bit [15:11]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [10:08]**: FIFO Wr Req Ctrl – IDE0 (R/W) – FIFO Write Request Control. This bit field defines the FIFO threshold to assign DMA0 priority when requesting a PCI bus write operation. A value of 00_H indicates that DMA0 write request priority is set whenever the FIFO contains greater than 32 bytes, while a value of 07_H indicates that DMA0 write request priority is set whenever the FIFO contains greater than 7x32 bytes (=224 bytes). This bit field is useful when two DMA channels are competing for accessing PCI bus.

  When the two DMA channels request the PCI bus at the same time, the one with the higher priority will have the bus when it's granted to the SiI3112A. If the two DMA channels have the same priority, the channel that had the bus last will have the bus when it's granted to the SiI3112A.

  When one DMA channel is controlling the PCI bus, and the other channel requests the PCI bus, if the channel currently controlling the PCI bus has the same or higher priority, it remains controlling the bus. However, if the channel requesting the PCI bus has higher priority, the lower priority channel terminates the PCI transaction, yielding the bus to the channel with the higher priority.

- **Bit [07:03]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [02:00]**: FIFO Rd Req Ctrl – IDE0 (R/W) – FIFO Read Request Control. This bit field defines the FIFO threshold to assign DMA0 priority when requesting a PCI bus read operation. A value of 00_H indicates that DMA0 read request priority is set whenever the FIFO has greater than 32 bytes available space, while a value of 07_H indicates that DMA0 read request priority is set whenever the FIFO has greater than 7x32 bytes (=224 bytes) available space. This bit field is useful when two DMA channels are competing for accessing the PCI bus.

When the two DMA channels request the PCI bus at the same time, the channel that had the bus last will have the bus when it's granted to the SiI3112A.

6.7.12 FIFO Valid Byte Count and Control – IDE1

Address Offset: 44_H
Access Type: Read /Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								FIFO Valid Byte Count – IDE1								Reserved					FIFO Wr Req Ctrl – IDE1			Reserved						FIFO Rd Req Ctrl – IDE1	

This register defines the FIFO valid byte count register and PCI bus request control for IDE Channel #1 in the SiI3112A. The register bits are defined below.

- **Bit [31:25]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [24:16]**: FIFO Valid Byte Count – IDE1 (R). This bit field provides the valid byte count for the data FIFO for IDE Channel #1. A value of 000_H indicates empty, while a value of 100_H indicates a full FIFO with 256 bytes.
- **Bit [15:11]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [10:08]**: FIFO Wr Req Ctrl – IDE1 (R/W) – FIFO Write Request Control. This bit field defines the FIFO threshold to assign DMA1 priority when requesting a PCI bus write operation. A value of 00_H indicates that DMA1 write request priority is set whenever the FIFO contains greater than 32 bytes, while a value of 07_H indicates that DMA1 write request priority is set whenever the FIFO contains greater than 7x32 bytes (=224 bytes). This bit field is useful when two DMA channels are competing for accessing PCI bus.

  When the two DMA channels request the PCI bus at the same time, the one with the higher priority will have the bus when it's granted to the SiI3112A. If the two DMA channels have the same priority, the channel that had the bus last will have the bus when it's granted to the SiI3112A.

  When one DMA channel is controlling the PCI bus, and the other channel requests the PCI bus, if the channel currently controlling the PCI bus has the same or higher priority, it remains controlling the bus. However, if the channel requesting the PCI bus has higher priority, the lower priority channel terminates the PCI transaction, yielding the bus to the channel with the higher priority.

- **Bit [07:03]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [02:00]**: FIFO Rd Req Ctrl – IDE1 (R/W) – FIFO Read Request Control. This bit field defines the FIFO threshold to assign DMA1 priority when requesting a PCI bus read operation. A value of 00_H indicates that DMA1 read request priority is set whenever the FIFO has greater than 32 bytes available space, while a value of 07_H indicates that DMA1 read request priority is set whenever the FIFO has greater than 7x32 bytes (=224 bytes) available space. This bit field is useful when two DMA channels are competing for accessing the PCI bus.

  When the two DMA channels request the PCI bus at the same time, the channel that had the bus last will have the bus when it's granted to the SiI3112A.

6.7.13 System Configuration Status – Command

Address Offset: 48_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE1 Int Block	IDE0 Int Block	Reserved					M66EN	Reserved								IDE0 Module Rst	IDE1 Module Rst	FF0 Module Rst	FF1 Module Rst	Reserved		ARB Module Rst	PBM Module Rst

This register defines the system configuration status and command register for the SiI3112A. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23]**: IDE1 Int Block (R/W) – IDE1 Interrupt Block. This bit is set to block interrupts from the IDE Channel #1 to the PCI bus.
- **Bit [22]**: IDE0 Int Block (R/W) – IDE0 Interrupt Block. This bit is set to block interrupts from the IDE Channel #0 to the PCI bus.
- **Bit [21:17]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [16]**: M66EN (R) – PCI 66MHz Enable. This bit reflects input pin M66EN.
- **Bit [15:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07]**: IDE0 Module Rst (R/W) – IDE0 Module Reset. This bit is set to reset the interface logic for the IDE Channel #0.
- **Bit [06]**: IDE1 Module Rst (R/W) – IDE1 Module Reset. This bit is set to reset the interface logic for the IDE Channel #1.
- **Bit [05]**: FF0 Module Rst (R/W) – FF0 Module Reset. This bit is set to reset the logic in the FIFO for IDE Channel #0.
- **Bit [04]**: FF1 Module Rst (R/W) – FF1 Module Reset. This bit is set to reset the logic in the FIFO for IDE Channel #1.
- **Bit [03:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01]**: ARB Module Rst (R/W) – ARB Module Reset. This bit is set to reset the internal logic for the PCI-IDE arbiter.
- **Bit [00]**: PBM Module Rst (R/W) – PBM Module Reset. This bit is set to reset the internal logic for the PCI bus master state machine.

6.7.14 System Software Data Register

Address Offset: $4C_H$
Access Type: Read/Write
Reset Value: Undefined

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
System Software Data																															

This register is used by the software for non-resettable data storage. The contents are unknown on power-up and are never cleared by any type of reset.

6.7.15 FLASH Memory Address – Command + Status

Address Offset: 50_H
Access Type: Read/Write
Reset Value: 0x0800_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved				Mem Init Done	Mem Init	Mem Access Start	Mem Access Type	Reserved					Memory Address																		

This register defines the address and command/status register for FLASH memory interface in the SiI3112A. The register bits are defined below.

- **Bit [31:28]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [27]**: Memory Init Done (R) – This bit set indicates that the memory initialization sequence is done. The memory sequence is activated upon the release of reset.
- **Bit [26]**: Mem Init (R) – Memory Initialized. This bit set indicates that the memory was initialized properly (a correct data sequence was read from the FLASH.)

- **Bit [25]**: Mem Access Start (R/W) – Memory Access Start. This bit is set to initiate an operation to FLASH memory. This bit is cleared by the chip when the operation is complete.
- **Bit [24]**: Mem Access Type (R/W) – Memory Access Type. This bit is set to define a read operation from FLASH memory. This bit is cleared to define a write operation to FLASH memory.
- **Bit [23:19]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [18:00]**: Memory Address (R/W). This bit field is programmed with the address for a FLASH memory read or write access.

6.7.16 FLASH Memory Data

Address Offset: 54_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																Reserved								Memory Data							

This register defines the data register for the FLASH memory in the SiI3112A. The system writes to this register for a write operation to FLASH memory, and reads from this register on a read operation from FLASH memory.

- **Bit [31:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [15:08]**: Reserved (R)
- **Bit [07:00]**: Memory Data (R/W) – FLASH Memory Data. This bit field is used for FLASH write data on a write operation, and returns the FLASH read data on a read operation.

6.7.17 EEPROM Memory Address – Command + Status

Address Offset: 58_H
Access Type: Read/Write
Reset Value: 0x0800_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved			Mem Error	Mem Init Done	Mem Init	Mem Access Start	Mem Access Type	Reserved								Mem Address															

This register defines the address and command/status register for EEPROM memory interface in the SiI3112A. The register bits are defined below.

- **Bit [31:29]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [28]**: Mem Error (R/W1C) – Memory Access Error. This bit set indicates that the EEPROM interface logic detects three NAKs from the memory device (EEPROM most likely not present.)
- **Bit [27]**: Mem Init Done (R) – Memory Initialization Done. This bit set indicates that the memory initialization sequence is done. The memory initialization sequence is activated upon the release of reset.
- **Bit [26]**: Mem Init (R) – Memory Initialized. This bit set indicates that the memory was initialized properly (a correct data sequence was read from the EEPROM.)
- **Bit [25]**: Mem Access Start (R/W) – Memory Access Start. This bit is set to initiate an operation to EEPROM memory. This bit is cleared by the chip when the operation is complete.
- **Bit [24]**: Mem Access Type (R/W) – Memory Access Type. This bit is set to define a read operation from EEPROM memory. This bit is cleared to define a write operation to EEPROM memory.
- **Bit [23:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [15:00]**: Memory Address (R/W). This bit field is programmed with the address for an EEPROM read or write access.

6.7.18 EEPROM Memory Data

Address Offset: $5C_H$
Access Type: Read/Write
Reset Value: 0x0000_00XX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Memory Data							

This register defines the data register for EEPROM memory interface in the SiI3112A. The system writes to this register for a write operation to EEPROM memory, and reads from this register on a read operation from EEPROM memory. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:00]**: Memory Data (R/W) – EEPROM Memory Data. This bit field is used for EEPROM write data on a write operation, and returns the EEPROM read data on a read operation.

6.7.19 FIFO Port – IDE0

Address Offset: 60_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Port – IDE0																															

This register defines the direct access register for the FIFO port of IDE Channel #0 in the SiI3112A. This register is used for hardware debugging purposes only. The system can read from or write to this register for direct access to the data FIFO between the PCI bus and IDE Channel #0. While DMA0 is active, reading this register will be terminated with Target-Abort.

6.7.20 FIFO Pointers1– IDE0

Address Offset: 68_H
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 1 Wr Pointer – IDE0								FIFO Byte 1 Rd Pointer – IDE0								FIFO Byte 0 Wr Pointer – IDE0								FIFO Byte 0 Rd Pointer – IDE0							

This register provides visibility into the data FIFO for IDE Channel #0 in the SiI3112A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 1 Wr Pointer – IDE0 (R) FIFO Byte 1 Write Pointer. This bit field provides the status on the write pointer for Byte 1.
- **Bit [23:16]**: FIFO Byte 1 Rd Pointer – IDE0 (R) FIFO Byte 1 Read Pointer. This bit field provides the status on the read pointer for Byte 1.
- **Bit [15:08]**: FIFO Byte 0 Wr Pointer – IDE0 (R) FIFO Byte 0 Write Pointer. This bit field provides the status on the write pointer for Byte 0.

- **Bit [07:00]**: FIFO Byte 0 Rd Pointer – IDE0 (R) FIFO Byte 0 Read Pointer. This bit field provides the status on the read pointer for Byte 0.

6.7.21 FIFO Pointers2– IDE0

Address Offset: $6C_H$
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 3 Wr Pointer – IDE0								FIFO Byte 3 Rd Pointer – IDE0								FIFO Byte 2 Wr Pointer – IDE0								FIFO Byte 2 Rd Pointer – IDE0							

This register provides visibility into the data FIFO for IDE Channel #0 in the SiI3112A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 3 Wr Pointer – IDE0 (R) FIFO Byte 3 Write Pointer. This bit field provides the status on the write pointer for Byte 3.
- **Bit [23:16]**: FIFO Byte 3 Rd Pointer – IDE0 (R) FIFO Byte 3 Read Pointer. This bit field provides the status on the read pointer for Byte 3.
- **Bit [15:08]**: FIFO Byte 2 Wr Pointer – IDE0 (R) FIFO Byte 2 Write Pointer. This bit field provides the status on the write pointer for Byte 2.
- **Bit [07:00]**: FIFO Byte 2 Rd Pointer – IDE0 (R) FIFO Byte 2 Read Pointer. This bit field provides the status on the read pointer for Byte 2.

6.7.22 FIFO Port – IDE1

Address Offset: 70_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Port – IDE1																															

This register defines the direct access register for the FIFO port of IDE Channel #1 in the SiI3112A. This register is used for hardware debugging purposes only. The system can read from or write to this register for direct access to the data FIFO between the PCI bus and IDE Channel #1. While DMA1 is active, reading this register will be terminated with Target-Abort.

6.7.23 FIFO Pointers1– IDE1

Address Offset: 78_H
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 1 Wr Pointer – IDE1								FIFO Byte 1 Rd Pointer – IDE1								FIFO Byte 0 Wr Pointer – IDE1								FIFO Byte 0 Rd Pointer – IDE1							

This register provides visibility into the data FIFO for IDE Channel #1 in the SiI3112A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 1 Wr Pointer – IDE1 (R) FIFO Byte 1 Write Pointer. This bit field provides the status on the write pointer for Byte 1.
- **Bit [23:16]**: FIFO Byte 1 Rd Pointer – IDE1 (R) FIFO Byte 1 Read Pointer. This bit field provides the status on the read pointer for Byte 1.
- **Bit [15:08]**: FIFO Byte 0 Wr Pointer – IDE1 (R) FIFO Byte 0 Write Pointer. This bit field provides the status on the write pointer for Byte 0.
- **Bit [07:00]**: FIFO Byte 0 Rd Pointer – IDE1 (R) FIFO Byte 0 Read Pointer. This bit field provides the status on the read pointer for Byte 0.

6.7.24 FIFO Pointers2– IDE1

Address Offset: $7C_H$
Access Type: Read Only
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIFO Byte 3 Wr Pointer – IDE1								FIFO Byte 3 Rd Pointer – IDE1								FIFO Byte 2 Wr Pointer – IDE1								FIFO Byte 2 Rd Pointer – IDE1							

This register provides visibility into the data FIFO for IDE Channel #1 in the SiI3112A. The data FIFO is organized as a four byte-wide x 64 deep memory array. There are separate write and read pointer for each of the byte slices. This register is used for hardware debugging purposes only. The register bits are defined below.

- **Bit [31:24]**: FIFO Byte 3 Wr Pointer – IDE1 (R) FIFO Byte 3 Write Pointer. This bit field provides the status on the write pointer for Byte 3.
- **Bit [23:16]**: FIFO Byte 3 Rd Pointer – IDE1 (R) FIFO Byte 3 Read Pointer. This bit field provides the status on the read pointer for Byte 3.
- **Bit [15:08]**: FIFO Byte 2 Wr Pointer – IDE1 (R) FIFO Byte 2 Write Pointer. This bit field provides the status on the write pointer for Byte 2.
- **Bit [07:00]**: FIFO Byte 2 Rd Pointer – IDE1 (R) FIFO Byte 2 Read Pointer. This bit field provides the status on the read pointer for Byte 2.

6.7.25 IDE0 Task File Register 0

Address Offset: 80_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Starting Sector Number								IDE0 Task File Sector Count								IDE0 Task File Features (W) IDE0 Task File Error (R)								IDE0 Task File Data							

This register defines one of the IDE Channel #0 Task File registers in the SiI3112A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE0 Task File Data (R/W). This bit field defines the IDE0 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 0 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE0 Task File Starting Sector Number (R/W). This bit field defines the IDE0 Task File Starting Sector Number register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [23:16]**: IDE0 Task File Sector Count (R/W). This bit field defines the IDE0 Task File Sector Count register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.

- **Bit [15:08]**: IDE0 Task File Features (W). This write-only bit field defines the IDE0 Task File Features register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [15:08]**: IDE0 Task File Error (R). This read-only bit field defines the IDE0 Task File Error register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.

6.7.26 IDE0 Task File Register 1

Address Offset: 84_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Command + Status								IDE0 Task File Device+Head								IDE0 Task File Cylinder High								IDE0 Task File Cylinder Low							

This register defines one of the IDE Channel #0 Task File registers in the SiI3112A. Access to these bit field is permitted if the PCI bus Byte Enable is active for one byte only.

The register bits are defined below.

- **Bit [31:24]**: IDE0 Task File Command (W). This write-only bit field defines the IDE0 Task File Command register.
- **Bit [31:24]**: IDE0 Task File Status (R). This read-only bit field defines the IDE0 Task File Status register.
- **Bit [23:16]**: IDE0 Task File Device+Head (R/W). This bit field defines the IDE0 Task File Device and Head register.
- **Bit [15:08]**: IDE0 Task File Cylinder High (R/W). This bit field defines the IDE0 Task File Cylinder High register.
- **Bit [07:00]**: IDE0 Task File Cylinder Low (R/W). This bit field defines the IDE0 Task File Cylinder Low register.

6.7.27 IDE0 Task File Register 2

Address Offset: 88_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE0 Task File Device Control IDE0 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #0 Task File registers in the SiI3112A. Access to these bit fields is permitted if the PCI bus Byte Enable is active for one byte only.

The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23:16]**: IDE0 Task File Device Control (W). This bit field defines the IDE0 Task File Device Control register.
- **Bit [23:16]**: IDE0 Task File Auxiliary Status (R). This bit field defines the IDE0 Task File Auxiliary Status register.
- **Bit [15:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

6.7.28 IDE0 Read Ahead Data

Address Offset: $8C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Read Ahead Data																															

This register defines the read ahead data port for PIO transfers on IDE Channel #0 in the SiI3112A. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned.

6.7.29 IDE0 Task File Register 0 – Command Buffering

Address Offset: 90_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Starting Sector Number								IDE0 Task File Sector Count								IDE0 Task File Features (W) IDE0 Task File Error (R)								IDE0 Task File Data							

This register defines one of the IDE Channel #0 Task File registers used for Command Buffered accesses in the SiI3112A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE0 Task File Data (R/W). This bit field defines the IDE0 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 0 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE0 Task File Starting Sector Number (R/W). This bit field defines the IDE0 Task File Starting Sector Number register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 3 is active.
- **Bit [23:16]**: IDE0 Task File Sector Count (R/W). This bit field defines the IDE0 Task File Sector Count register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 2 is active.
- **Bit [15:08]**: IDE0 Task File Features (W). This write-only bit field defines the IDE0 Task File Features register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.
- **Bit [15:08]**: IDE0 Task File Error (R). This read-only bit field defines the IDE0 Task File Error register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.

6.7.30 IDE0 Task File Register 1 – Command Buffering

Address Offset: 94_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Command + Status								IDE0 Task File Device+Head								IDE0 Task File Cylinder High								IDE0 Task File Cylinder Low							

This register defines one of the IDE Channel #0 Task File registers used for Command Buffered accesses in the SiI3112A. The register bits are defined below.

- **Bit [31:24]**: IDE0 Task File Command (W). This write-only bit field defines the IDE0 Task File Command register.
- **Bit [31:24]**: IDE0 Task File Status (R). This read-only bit field defines the IDE0 Task File Status register.
- **Bit [23:16]**: IDE0 Task File Device+Head (R/W). This bit field defines the IDE0 Task File Device and Head register.
- **Bit [15:08]**: IDE0 Task File Cylinder High (R/W). This bit field defines the IDE0 Task File Cylinder High register.
- **Bit [07:00]**: IDE0 Task File Cylinder Low (R/W). This bit field defines the IDE0 Task File Cylinder Low register.

6.7.31 IDE0 Extended Task File Register – Command Buffering

Address Offset: 98_H
Access Type: Read/Write

Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Task File Cylinder High Ext								IDE0 Task File Cylinder Low Ext								IDE0 Task File Start Sector Ext								IDE0 Task File Sector Count Ext							

This register defines one of the IDE Channel #0 Task File registers used for Command Buffered accesses in the SiI3112. The register bits are defined below. If this register is written, the IDE0 Task File Device+Head byte of the IDE0 Task File Register 1 – Command Buffering register must not be written.

- **Bit [31:24]**: IDE0 Task File Cylinder High Ext(R/W). This write-only bit field defines the IDE0 Task File Extended Cylinder High register.
- **Bit [23:16]**: IDE0 Task File Cylinder Low Ext (R/W). This bit field defines the IDE0 Task File Extended Cylinder Low register.
- **Bit [15:08]**: IDE0 Task File Start Sector Ext (R/W). This bit field defines the IDE0 Task File Extended Start Sector register.
- **Bit [07:00]**: IDE0 Task File Sector Count Ext (R/W). This bit field defines the IDE0 Task File Extended Sector Count register.

6.7.32 IDE0 Virtual DMA/PIO Read Ahead Byte Count

Address Offset: $9C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE0 Virtual DMA/PIO Read Ahead Byte Count																															Not Used

This register defines the read ahead byte count register for Virtual DMA and PIO Read Ahead transfers on IDE Channel #0 in the SiI3112A. In Virtual DMA mode (PCI bus master DMA with PIO transfers on the IDE), all 32 bits are used as the word-aligned byte count. In PIO Read Ahead mode, only the lower 16 bits are used as the word-aligned byte count.

6.7.33 IDE0 Task File Configuration + Status

Address Offset: $A0_H$
Access Type: Read/Write
Reset Value: 0x6515_0101

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																Reserved	Watchdog Int Ena	Watchdog Ena	Watchdog Timeout	Interrupt Status	Virtual DMA Int	Reserved							Channel Rst	Buffered Cmd	Reserved

This register defines the task file configuration and status register for IDE Channel #0 in the SiI3112A. The register bits are defined below.

- **Bit [31:16]**: Reserved (R). This bit field is reserved and defaults to 0x6515.
- **Bit [15]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [14]** : Watchdog Int Ena (R/W) – IDE0 Watchdog Interrupt Enable. This bit is set to enable Interrupt when Watchdog timer expired.
- **Bit [13]**: Watchdog Ena (R/W) – IDE0 Watchdog Timer Enable. This bit is set to enable the watchdog timer for IDE0. This bit is cleared to disable the watchdog timer.
- **Bit [12]**: Watchdog Timeout (R/W1C) – IDE0 Watchdog Timer Timeout. This bit set indicates that the watchdog timer for IDE0 timed out. When enabled, and IORDY monitoring bit is also enabled, during IDE0 PIO opeartion, the watchdog counter starts counting when IORDY signal is deasserted. If after 256 PCI clocks, the IORDY signal is still deasserted, the Watchdog Timer is expires, and this bit is set and the SiI3112A continue its operation and stop monitoring IORDY signal. Software writes one to clear this bit. Once this bit is cleared, the SiI3112A starts monitoring IORDY on channel 0 again.
- **Bit [11]**: Interrupt Status (R) – IDE0 Interrupt Status. This bit set indicates that an interrupt is pending on IDE0. This bit provides real-time status of the IDE0 interrupt pin.
- **Bit [10]**: Virtual DMA Int (R) – IDE0 Virtual DMA Completion Interrupt. This bit set indicates that the Virtual DMA data transfer has completed. This bit is cleared when bit[0] PBM enable in PCI Bus Master – IDE0 is cleared .
- **Bit [09:03]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [02]**: Channel Rst (R/W) – IDE0 Channel Reset. When this bit is set, IDE Channel #0 RST signal is asserted.
- **Bit [01]**: Buffered Cmd (R) – IDE0 Buffered Command Active. This bit set indicates that a Buffered Command is currently active. This bit is set when the first command byte is written to the command buffer. This bit is cleared when all of the task file bytes, including the command byte, have been written to the device.
- **Bit [00]**: Reserved (R). This bit is reserved and returns one on a read.

6.7.34 Data Transfer Mode – IDE0

Address Offset: $B4_H$
Access Type: Read/Write
Reset Value: 0x0000_0022

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Reserved		IDE0 Device 1 Transfer Mode		Reserved		IDE0 Device 0 Transfer Mode	

This register defines the transfer mode register for IDE Channel #0 in the SiI3112A. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.

- **Bit [07:06]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [05:04]**: Device 1 Transfer Mode (R/W) – IDE0 Device 1 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B or 01_B = PIO transfer; 10_B or 11_B = DMA transfer.
- **Bit [03:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: Device 0 Transfer Mode (R/W) – IDE0 Device 0 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B or 01_B = PIO transfer; 10_B or 11_B = DMA transfer.

6.7.35 IDE1 Task File Register 0

Address Offset: $C0_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Starting Sector Number								IDE1 Task File Sector Count								IDE1 Task File Features (W) IDE1 Task File Error (R)								IDE1 Task File Data							

This register defines one of the IDE Channel #1 Task File registers in the SiI3112A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE1 Task File Data (R/W). This bit field defines the IDE1 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus Byte Enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 0 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE1 Task File Starting Sector Number (R/W). This bit field defines the IDE1 Task File Starting Sector Number register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [23:16]**: IDE1 Task File Sector Count (R/W). This bit field defines the IDE1 Task File Sector Count register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [15:08]**: IDE1 Task File Features (W). This write-only bit field defines the IDE1 Task File Features register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.
- **Bit [15:08]**: IDE1 Task File Error (R). This read-only bit field defines the IDE1 Task File Error register. Access to this bit field is permitted if the PCI bus Byte Enable is active for this byte only.

6.7.36 IDE1 Task File Register 1

Address Offset: $C4_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Command + Status								IDE1 Task File Device+Head								IDE1 Task File Cylinder High								IDE1 Task File Cylinder Low							

This register defines one of the IDE Channel #1 Task File registers in the SiI3112A. Access to these bit fields is permitted if the PCI bus Byte Enable is active for one byte only. The register bits are defined below.

- **Bit [31:24]**: IDE1 Task File Command (W). This write-only bit field defines the IDE1 Task File Command register.
- **Bit [31:24]**: IDE1 Task File Status (R). This read-only bit field defines the IDE1 Task File Status register.

- **Bit [23:16]**: IDE1 Task File Device+Head (R/W). This bit field defines the IDE1 Task File Device and Head register.
- **Bit [15:08]**: IDE1 Task File Cylinder High (R/W). This bit field defines the IDE1 Task File Cylinder High register.
- **Bit [07:00]**: IDE1 Task File Cylinder Low (R/W). This bit field defines the IDE1 Task File Cylinder Low register.

6.7.37 IDE1 Task File Register 2

Address Offset: $C8_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								IDE1 Task File Device Control IDE1 Task File Auxiliary Status								Reserved								Reserved							

This register defines one of the IDE Channel #1 Task File registers in the SiI3112A. Access to these bit fields is permitted if the PCI bus Byte Enable is active for one byte only. The register bits are defined below.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23:16]**: IDE1 Task File Device Control (W). This bit field defines the IDE1 Task File Device Control register.
- **Bit [23:16]**: IDE1 Task File Auxiliary Status (R). This bit field defines the IDE1 Task File Auxiliary Status register.
- **Bit [15:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

6.7.38 IDE1 Read/Write Ahead Data

Address Offset: CC_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Read Ahead Data																															

This register defines the read ahead data port for PIO transfers on IDE Channel #1 in the SiI3112A.

This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus byte enables. The data written to this register must be zero-aligned.

6.7.39 IDE1 Task File Register 0 – Command Buffering

Address Offset: $D0_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Starting Sector Number								IDE1 Task File Sector Count								IDE1 Task File Features (W) IDE1 Task File Error (R)								IDE1 Task File Data							

This register defines one of the IDE Channel #1 Task File registers used for Command Buffered accesses in the SiI3112A. Access to the individual bytes of this register is determined by the PCI bus Byte Enables at the time of the read or write operation. The register bits are defined below.

- **Bit [31:00]**: IDE1 Task File Data (R/W). This bit field defines the IDE1 Task File Data register. This register can be accessed as an 8-bit, 16-bit, or 32-bit word, depending upon the PCI bus byte enables. The data written to this register must be zero-aligned. To access 8-bit Task File Data, the PCI bus Byte Enable for byte 0 must be active. To access 16-bit Task File Data, the Byte Enables for byte 1 and byte 3 must be active. To access 32-bit Task File Data, the Byte Enables for all four bytes must be active.
- **Bit [31:24]**: IDE1 Task File Starting Sector Number (R/W). This bit field defines the IDE1 Task File Starting Sector Number register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 3 is active.
- **Bit [23:16]**: IDE1 Task File Sector Count (R/W). This bit field defines the IDE1 Task File Sector Count register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 2 is active.
- **Bit [15:08]**: IDE1 Task File Features (W). This write-only bit field defines the IDE1 Task File Features register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.
- **Bit [15:08]**: IDE1 Task File Error (R). This read-only bit field defines the IDE1 Task File Error register. Access to this bit field is permitted only if the PCI bus Byte Enable for byte 1 is active.

6.7.40 IDE1 Task File Register 1 – Command Buffering

Address Offset: $D4_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Command + Status								IDE1 Task File Device+Head								IDE1 Task File Cylinder High								IDE1 Task File Cylinder Low							

This register defines one of the IDE Channel #1 Task File registers used for Command Buffered accesses in the Sil3112A. The register bits are defined below.

- **Bit [31:24]**: IDE1 Task File Command (W). This write-only bit field defines the IDE1 Task File Command register.
- **Bit [31:24]**: IDE1 Task File Status (R). This read-only bit field defines the IDE1 Task File Status register.
- **Bit [23:16]**: IDE1 Task File Device+Head (R/W). This bit field defines the IDE1 Task File Device and Head register.
- **Bit [15:08]**: IDE1 Task File Cylinder High (R/W). This bit field defines the IDE1 Task File Cylinder High register.
- **Bit [07:00]**: IDE1 Task File Cylinder Low (R/W). This bit field defines the IDE1 Task File Cylinder Low register.

6.7.41 IDE1 Extended Task File Register – Command Buffering

Address Offset: $D8_H$
Access Type: Read/Write

Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDE1 Task File Cylinder High Ext								IDE1 Task File Cylinder Low Ext								IDE1 Task File Start Sector Ext								IDE1 Task File Sector Count Ext							

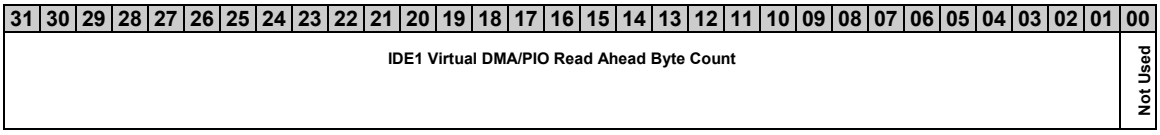
This register defines one of the IDE Channel #1 Task File registers used for Command Buffered accesses in the Sil3112. The register bits are defined below. If this register is written, the IDE1 Task File Device+Head byte of the IDE1 Task File Register 1 – Command Buffering register must not be written.

- **Bit [31:24]**: IDE1 Task File Cylinder High Ext(R/W). This write-only bit field defines the IDE1 Task File Extended Cylinder High register.
- **Bit [23:16]**: IDE1 Task File Cylinder Low Ext (R/W). This bit field defines the IDE1 Task File Extended Cylinder Low register.

- **Bit [15:08]**: IDE1 Task File Start Sector Ext (R/W). This bit field defines the IDE1 Task File Extended Start Sector register.
- **Bit [07:00]**: IDE1 Task File Sector Count Ext (R/W). This bit field defines the IDE1 Task File Extended Sector Count register.

6.7.42 IDE1 Virtual DMA/PIO Read Ahead Byte Count

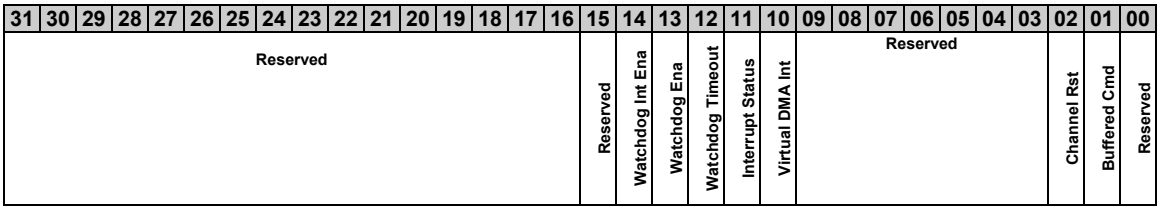
Address Offset: DC_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register defines the read ahead byte count register for Virtual DMA and PIO Read Ahead transfers on IDE Channel #1 in the SiI3112A. In Virtual DMA mode (PCI bus master DMA with PIO transfers on the IDE), all 32 bits are used as the word-aligned byte count. In PIO Read Ahead mode, only the lower 16 bits are used as the word-aligned byte count.

6.7.43 IDE1 Task File Configuration + Status

Address Offset: $E0_H$
Access Type: Read/Write
Reset Value: 0x6515_0101



This register defines the task file configuration and status register for IDE Channel #1 in the SiI3112A. The register bits are defined below.

- **Bit [31:16]**: Reserved (R). This bit field is reserved and defaults to 0x6515.
- **Bit [15]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [14]** : Watchdog Int Ena (R/W) – IDE1 Watchdog Interrupt Enable. This bit is set to enable Interrupt when Watchdog timer expired.
- **Bit [13]**: Watchdog Ena (R/W) – IDE1 Watchdog Timer Enable. This bit is set to enable the watchdog timer for IDE1. This bit is cleared to disable the watchdog timer.
- **Bit [12]**: Watchdog Timeout (R) – IDE1 Watchdog Timer Timeout. This bit set indicates that the watchdog timer for IDE1 timed out. When enabled, and IORDY monitoring bit is also enabled, during IDE0 PIO opeartion, the watchdog counter starts counting when IORDY signal is deasserted. If after 256 PCI clocks cycles, the IORDY signal is still deasserted, the Watchdog Timer is expires, and this bit is set and the SiI3112A continue its operation and stop monitoring IORDY signal. Software writes one to clear this bit. Once this bit is cleared, the SiI3112A starts monitoring IORDY on channel 1 again.
- **Bit [11]**: Interrupt Status (R) – IDE1 Interrupt Status. This bit set indicates that an interrupt is pending on IDE1. This bit provides real-time status of the IDE1 interrupt pin.
- **Bit [10]**: Virtual DMA Int (R) – IDE1 Virtual DMA Completion Interrupt. This bit set indicates that the Virtual DMA data transfer has completed. This bit is cleared when bit[0] PBM enable in PCI Bus Master – IDE1 is cleared .
- **Bit [09:03]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [02]**: Channel Rst (R/W) – IDE1 Channel Reset. When this bit is set, IDE Channel # 1 RST signal is asserted.

- **Bit [01]**: Buffered Cmd (R) – IDE1 Buffered Command Active. This bit set indicates that a Buffered Command is currently active. This bit is set when the first command byte is written to the comand buffer. This bit is cleared when all of the task file bytes, including the command byte, have been written to the device.
- **Bit [00]**: Reserved (R). This bit field is reserved and returns one on a read.

6.7.44 Data Transfer Mode – IDE1

Address Offset: $F4_H$
Access Type: Read/Write
Reset Value: 0x0000_0022

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Reserved		IDE1 Device 1 Transfer Mode		Reserved		IDE1 Device 0 Transfer Mode	

This register defines the transfer mode register for IDE Channel #1 in the SiI3112A. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:06]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [05:04]**: Device 1 Transfer Mode (R/W) – IDE1 Device 1 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B or 01_B = PIO transfer; 10_B or 11_B = DMA transfer.
- **Bit [03:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: Device 0 Transfer Mode (R/W) – IDE0 Device 0 Data Transfer Mode. This bit field is used to set the data transfer mode on IDE side during PCI DMA transfer: 00_B or 01_B = PIO transfer; 10_B or 11_B = DMA transfer.

6.7.45 Serial ATA SControl

Address Offset: 100_H (channel 0) / 180_H (channel 1)
Access Type: Read/Write
Reset Value: 0x0000_0010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																				IPM				SPD				DET			

This register is the SControl register as defined by the Serial ATA specification (section 8.1.3).

- **Bit [31:12]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [11:08]**: IPM – This field identifies the interface power management states that may be invoked via the Serial ATA interface power management capabilities.

Value	Definition
0000	No interface power management restrictions (Partial and Slumber modes enabled)
0001	Transitions to the Partial power management state are disabledd
0010	Transitions to the Slumber power management state are disabled
0011	Transitions to both the Partial and Slumber power management states are disabled
others	Reserved

- **Bit [07:04]**: SPD – This field identifies the highest allowed communication speed the interface is allowed to negotiate.

Value	Definition
0000	No restrictions
0001	Limit to Generation 1 (1.5 Gb/s) (default value)
others	Reserved

- **Bit [03:00]**: DET – This field controls host adapter device detection and interface initialization.

Value	Action
0000	No action
0001	ATA Reset is generated until another value is written to the field
0100	No action
others	Reserved, no action

6.7.46 Serial ATA Sstatus

Address Offset: 104_H (channel 0) / 184_H (channel 1)
Access Type: Read
Reset Value: 0x0000_00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																				IPM				SPD				DET			

This register is the SStatus register as defined by the Serial ATA specification (section 10.1.1).

- **Bit [31:12]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [11:08]**: IPM – This field identifies the current interface power management state.

Value	Definition
0000	Device not present or communication not established
0001	Interface in active state
0010	Interface in Partial power management state
0110	Interface in Slumber power management state
others	Reserved

- **Bit [07:04]**: SPD – This field identifies the negotiated interface communication speed.

Value	Definition
0000	No negotiated speed (reported if `phygood` false)
0001	Generation 1 communication rate (1.5 Gb/s) (reported if `phygood` true)
others	Reserved

- **Bit [03:00]**: DET – This field indicates the interface device detection and PHY state.

Value	Action
0000	No device detected and PHY communication not established (`phygood` false)
0001	Device presence detected but PHY communication not established (detected cominit but phygood not true)
0011	Device presence detected and PHY communication established (`phygood` true)
0100	PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode
others	Reserved, no action

Until a device is detected (IPM and DET fields become nonzero), the SiI3112A issues a COMRESET every 100 milliseconds.

6.7.47 Serial ATA Serror

Address Offset: 108_H (channel 0) / 188_H (channel 1)
Access Type: Read/Clear
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	R	R	R	R	R	**F**	**T**	**S**	**H**	**C**	**D**	**B**	**W**	**I**	**N**	R	R	R	R	**E**	**P**	**C**	**T**	R	R	R	R	R	R	**M**	**I**
DIAG																**ERR**															

This register is the SError register as defined by the Serial ATA specification (section 10.1.2).

- **Bit [31:16]**: DIAG – This field contains bits defined as shown in the following table. Writing a 1 to the register bit clears the B, C, F, N, H, and W bits.

Bit	Definition	Description
B	10b to 8b decode error	Latched decode error or disparity error from the Serial ATA PHY
C	CRC error	Latched CRC error from the Serial ATA PHY
D	Disparity error	N/A, always 0; this error condition is combined with the decode error and reported as B error
F	Unrecognized FIS type	Latched Unrecognized FIS error from the Serial ATA Link
I	PHY Internal error	N/A, always 0
N	PHYRDY change	Indicates a change in the status of the Serial ATA PHY
H	Handshake error	Latched Handshake error from the Serial ATA PHY
R	Reserved	Always 0
S	Link Sequence error	N/A, always 0
T	Transport state transition error	N/A, always 0
W	ComWake	Latched ComWake status from the Serial ATA PHY

Table 6-10 SError Register Bits (DIAG Field)

- **Bit [15:00]**: ERR – This field contains bits defined as shown in the following table. The ERR Field is not implemented; all bits are always 0.

Bit	Definition	Description
C	Non-recovered persistent Communication error or data integrity error	N/A, always 0
E	Internal Error	N/A, always 0
I	Recovered data Integrity error	N/A, always 0
M	Recovered communications error	N/A, always 0
P	Protocol error	N/A, always 0
R	Reserved	Always 0
T	Non-recovered Transient data integrity error	N/A, always 0

Table 6-11 SError Register Bits (ERR Field)

6.7.48 Serial ATA Sdevice

Address Offset: $10C_H$ (channel 0) / $18C_H$ (channel 1)
Access Type: Read Only
Reset Value: 0x????_????

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SDbits																															

This register contains the 32 Set Device bits from Dword 1 of the Set Device Bits FIS.

6.7.49 Smisc

Address Offset: 140_H (channel 0) / $1C0_H$ (channel 1)
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIS_Done	Transmit_FIS	Transmit_OK	IFIS_OK	IntrlckFIS	Reject_IF	Accept_IF	Rx_IFIS	SDB	Reserved	Scr_dis	Cont_dis	VS_Lock_Abort	Reserved			Transmit_BIST	Reserved			ComWake	Reserved				PMCHG	PMMODE		Reserved		PMREQ	

This register contains bits for controlling Serial ATA power management, ComWake, loopback modes, and FIS transfers.

- **Bit [31]**: FIS_Done (R)– This bit is used to indicate to the link logic that all the data for the Transparent FIS has been transferred and that the link can proceed to close out the FIS. This is used in Transparent FIS transmission. Please refer to the section “FIS Support” for more details
- **Bit [30]**: Transmit_FIS (R/W)– This bit is used to signal the link logic to start the process of transmitting a Transparent FIS. Please refer to the section on “FIS Support” for more details
- **Bit [29]**: Transmit_OK (R)– This bit is used in Tansparent FIS transmission. It is used by the link to signal to the host that the current Transparent FIS has been successfully transferred to the device, and that a R_OK has been received
- **Bit [28]**: IFIS_OK (R)– This bit is used in the reception of Interlocked FISes. This bit is set by the link logic to inform the host that the current Interlocked FIS has been successfully received with no errors.
- **Bit [27]**: IntrlckFIS (R)– This bit is set to indicate to the host driver that the link has detected an the arrival of an interlocked FIS and that the host should set up the DMA engine to start transfer of data
- **Bit [26]**: Reject_IFIS (W)– This bit is set by the host driver to indicate to the link that the current Interlocked FIS should be rejected. The link logic will respond to the device with an R_ERR when the complete FIS has been received.
- **Bit [25]**: Accept_IFIS (W)– This bit is set by the host driver to indicate to the link that the current interlocked FIS should be accepted. The link logic will respond to the device with R_OK
- **Bit [24]**: Rx_IFIS (R/W)– This bit is set by the host driver to inform the link/transport logic that the host has set up the DMA engine to transfer the incoming Interlocked FIS and that the DMA cycles can begin
- **Bit [23]**: SDB (R)– This bit indicates that a Set Device Bits FIS has been received
- **Bit [22]**: Reserved (R). This bit is reserved and returns zero on a read.
- **Bit [21]**: Scr_dis (R/W)– This bit disables the scrambling of data on the serial ATA bus. This is used only for debugging purposes and should not be changed by the user
- **Bit [20]**: Cont_dis (R/W)– Setting this bit disables the CONT primitive, i.e., the SiI3112 will always send the actual primitive instead of a CONT followed by random data.
- **Bit [19]**: VS_Lock_Abort (R/W)– This bit controls the changes to the entries in the Command Protocol Table upon receiving a VS_Lock command. If this bit is set, all Command Protocol Table will be cleared. If this bit is not set, the Command Protocol Table will not be cleared in the VS_Lock state.
- **Bit [18:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [15]**: Reserved (R). Always write 0 to the bit.
- **Bit [14:12]**: Reserved (R). This bit field is reserved and returns zero on a read.
- **Bit [11]**: ComWake (R/W)– Setting this bit (to 1) asserts ComWake on the Serial ATA bus.
- **Bit [10:07]**: Reserved (R). This bit field is reserved and returns zeros on a read.

- **Bit [6]**: PMCHG (R/W)– This bit reports a change in the Power Management mode. This bit corresponds to the interrupt enabled by bit 26 of SIEN. This bit is cleared by writing a 1.
- **Bit [05:04]**: PMMODE (R/W)– These bits report the power management mode status: bit 5 corresponds to Slumber mode, bit 4 to Partial mode. A transition on either of these bits causes a Power Management mode change interrupt.
- **Bit [03:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: PMREQ (R/W)– These bits initiate power management requests: setting bit 1 will send a slumber mode request `pmreq_s to the device`; setting bit 0 will send a Partial mode request `pmreq_p` to the device

6.7.50 Serial ATA PHY Configuration

Address Offset: 144_H
Access Type: Read/Write
Reset Value: 0x0000_80F1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										Bypass OOB	Reserved	Tx_Swing_1	Reserved				Tx_Swing_0	Reserved													

The PHY Configuration register is auto-initialized from external Flash or EEPROM. The bit definitions are as follows:

- **Bit[31:22]**: Reserved. The values of these bits should not be changed from their defaults otherwise erratic operation may result
- **Bit[21]**: Bypass OOB sequence. If the bit set to 1, all channel Tx outputs random pattern data.
- **Bit[20]**: Reserved. The value of this bits should not be changed from their defaults otherwise erratic operation may result
- **Bit[19]**: Tx_Swing_1: This bit, together with Tx_Swing_0, sets the nominal output amplitude for the Transmitter
- **Bit[18:14]**: Reserved. The values of these bits should not be changed from their defaults otherwise erratic operation may result
- **Bit[13]**: Tx_Swing_0: This bit, together with Tx_Swing_1, sets the nominal output swing for the Transmitter. The available combinations are as follows:

Tx_Swing_1	Tx_Swing_0	Nominal Output Swing
0	0	500mV
0	1	600mV
1	0	700mV
1	1	800mV

- **Bit[12:0]**: Reserved. The values of these bits should not be changed from their defaults otherwise erratic operation may result.

6.7.51 SIEN

Address Offset: 148_H (channel 0) / $1C8_H$ (channel 1)
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved		Transmit_OK	IFIS_OK	IntrickFIS	PMCHG	F	Reserved	SDB	H	C	Reserved	B	W	Reserved	N	Reserved															

This register contains bits for enabling interrupts.

- **Bit [31:30]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [29]**: Transmit_OK – This bit enables an interrupt upon the assertion of the Transmit_OK bit in the SMisc register.
- **Bit [28]**: IFIS_OK – This bit enables an interrupt upon the assertion of the IFIS_OK bit in the SMisc register.
- **Bit [27]**: IntrlckFIS – This bit enables an interrupt upon the assertion of the IntrlckFIS bit in the SMisc register.
- **Bit [26]**: PMCHG – This bit enables an interrupt upon a Power Management Mode change. The interrupt is reported in bit 6 of SMisc.
- **Bit [25]**: F – This bit enables an interrupt upon the assertion of the F bit in the DIAG field of the SError register.
- **Bit [24]**: Reserved (R). This bit is reserved and returns zero on a read.
- **Bit [23]**: SDB – This bit enables an interrupt upon the assertion of the SDB bit in the SMisc register.
- **Bit [22]**: H – This bit enables an interrupt upon the assertion of the H bit in the DIAG field of the SError register.
- **Bit [21]**: C – This bit enables an interrupt upon the assertion of the C bit in the DIAG field of the SError register.
- **Bit [20]**: Reserved (R). This bit is reserved and returns zero on a read.
- **Bit [19]**: B – This bit enables an interrupt upon the assertion of the B bit in the DIAG field of the SError register.
- **Bit [18]**: W – This bit enables an interrupt upon the assertion of the W bit in the DIAG field of the SError register.
- **Bit [17]**: Reserved (R). This bit is reserved and returns zeros on a read.
- **Bit [16]**: N – This bit enables an interrupt upon the assertion of the N bit in the DIAG field of the SError register.
- **Bit [15:00]**: Reserved (R). This bit field is reserved and returns zeros on a read.

6.7.52 SFISCfg

Address Offset: $14C_H$ (channel 0) / $1CC_H$ (channel 1)
Access Type: Read/Write
Reset Value: 0x1040_1555

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved		FIS27cfg		FIS34cfg		FIS39cfg		FIS41cfg		FIS46cfg		FIS58cfg		FIS5Fcfg		FISA1cfg		FISA6cfg		FISB8cfg		FISBFcfg		FISC7cfg		FISD4cfg		FISD9cfg		FISOcfg	

This register contains bits for controlling Serial ATA FIS reception. See the section on FIS Support for explanation of the configuration bits.

6.7.53 RxFIS0-RxFIS6

Address Offset: 160_H-178_H (channel 0) / $1E0_H$-$1F8_H$ (channel 1)
Access Type: Read
Reset Value: 0x????_????

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FIS Dword																															

These registers contain 7 Dwords from a Serial ATA FIS reception.

7 Programming Sequences

7.1 Recommended Initialization Sequence for the Sil3112A

The recommended initialization sequence for the SiI3112A is detailed below.

Initialize PCI Configuration Space registers

- Initialize Base Address Register 0 with the address of an 8-byte range in I/O space.
- Initialize Base Address Register 1 with the address of a 4-byte range in I/O space.
- Initialize Base Address Register 2 with the address of an 8-byte range in I/O space.
- Initialize Base Address Register 3 with the address of a 4-byte range in I/O space.
- Initialize Base Address Register 4 with the address of a 16-byte range in I/O space.
- Initialize Base Address Register 5 with the address of a 512-byte range in memory space.
- To enable the bios expansion ROM, initialize the Expansion ROM Base Address Register with the address of a 512KB range in memory space.
- Enable I/O space access, memory space access, and bus master operation by setting bits [2:0] of the PCI Command register.

NOTE: The preceding configuration space register initialization is normally done by the motherboard BIOS in PC type systems.

If the PCI-IDE arbiter's default FIFO read/write request thresholds are not suitable for the application they may be changed via the FIFO Valid Byte Count and Control IDEx register. The read threshold is defined by bits [05:00], and the write threshold is defined by bits [13:08] in the FIFO Valid Byte Count and Control – IDEx register. In most environments, setting these bit fields to zero results in the best utilization of the PCI bus by the SiI3112A controller.

If interrupt driven operation is **not** desired, set bits [23:22] of the System Configuration Status and Command register to block IDE interrupts from reaching the PCI bus.

7.2 Serial ATA Device Initialization

This section provides a general overview of the steps necessary to initialize a Serial ATA device before it can be used for read/write operations.

Select the Serial ATA device. The device is selected by programming bits [23:16] in the IDEx Task File Register 1 register.

If interrupt driven operation is desired, ensure that IDE interrupts are enabled by writing 0 to bits [23:16] of the IDEx Task File Register 2 register.

For ATA devices only:

Issue the Initialize Device Parameters command by

- Programming bits [23:16] in the IDEx Task File 0 register with the number of logical sectors per logical track.
- Programming bits [23:16] in the IDEx Task File 1 register with the maximum head number.
- Programming bits [31:24] in the IDEx Task File Register 1 register with the value = 91_H.
- Wait for the command to complete. This can be accomplished by waiting for an interrupt if interrupts have been enabled at both the controller and the device. If interrupts are not enabled, command completion can be detected by polling bits [31:24] of the IDEx Task File Register 1 register until the BUSY bit is no longer asserted.

If device supports read/write multiple commands, issue the Set Multiple Mode command by:

- Programming bits [23:16] in the IDEx Task File 0 register with the number of sectors per block to use on the following Read/Write Multiple commands.
- Programming bits [31:24] in the IDEx Task File Register 1 register with the value = $C6_H$.
- Wait for the command to complete (see above).

For both ATA and ATAPI devices:

Set device transfer mode by:

- Programming bits [15:08] in the IDEx Task File 0 register with the value 03_H to "Set the transfer mode based on value in Sector Count Register".
- Programming bits [23:16] in the IDEx Task File 0 register to the desired transfer mode. The settings are defined below:

  08_H = PIO Mode 0
  09_H = PIO Mode 1
  $0A_H$ = PIO Mode 2
  $0B_H$ = PIO Mode 3
  $0C_H$ = PIO Mode 4
  20_H = Multiword DMA Mode 0
  21_H = Multiword DMA Mode 1
  22_H = Multiword DMA Mode 2
  40_H = Ultra DMA Mode 0
  41_H = Ultra DMA Mode 1
  42_H = Ultra DMA Mode 2
  43_H = Ultra DMA Mode 3
  44_H = Ultra DMA Mode 4
  45_H = Ultra DMA Mode 5
  46_H = Ultra DMA Mode 6

- Programming bits [31:24] in the IDEx Task File Register 1 register with the value = EF_H.
- Wait for the command to complete (see above).

In order to use the controller's DMA capability to perform the data transfer for an ATA/ATAPI command, the controller needs to be configured for the transfer mode to use when transferring data to or from the ATA bus. The data transfer mode is set by programming bits [1:0] of the IDEx Data Transfer Mode register. The transfer mode select values are listed below::

00_B = PIO/Virtual DMA Mode
10_B = DMA Mode

7.3 Issue ATA Command

The following describes the sequence to issue a read/write type command to an ATA device.

Select the IDE device. The IDE device is selected by programming bits [23:16] in the IDEx Task File Register 1 register.

Set the number of sectors to be transferred by programming bits [23:16] of the IDEx Task File Register 0 register.

Set the location of data to be transferred. The location is defined by programming the following.
Bits [31:24] in the IDEx Task File Register 0 register define the Starting Sector.
Bits [23:16] in the IDEx Task File Register 1 register define the Device and Head value.
Bits [15:08] in the IDEx Task File Register 1 register define the Cylinder High value.
Bits [07:00] in the IDEx Task File Register 1 register define the Cylinder Low value.

Issue the Read/Write PIO/DMA command by programming bits [31:24] in the IDEx Task File Register 1 register with the command desired.

7.4 IDE PIO Mode Read/Write Operation

Once the SiI3112A is initialized via the initialization sequence described above, the ATA device has been initialized for PIO mode data transfer per the guidelines in section 7.2, and the controller channel has been initialized for PIO mode data transfer , PIO read/write operations may be performed by following the programming sequence described below.

Issue a PIO Read/Write command to device following the steps in section 7.3.

Read Operation

Wait until an IDE channel interrupt (bit 11 in the IDEx Task File Timing + Configuration + Status register is set).

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was error.

If no error, continue to read IDE data via the IDEx Task File Register 0 register, until the expected number of sectors of data per interrupt are read.

Repeat the above three steps until all data for the read command has been transferred or an error has been detected.

Write Operation

Wait until bit 27(DRQ) in the IDEx Task File Register 1 register is set.

Continue to write IDE data via the IDEx Task File Register 0 register until the expected number of sectors of data per interrupt are written.

Wait until an IDE channel interrupt (bit 11 in the IDEx Task File Timing + Configuration + Status register is set).

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was error.

If no error, repeat the previous four steps until all data for the write command has been transferred or an error has been detected.

7.5 Watchdog Timer Operation

The purpose of the watchdog timer is to prevent the host system from hanging because a device operating in PIO mode stopped responding to task file accesses. If, during a task file access by the host, the device negates IORDY and then stops responding, the host will hang waiting for the access to complete. It is this type of hang, that the watchdog timer is designed to protect against.

The watchdog timer monitors the length of time the IORDY signal is negated. If the watchdog timer detects that the the IORDY signal has remained negated longer than the watchdog timeout period (approximately 7.75us), the watchdog timer will force the task file access cycle to complete, and set the watchdog timeout bit in the IDEx Task File Timing + Configuration + Status register. The data associated with a timed out access should be considered invalid. Additionally, the watchdog timer can be configured to generate an interrupt when a timeout is detected by setting bit 14 of the IDEx Task File Timing + Configuration + Status register.

The watchdog timer feature is disabled by default.

In addition to the controller channel initialization specified previously, add the following two steps to enable the watchdog timer:

Enable the watchdog timer by setting bit 13 of the IDEx Task File Timing + Config + Status register.

If an interrupt is desired whenever the watchdog times out, enable the watchdog interrupt by setting bit 14 of the IDEx Task File Timing + Config + Status register.

The following programming sequences are needed for each PIO Mode Read/Write Operation with the watchdog timer enabled:

Issue a Read/Write PIO Command to the ATA drive following the steps in section 7.3.

Read Operation

Wait for an IDE channel interrupt.

If controller interrupts are disabled, poll for the IDE interrupt by reading the IDEx Task File Timing + Configuration + Status register. If bit 12 is set, a watchdog timeout has occurred. If bit 11 is set, the ATA device is interrupting.

If the watchdog timeout bit is set,

Write 1 to bit 12 in the IDEx Task File Timing + Configuration + Status register to clear watchdog timeout status.

The watchdog timeout represents a fatal error as far as the current ATA command is concerned. A course of action that might be appropriate at this point might be to reset and reinitialize the ATA channel and then retrying the command that failed.

If the ATA device interrupt bit is set,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx Register to clear the ATA interrupt.

If the ATA device is not reporting an error, continue to read IDE data via the IDEx Task File Register 0 register, until the expected number of sectors of data per interrupt are read.

Repeat the read operation steps until all data for the read command has been transferred or an error has been detected.

Write Operation

Wait until bit 27(DRQ) in the IDEx Task File Register 1 register is set.

Continue to write IDE data via the IDEx Task File Register 0 register until the expected number of sectors of data per interrupt are written.

Wait for an IDE channel interrupt.

If controller interrupts are disabled, poll for the IDE interrupt by reading the IDEx Task File Timing + Configuration + Status register. If bit 12 is set, a watchdog timeout has occurred. If bit 11 is set, the ATA device is interrupting.

If the watchdog timeout bit is set,

Write 1 to bit 12 in the IDEx Task File Timing + Configuration + Status register to clear watchdog timeout status.

The watchdog timeout represents a fatal error as far as the current ATA command is concerned. A course of action that might be appropriate at this point might be to reset and reinitialize the ATA channel and then retrying the command that failed.

If the ATA device interrupt bit is set,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx Register to clear the ATA interrupt.

If no error, repeat the write operation steps until all data for the write command has been transferred or an error has been detected.

7.6 IDE PIO Mode Read Ahead Operation

Read ahead operation allows the controller to “pre-fetch” data from the IDE bus and store it in the controller’s channel FIFO, where it will later be retrieved by the host. This mode of operation has the potential to speed-up PIO data transfers by not

forcing the host to wait the programmed PIO cycle time for every access to the task file data register. The amount of any speed increase will depend on the PIO mode in use, the characteristics of the host PCI bus, as well as the speed of the host processor.

To use the controller's PIO read ahead capability, make the following changes to the "Read Operation" portion of sections 7.4and 7.5.

Just prior to retrieving the read data, set the read ahead byte count by programming bits [15:00] in the IDEx Virtual DMA/PIO Read Ahead Byte Count register with the exact number of bytes to be read for the interrupt.

Instead of reading the IDEx Task File Register 0 register to retrieve the data, read the IDEx Read Ahead Data register instead.

7.7 IDE MDMA/UDMA Read/Write Operation

Once the SiI3112A is initialized via the initialization sequence described in Section 7.1 and the ATA device has been initialized for MDMA/UDMA mode data transfer per the guidelines in section 7.2, DMA read/write operations may be performed by following the programming sequence described below.

Issue a DMA read/write command to the device following steps in section 7.3.

Program Bus Master Registers

Clear bit 17 in the PCI Bus Master – IDEx register. This bit is set if an error occurred during the previous DMA access.
Clear bit 18 in the PCI Bus Master – IDEx register. This bit is set if an IDE interrupt occurred during the previous DMA access.

Create a Physical Region Descriptor (PRD) Table.
A PRD table is an array where each entry describes the location and size of a physical memory buffer that will be used during the DMA operation. Each PRD table entry is 64-bits in length, formatted as follows; bits [31:0] contain the 32-bit starting address of the memory buffer, bits [47:32] contain the 16-bit size of the memory buffer, bits [62:48] are normally unused (see section 8.10 for details of how these bits may be used), bit 63 flags the end of the PRD table and therefore should only be set in the last entry of the PRD table. The PRD table itself must be constructed in a memory region that can be directly accessed by the SiI3112A controller. Once the PRD table is built, the controller must be informed of its location. This is accomplished by writing the 32-bit address of the PRD table to the PRD Table Address – IDEx register.

Enable DMA transfer.
DMA is enabled by writing bits [7:0] of the PCI Bus Master – IDEx register. Bit 3 of this register controls the direction of the DMA transfer; 1 = write to memory, 0 = read from memory. Setting bit 0 of the register enables the controller to perform DMA operations.
Note: Task file registers are inaccessible as long as bit 0 is set.

Wait for a PCI interrupt.

When a PCI interrupt occurs, read the PCI Master – IDEx status register and check the DMA status bits. The possible combinations of the status bits [18:16] are defined below.

000_B = If the IDE device does not report an error, then the PRD table specified a size that is smaller than the IDE transfer size.

001_B = DMA transfer in progress.

010_B = The controller had a problem transferring data to/from memory.

100_B = Normal completion.

101_B = If the IDE device does not report an error, then the PRD specified a size that is larger than the IDE transfer size.

Make sure PCI bus master operation of the SiI3112A is stopped by clearing bit 0 of the PCI Bus Master – IDEx register.
Note: The task file registers are not accessible as long as bit 0 is set. Clearing bit 0 causes bit 16 to be cleared as well.

Read the device status at bits [13:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was error.

Write '1' to bit 18 (write-one-to-clear) in the PCI Bus Master – IDEx register to clear the PCI Interrupt.

7.8 IDE Virtual DMA Read/Write Operation

In virtual DMA operation the controller uses a PIO data transfer mode to move data between an ATA/ATAPI device and the controller, and uses DMA to move that same data between the controller and the host memory. For ATA/ATAPI devices that cannot operate in a "true" DMA mode, virtual DMA provides two benefits; first, using DMA to move data reduces the demand on the host CPU, and second, systems that use virtual memory often require that data buffers that will be accessed directly by low level device drivers be "mapped" into the operating system's address space, in virtual DMA mode the CPU does not access the data buffer directly, so the overhead of obtaining the mapping to operating system address space is eliminated.

7.8.1 Using Virtual DMA with Non-DMA Capable Devices

Once the SiI3112A is initialized via the initialization sequence described in Section 7.1 and the ATA device has been initialized for PIO mode data transfer per the guidelines in section 7.2, virtual DMA read/write operations may be performed by following the programming sequence described below.

NOTE: The watchdog timer feature is compatible with virtual DMA operation. See section 7.5 for details about using the watchdog timer.

Issue a PIO read/write command to the device following steps in section 7.3.

Read Operation

Wait for a PCI interrupt.

Read the DMA status bits [18:16] of the PCI Bus Master – IDEx register, and check that bit 18 is set to make sure the interrupt was generated by the expected channel.

If expected channel interrupted, read bits [11:10] of the channel's IDEx Task File Timing + Configuration + Status register to determine the cause of the interrupt. Bit 11 is set if the ATA/ATAPI device has an interrupt pending, bit 10 is set if a virtual DMA operation completed.

If a virtual DMA operation completed,

Write 00_H to bits [7:0] of the PCI Bus Master – IDEx register to disable DMA operation.

Write 1 to bits [18:17] of the PCI Bus Master –IDEx register to reset the DMA status and virtual DMA interrupt bits, and the PCI interrupt.

Check the previously read DMA status bits to ensure the DMA completed successfully.
Because ATA/ATAPI commands that transfer data using PIO can generate several interrupts during the data transfer phase of the command, a race condition is created between the interrupt indicating the completion of a virtual DMA operation, and the interrupt from the ATA/ATAPI device indicating it is ready to perform the next part of the data transfer. To prevent missing an ATA/ATAPI device interrupt due to this race condition, it is necessary to re-read the channel's IDEx Task File Timing + Configuration + Status register after disabling DMA operation and examining bit 11. If bit 11 is set, the ATA/ATAPI device is interrupting and should be serviced by following the steps below (assuming that the virtual DMA operation completed successfully).

If the ATA/ATAPI device has interrupted,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx register to clear the DMA Complete bit (NOTE: The DMA Complete bit acts as a latched copy of the ATA interrupt line when the channel is not performing a DMA operation).

If the ATA/ATAPI device is not reporting an error, and DRQ is asserted (bit 27 of IDEx Task File Register 1), then the device is interrupting to transfer data to the host. To transfer the data, the DMA registers are setup to only perform that part of the data transfer expected for this interrupt. The DMA is setup similarly to the way it is when performing a normal read DMA command, but with

one additional step. Before the DMA is enabled, the IDEx Virtual DMA/PIO Read Ahead Byte Count register must be written with the 32-bit count of the number of bytes to be transferred for this interrupt.

Repeat the above steps until all data for the read command has been transferred or an error has been detected.

Write Operation

Poll the IDEx Task File Register 1 bits [31:24] until either bit 27 (DRQ) is set indicating the device is ready for write data transfer, or bit 24 (ERR) is set indicating the device has detected an error with the write command.

If no error, and DRQ is asserted (bit 27 of IDEx Task File Register 1), then the device is waiting for write data transfer. To transfer the data, the DMA registers are setup to only perform that part of the data transfer expected at this time. For example, a Write Sectors command would expect to transfer 1 sector (512 bytes), while a Write Multiple command would expect to transfer the lesser of the number of sectors set by the Set Multiple Mode command or the total number of sectors specified by the Write Multiple command. The DMA is setup similarly to the way it is when performing a normal write DMA command, but with one additional step. Before the DMA is enabled, the IDEx Virtual DMA/PIO Read Ahead Byte Count register must be written with the 32-bit count of the number of bytes to be transferred.

Wait for a PCI interrupt.

Read the DMA status bits [18:16] of the PCI Bus Master – IDEx register, and check that bit 18 is set to make sure the interrupt was generated by the expected channel.

If expected channel interrupted, read bits [11:10] of the channel's IDEx Task File Timing + Configuration + Status register to determine the cause of the interrupt. Bit 11 is set if the ATA/ATAPI device has an interrupt pending, bit 10 is set if a virtual DMA operation completed.

If a virtual DMA operation completed,

Write 00_H to bits [7:0] of the PCI Bus Master – IDEx register to disable DMA operation.

Write 1 to bits [18:17] of the PCI Bus Master –IDEx register to reset the DMA status and virtual DMA interrupt bits, and PCI interrupt.

Check the previously read DMA status bits to ensure the DMA completed successfully.
Because ATA/ATAPI commands that transfer data using PIO can generate several interrupts during the data transfer phase of the command, a race condition is created between the interrupt indicating the completion of a virtual DMA operation, and the interrupt from the ATA/ATAPI device indicating it is ready to perform the next part of the data transfer. To prevent missing an ATA/ATAPI device interrupt due to this race condition, it is necessary to re-read the channel's IDEx Task File Timing + Configuration + Status register after disabling DMA operation and examining bit 11. If bit 11 is set, the ATA/ATAPI device is interrupting and should be serviced by following the steps below (assuming that the virtual DMA operation completed successfully).

If the ATA/ATAPI device has interrupted,

Read the device status at bits [31:24] in the IDEx Task File Register 1 register to clear the device interrupt and determine if there was an error.

Write 1 to bit 18 of the PCI Bus Master – IDEx register to clear the DMA Complete bit (NOTE: The DMA Complete bit acts as a latched copy of the ATA interrupt line when the channel is not performing a DMA operation).

If the ATA/ATAPI device is not reporting an error, and DRQ is asserted (bit 27 of IDEx Task File Register 1), then the device is interrupting to transfer data to the device. To transfer the data, the DMA registers are setup to only perform that part of the data transfer expected for this interrupt. The DMA is setup similarly to the way it is when performing a normal write DMA command, but with one additional step. Before the DMA is enabled, the IDEx Virtual DMA/PIO Read Ahead Byte Count register must be written with the 32-bit count of the number of bytes to be transferred for this interrupt.

Repeat the above steps starting at “Wait for PCI interrupt” until all data for the write command has been transferred or an error has been detected.

7.8.2 Using Virtual DMA with DMA Capable Devices

Even though a device may be DMA capable, there are ATA/ATAPI commands that require that a PIO mode be used to transfer data. For these commands, virtual DMA can be used to perform the data transfer. Using virtual DMA with an ATA/ATAPI device that has already been configured to use DMA for normal read/write operation is performed very much like the sequence described above for PIO mode only devices, but with the following additional consideration:

- The Data Transfer Mode – IDEx register associated with the ATA/ATAPI device needs to be programmed for a PIO type transfer mode **before** DMA operation is enabled, and must be re-programmed with the DMA/UDMA transfer type used during normal DMA operation once the virtual DMA operation is complete.

7.9 Second PCI Bus Master Registers Usage

In order to provide backward compatibility with existing drivers, the Physical Region Descriptor (PRD) tables used by the SiI3112A controller when performing DMA transfers suffer the following limitations; a PRD table entry cannot represent a memory area greater than 64k, nor can a PRD table entry represent a memory area that spans a 64k address boundary. Whenever DMA is initiated via the PCI Bus Master – IDEx registers, the foregoing limitations are enforced by the SiI3112A controller.

A feature known as Large Block Transfer in the SiI3112A controller allows drivers to get around the 64k size and address limits of PRD table entries expected by existing drivers. Large Block Transfer simplifies the creation of PRD tables by reducing the number of table entries that need to be created and eliminating the need to make sure a memory region does not cross a 64k boundary. Large Block Transfer mode is enabled whenever DMA is initiated by writing to the PCI Bus Master 2 – IDEx registers (base address 5, offset 10_H or 18_H). When performing DMA in Large Block Transfer mode, the SiI3112A controller interprets the fields of a PRD table entry differently. In all other respects, DMA interrupt generation, DMA status bit interpretation, etc., Large Block Transfer mode behaves identically to a non-Large Block Transfer mode DMA operation. The following table describes the format of a PRD table entry:

Bits 31:0	32-bit starting address of the memory region.
Bits 47:32	When not operating in Large Block Transfer mode, this field specifies the size of the memory region. If the size of the memory region is greater than 64k, or crosses a 64k address boundary, then two or more PRD table entries will need to be created to describe it. If operating in Large Block Transfer mode, this field contains the least significant 16-bits of the size of the memory region.
Bits 62:48	If not operating in Large Block Transfer mode, this field is unused. If operating in Large Block Transfer mode, this field contains the most significant 15-bits of the size of the memory region.
Bit 63	When set, this bit indicates that this is the last entry in the PRD table.

Table 7-1 Physical Region Descriptor (PRD) Format

8 Power Management

Power Management in the SiI3112A is controlled by the following register bits.

Register	Bits	Description
SMisc	PMCHG Bit 6	This bit reports a change in the Power Management mode. It corresponds to the interrupt enabled by bit 26 of SIEN.
SMisc	PMMODE Bits 5,4	These bits report the power management mode status: bit 5 corresponds to Slumber mode; bit 4 to Partial mode. A transition on either of these bits causes a Power Management mode change interrupt.
SError	W Bit 18	ComWake received from the Serial ATA bus
SMisc	ComWake Bit 11	Generates a ComWake condition on the Serial ATA bus
SMisc	PMREQ Bits 1,0	Generates a request from the Host for the Device to go to a Power Management state; bit 1 corresponds to Slumber mode; bit 0 corresponds to Partial mode. These bits are effective regardless of the state of the HPMDS bit.
SControl	IPM Bits 11-8	This bit field disables transitions to Partial or Slumber power management states; bit 9 corresponds to Slumber mode; bit 8 corresponds to Partial mode.
SStatus	IPM Bits 11-8	This bit field reports the power management state; '0110' corresponds to Slumber mode; '0010' corresponds to Partial mode.

Table 8-1 Power Management Register Bits

8.1 Power Management Summary

There are two power management modes: Partial and Slumber. These power management modes may be software initiated through the SMisc register or device initiated from the Serial ATA device.
Transitions to and from either power management mode generate an interrupt, the Power Management Mode Change Interrupt, which may be masked in the SIEN register (bit 26).

8.2 Partial Power Management Mode

Partial mode may be initiated by software through the SMisc register (bit 0). By setting the bit, the software causes PMREQ_P primitives (Power Management REQuest – Partial) to be sent to the Serial ATA device, which will respond with either a PMACK or PMNAK. If a PMACK is received the Partial mode is entered; A PMNAK is ignored; the request remains asserted.
The Serial ATA device may initiate partial mode. This is indicated by the reception of PMREQ_P primitives from the device. Software enables the acknowledgement of this request by setting the IPM value in the SControl register to '00x1' If enabled, a PMACK will be sent to the device; if not enabled, a PMNAK will be sent. When the request is received and its acknowledgement is enabled, Partial mode is entered.
Partial mode status is reported in both the SStatus register ('0010' in the IPM field) and the SMisc register (bit 4).
Partial mode is cleared by setting the ComWake bit in the Smisc register. This will send a COMWAKE signal to the device through the Serial ATA link to initiate a Partial to On sequence. Partial mode can also be cleared through receipt of OOB signals from the device.

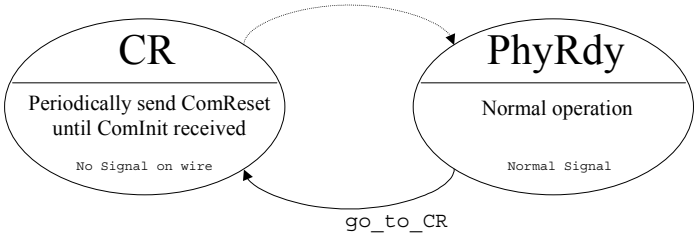
8.3 Slumber Power Management Mode

Slumber mode may be initiated by software through the SMisc register (bit 1). By setting the bit, software causes PMREQ_S primitives to be sent to the Serial ATA device, which will respond with either a PMACK or PMNAK. If a PMACK is received the Slumber mode is entered. A PMNAK is ignored; the request remains asserted.
The Serial ATA device may initiate slumber mode. This is indicated by the reception of PMREQ_S primitives. Software enables the acknowledgement of this request by setting the IPM value in the SControl register to '001x'. If enabled, a PMACK will be sent to the device; if not enabled, a PMNAK will be sent. When the request is received and its acknowledgement is enabled, Slumber mode is entered.
Slumber mode status is reported in both the SStatus register ('0110' in the IPM field) and the SMisc register (bit 5).

Slumber mode is cleared by setting the ComWake bit in the Smisc register. This will send a COMWAKE signal to the device through the Serial ATA link to initiate a Slumber to On sequence. Slumber mode can also be cleared through receipt of OOB signals from the device.

8.4 Hot Plug Support

The state diagram below illustrates the logic to support Hot Plugging.



The `go_to_CR` signal is generated by a timer if the internal logic fails to detect valid signals from the Serial ATA wire for 200 ns. Logic behavior is as follows:

1. Initial power-up – A ComReset is generated during initial power up. If a device is present and operational, the PhyRdy state will be entered. If a device is not present or not responding, the CR state will be entered and ComReset will be generated every 100 ms.
2. Device is unplugged – The internal logic detects that no more signal is present on the Serial ATA wire. The timer will expire after 200 ns and `go_to_CR` will be asserted; the CR state will be entered and ComReset will be generated every 100 ms. The internal PHYRDY signal will go false causing an interrupt to the host driver (PHYRDY change interrupt, bit 16 of SError register; enabled by bit 16 of SIEN register).
3. Device is plugged in – The device will respond to the ComReset with a ComInit. Normal operation will commence and the internal logic will detect a PHYRDY signal going true causing an interrupt to the host driver (PHYRDY change interrupt, bit 16 of SError register; enabled by bit 16 of SIEN register).

9 FIS Support

This section describes the implementation of Serial ATA FIS support.

9.1 FIS Summary

The following table summarizes the implementation of FIS Support. Note that 14 FIS codes meet the criteria of FIS code selection in Serial ATA, and eight out of the 14 are already defined.

Table 9-1 FIS Summary

FIS Code	FIS Name	Host to Device	Device to Host	Comment
27h	Register (Host to Device)	√		• Support Expanded Registers • HOB not sent to device (device bridge ignores HOB received) • Can be individually controlled via PCI registers - default to reject
34h	Register (Device to Host)		√	• Support Expanded Registers • Host to Device transmission is possible as Transparent. • Can be individually controlled via PCI registers - default to accept
39h	DMA Activate		√	• Supported per Serial ATA specification. • Host to Device transmission is possible as Transparent. • Can be individually controlled via PCI registers - default to accept
41h	DMA Setup	√	√	• On reception, the first 7 Dwords of any FIS can be read direcly by the PCI. • Transmission: As transparent FIS • Can be individually controlled via PCI registers - default to reject
46h	Data	√	√	• Supported per Serial ATA specification. • Can be individually controlled via PCI registers - default to accept
58h	BIST Activate	√	√	• Support for reception of Far-End Retimed Loopback. No transmission supported. • Can be individually controlled via PCI registers - default to accept for Far-End Retimed Loopback; default to reject for all other BIST types
5Fh	PIO Setup		√	• Supported per Serial ATA specification. • Host to Device transmission is possible as Transparent. • Can be individually controlled via PCI registers - default to accept
A1h	Set Device Bits		√	• Supported per Serial ATA specification • Host to Device transmission is possible as Transparent • Can be individually controlled via PCI registers - default to accept

Table 9-1 FIS Summary

FIS Code	FIS Name	Host to Device	Device to Host	Comment
A6h	reserved	TBD	TBD	• Supported as one group of unrecognized FIS, together with other unsupported FISes, such as "Others" below, and FIS Code 27h in the reception direction. • Can be individually controlled via PCI registers - default to reject
B8h	reserved	TBD	TBD	
BFh	reserved	TBD	TBD	
C7h	reserved	TBD	TBD	
D4h	reserved	TBD	TBD	
D9h	reserved	TBD	TBD	
Others	reserved	TBD	TBD	• Supported as one group of unrecognized FIS, together with other unsupported FISes (FIS Code 27h, A6h, B8h, BFh, C7h, D4h, D9h) in the reception direction. • All "Others" are controlled as a group via PCI registers - default to reject

9.2 FIS Transmission

There are two ways in which a FIS transmission is initiated:

- Protocol-initiated FIS transmission, e.g., when an ATA command is written to the SiI3112A it will send a Command Register FIS and expects some FIS(es) (e.g., PIO Setup, Register, DMA Activate, Data, Set Device Bits).
- Transparent FIS transmission

  FISes that are not protocol initiated can also be transmitted as Transparenet FISes, under the control of the host driver.
  - Sequence:
    - Host sets the Transmit_FIS bit in the Smisc register (bit 30).This tells the Transport/Link logic that a transparent FIS needs to be transmitted.
    - The Transport/Link logic responds by setting itself up to transfer data from the host through UMDA cycles.
    - The host writes the data through the PCI interface. Note that the FIS header (Dword 0 that contains the FIS type) must also be written. The Transport/Link logic sends the FIS to the device. Note that:
      - All data to be transferred in this FIS must be sent within one UDMA burst. Burst termination will not be allowed and may produce unpredictable result.
      - There must be an even number of words.
      - The size of the FIS, including the header, must not exceed the maximum number of words specified for DMA frame size. This is important because the FIS header information will be lost when sent.
      - As in Data FIS, upon a transmission error, no retries can be supported. The PCI block must restart the transparent FIS transmission from the beginning.
      - Serial ATA CRC is calculated by the Transport/Link logic. The host will NOT append the CRC at the end.
    - After the last write, the host sets the FIS_Done bit in the Smisc register (bit 31). This indicates to the link that all data for this transaction has been transferred. The Transport/Link logic will then close out the FIS by appending CRC and EOF and wait for termination. If R_OK is received from the downstream device, the Transmit_OK bit will be set to indicate to the host that the FIS has been successfully transferred to the device. If there is an error in the transmission process (e.g., the FIS not recognized by the downstream device) resulting in the device acknowledging the FIS with an R_ERR, the F bit of the Serror Register will be set (Bit 25).
    - The values of the status registers are latched and will not be cleared automatically. Before the next Transparent FIS is being sent, the host must clear the status bits by performing a write to the particular status registers.

9.3 FIS Reception

The SiI3112A is capable of receiving Unrecognized FIS types through an Interlocked FIS scheme. This capability is over and above the regular protocol related FISes as defined in the Serial ATA specifications.
In general, an internal table determines the behavior when receiving all possible FIS types. This table is defined in the register SFISCfg. The configuration codes in the SFISCfg register is defined as follows:

Table 9-2 Configuration Bits for FIS Reception

FISxxCFG[1:0]	Comments
00b	Accept FIS without interlock. If there is no error detected for the entire FIS, R_OK will be sent after EOF is received. If any error is received, R_ERR will be sent after EOF
01b	Reject FIS without interlock. R_ERR will be sent
10b	Interlock. This allows the host to examine the first Dwords of the FIS to determine whether to accept or reject the FIS
11b	reserved.

The following table shows the default configurations of all Serial ATA FIS types:

Table 9-3 Default FIS Configurations

FIS Code	FIS Name	Configuration Bits		Comments
		Register Bits	Default Value	
27h	Register (Host to Device)	FIS27cfg[1:0]	01b	Default to reject FIS without interlock.
34h	Register (Device to Host)	FIS34cfg[1:0]	00b	Default to accept FIS without interlock.
39h	DMA Activate	FIS39cfg[1:0]	00b	Default to accept FIS without interlock.
41h	DMA Setup	FIS41cfg[1:0]	01b	Default to reject.
46h	Data	FIS46cfg[1:0]	00b	Default to accept FIS without interlock.
58h	BIST Activate	FIS58cfg[1:0]	00b	Default to accept for far-end retimed loopback, reject for any other.
5Fh	PIO Setup	FIS5Fcfg[1:0]	00b	Default to accept FIS without interlock.
A1h	Set Device Bits	FISa1cfg[1:0]	00b	Default to accept FIS without interlock.
A6h	reserved	FISa6cfg[1:0]	01b	Default to reject FIS without interlock.
B8h	reserved	FISb8cfg[1:0]	01b	Default to reject FIS without interlock.
BFh	reserved	FISbFcfg[1:0]	01b	Default to reject FIS without interlock.
C7h	reserved	FISc7cfg[1:0]	01b	Default to reject FIS without interlock.
D4h	reserved	FISd4cfg[1:0]	01b	Default to reject FIS without interlock.
D9h	reserved	FISd9cfg[1:0]	01b	Default to reject FIS without interlock.
Others	reserved	FISocfg[1:0]	01b	Default to reject FIS without interlock.

- RxFIS[0-6]- First seven Dwords received from device. RxFIS[0] is the first Dword that contains the FIS header. RxFIS[6] is the last of the seven Dwords received. It is enough to support DMA Setup FIS.

Note that:

- FIS data can also be read out directly from RxFIS (first seven Dwords).
- All data to be transferred must be sent within one UDMA burst. Burst termination will not be allowed and may produce unpredictable result.
- There is no limit on received frame size.
- In a Data FIS, the receive FIFO will automatically advance one Dword to skip the header. Upon an interlocked FIS, the FIFO read pointer will rewind to the beginning so that the first Dword read is the header.

The following summarizes the behavior:

- On power up, the default configurations are as follows:
  - All defined FISes, except BIST Activate and DMA Setup, default to be supported (FISxxcfg[1:0] = '00').
  - BIST Activate is default to be accepted ONLY for Far-end Retimed Loopback and to be rejected for any other BIST types.
  - DMA Setup defaults to be rejected.
  - All undefined FISes default to be rejected (FISxxcfg[1:0] = '01').
- Sequences:
  - Upon reception of an unsupported FIS (FISxxcfg[1:0] = '01'), the Link/Transport Logic responds with R_ERR to the downstream device. The host will not be notified.
  - Upon reception of a supported FIS (FISxxcfg[1:0] = '00'), the Link/Transport Logic responds with R_OK at WTRM (if no error is detected) or R_ERR (if an error is detected) to the downstream device. The host will be notified only as required by the protocol.
  - Upon reception of an interlocked FIS (FISxxcfg[1:0] = '10'), the Link/Transport Logic sets the IntrlckFIS bit in the Smisc register. The following describes the possible sequence of events:
    - Sequence 1:
      - The Link Logic will continue to receive data while its buffer is being filled up. IntrlckFIS will cause an interrupt to the host.
      - The first 7 Dwords of the FIS are available to the host in the RxFIS0 to RxFIS6 registers.The driver will check the FIS type, clean up the PCI section, arm the DMA controller, and then assert the Rx_IFIS bit in the Smisc register.
      - The Link/Transport Logic transfers the received FIS, including the header, through the PCI interface to the host.
      - When all the data is received with no errors, the Link/Transport Logic will assert the IFIS_OK bit in the Smisc register. Otherwise one of the error bits will be set in the Serror register.
      - The host will set the Accept_IFIS bit to accept or Reject_IFIS to reject the FIS.
      - If no error is detected inside the frame and the Accept_IFIS bit is asserted, the Link/Transport Logic will send R_OK to the downstream device. If Reject_IFIS is asserted or any error is detected, the Link/Transport Logic will respond with R_ERR. Note that there is an interlock - if the frame is good, it will always wait for the Accept_IFIS or Reject_IFIS (if not asserted already) before responding.
    - Sequence 2:
      - Link/Transport Logic will continue to receive data while its buffer is being filled up. IntrlckFIS will cause an interrupt to the host.
      - Host reads the header; the driver will check the FIS type in RxFIS register and knows that the entire FIS is not larger than the size of RxFIS0 to 6 register.
      - Host waits for IFIS_OK (if any error detected – the error signals).
      - If IFIS_OK is received, host reads all data directly via PCI registers and then issues a Accept_IFIS (Link/Transport Logic to send R_OK) or a Reject_IFIS (Link/Transport Logic to send R_ERR).
      - If any error is detected, host can ignore, the Link will respond with R_ERR anyway.

9.4 FIS Types Not Affiliated with Current ATA/ATAPI operations

9.4.1 BIST Support

Far-End Retimed Loopback is supported in reception mode only. All other BIST codes will be rejected via R_ERR. It defaults to be interlocked supported (for Far-End Retimed Loopback only).
The SiI3112A does not support any BIST in transmission mode. There is no provision to send the test patterns and compare against loopback data.

9.4.1.1 BIST Signals

- When SiI3112A enters the BIST operation, the “PHY offline” mode will be set in the DET bits of the Sstatus register. This conditoin will remain asserted until the host generates an ATA reset (hreset_b asserted) or a COMINIT is received from the device.
-

9.4.2 DMA Setup

DMA Setup FIS can only be sent as a transparent FIS.
On Power up, DMA Setup FIS defaults to be rejected.

9.4.2.1 First Party DMA Read of Host memory by Device

Sequence (FIS41cfg[1:0] = '10', i.e. interlocked):

- Device send DMA Setup FIS to host. The "D" field in the FIS is '0'.
- The IntrlckFIS bit is set and causes an interrupt to the host.
- The host driver checks the FIS type (RxFIS), sets up, and arms the DMA controller.
- The host sets the Accept_FIS bit to accept the FIS.
- The host sends one or more Data FISes. Note that no DMA Activate FIS is required for first party DMA.
- There is no need to report transfer status.
-

9.4.2.2 First Party DMA Write of Host Memory by Device

Sequence (FIS41cfg[1:0] = '10', i.e. interlocked):

- Device send DMA Setup FIS to host. The "D" field in the FIS is '1'.
- The IntrlckFIS bit is set and causes an interrupt to the host.
- The host driver checks the FIS type (RxFIS), sets up, and arms the DMA controller.
- The host sets the Accept_FIS bit to accept the FIS.
- The device sends one or more Data FISes.
- There is no need to report transfer status.

10 ATA Command Supported

10.1 Data Modes

The SiI3112A PCI to Serial ATA Controller has an internal datapath interface between the PCI block and the Serial ATA controller block. The data modes (Register mode, PIO mode and DMA mode) are of no significance inside the SiI3112A.

10.2 ATA Commands

The SiI3112A PCI to Serial ATA Controller decodes ATA commands in hardware. The commands supported include ATA/ATAPI-5 and ATA/ATAPI-6 commands, including the 48-bit LBA extended commands. Certain obsolesced commands are also supported. The supported commands are listed below:

Table 10-1 Supported ATA Commands

Command	Command/ Features Codes	Comment
CFA Erase Sectors	C0h	
CFA Request Extended Error Code	03h	
CFA Translate Sector	87h	
CFA Write Multiple without Erase	CDh	
CFA Write Sectors without Erase	38h	
Check Media Card Type	D1h	
Check Power Mode	E5h	
Configure Stream	51h	
Device Configuration Freeze Lock	B1h/C1h	
Device Configuration Identify	B1h/C2h	
Device Configuration Restore	B1h/C0h	
Device Configuration Set	B1h/C3h	
Device Reset	08h	
Download Microcode	92h	
Execute Device Diagnostics	90h	The two Serial ATA ports for SiI3112A PCI to Serial ATA Controller are both "single masters".
Flush Cache	E7h	
Flush Cache Ext	EAh	48-bit LBA Command
Format Track	50h	Obsolesced vendor specific command, needs to be programmed as vendor specific commands
Get Media Status	DAh	
Identify Device	ECh	

Command	Command/ Features Codes	Comment
Identify Packet Device	A1h	
Idle	E3h	
Idle Immediate	E1h	
Initialize Device Parameters	91h	Obsolesced in ATA/ATAPI-6.
Media Eject	EDh	
Media Lock	DEh	
Media Unlock	DFh	
Nop	00h	
Packet	A0h	
Read Buffer	E4h	
Read DMA	C8h	
	C9h	Obsolesced Command code supported, decoded as Command Code C8h
Read DMA Ext	25h	48-bit LBA Command
Read DMA Queued	C7h	
Read DMA Queued Ext	26h	48-bit LBA Command
Read Log Ext	2Fh	
Read Long	22h	Obsolesced command
	23h	
Read Multiple	C4h	
Read Multiple Ext	29h	48-bit LBA Command
Read Native Max Address	F8h	
Read Native Max Address Ext	27h	48-bit LBA Command
Read Sector(s)	20h	
	21h	Obsolesced Command code supported, decoded as Command Code 20h
Read Sector(s) Ext	24h	48-bit LBA Command
Read Stream DMA	2A	
Read Stream PIO	2B	
Read Verify Sector(s)	40h	
	41h	Obsolesced Command code supported, decoded as Command Code 40h
Read Verify Sector(s) Ext	42h	48-bit LBA Command
Recalibrate	10h	Obsolesced command supported.
Security Disable Password	F6h	
Security Erase Prepare	F3h	
Security Erase Unit	F4h	

Command	Command/ Features Codes	Comment
Security Freeze Lock	F5h	
Security Set Password	F1h	
Security Unlock	F2h	
Seek	70h	
Service	A2h	
Set Features	EFh	
Set Max Address	F9h/00h	
Set Max Address Ext	37h	48-bit LBA Command
Set Max Freeze Lock	F9h/04h	
Set Max Lock	F9h/02h	
Set Max Unlock	F9h/03h	Obsolesced command supported.
Set Max Set Password	F9h/01h	
Set Multiple Mode	C6h	The SiI3112A PCI to Serial ATA Controller intercepts the command to set up the number of sectors for a DRQ block upon this command.
Sleep	E6h	
Smart Disable Operations	B0h/D9h	
Smart Enable Operations	B0h/D8h	
Smart Enable/Disable Attributes Autosave	B0h/D2h	
Smart Execute Off-Line Immediate	B0h/D4h	
Smart Read Attribute Thresholds	B0h/D1h	Obsolesced command supported.
Smart Read Data	B0h/D0h	
Smart Read Log	B0h/D5h	
Smart Return Status	B0h/DAh	
Smart Save Attribute Values	B0h/D3h	Obsolesced command supported.
Smart Write Log	B0h/D6h	
Standby	E2h	
Standby Immediate	E0h	
Write Buffer	E8h	
Write DMA	CAh	
	CBh	Obsolesced Command code supported, decoded as Command Code CAh
Write DMA Ext	35h	48-bit LBA Command
Write DMA Queued	CCh	
Write DMA Queued Ext	36h	48-bit LBA Command
Write Log Ext	3Fh	
Write Long	32h	Obsolesced command supported

Command	Command/ Features Codes	Comment
	33h	
Write Multiple	C5h	
Write Multiple Ext	39h	48-bit LBA Command
Write Sector(s)	30h	
	31h	Obsolesced Command code supported, decoded as Command Code 30h
Write Sector(s) Ext	34h	48-bit LBA Command
Write Stream DMA	3Ah	
Write Stream PIO	3Bh	

10.2.1 Obsolesced Commands

Certain obsolesced commands are supported as shown in the table above. Commands Read Long and Write Long are to be treated differently (see the following section)

10.2.2 Read/Write Long

Read Long and Write Long commands are implemented in accordance with the ATA/ATAPI-3. The PIO Mode used (Mode 0) is of no significance in the SiI3112A PCI to Serial ATA Controller , as the datapath interface between the PCI and the Link/Transport logic is internal. The number of vendor specific bytes is provided by the Serial ATA PIO Setup FIS from the downstream device as follows:

n = ((XC - 512) + 1) ÷2 (i.e., XC - 512 divided by 2 with round up)

where:

- n is the number of vendor specific bytes.
- XC is the transfer count.

The total number of data dwords in the Data FIS is given by:

m = (XC + 3) ÷ 4 (i.e., XC divided by 4 with round up)

where:

- m is the number of data dwords in the Data FIS, excluding the FIS header (and CRC).
- XC is the transfer count.

In this command, the Data FIS must use the following format:

Table 10-2 Data FIS

Dword	Byte 3	Byte 2	Byte 1	Byte 0
0	Data FIS Header			
1	Sector Data Byte 3	Sector Data Byte 2	Sector Data Byte 1	Sector Data Byte 0
2	Sector Data Byte 7	Sector Data Byte 6	Sector Data Byte 5	Sector Data Byte 4
3 ... 126				
127	Sector Data Byte 507	Sector Data Byte 506	Sector Data Byte 505	Sector Data Byte 504
128	Sector Data Byte 511	Sector Data Byte 510	Sector Data Byte 509	Sector Data Byte 508
129	Don't care	Vendor Specific Byte 1	Don't care	Vendor Specific Byte 0
130	Don't care	Vendor Specific Byte 3	Don't care	Vendor Specific Byte 2

Table 10-2 Data FIS

Dword	Byte 3	Byte 2	Byte 1	Byte 0
...				
Last (n is even)	Don't care	Vendor Specific Byte n-1	Don't care	Vendor Specific Byte n-2
Last (n is odd)	Don't care	Don't care	Don't care	Vendor Specific Byte n-1

10.3 Vendor Specific Command Support

The SiI3112A PCI to Serial ATA Controller supports most vendor specific commands that utilize existing protocols.

10.3.1 Silicon Image's Vendor Specific Commands

Silicon Image defines several vendor specific commands (all of which use Expanded Features in 48-bit LBA addressing) to support vendor specific and reserved commands:

- VS Unlock Vendor Specific: Unlock the host or device to support vendor specific commands.
- VS Unlock Reserved: Unlock the host or device to support reserved commands.
- VS Unlock Individual: Unlock the host or device to support individual vendor specific and reserved commands.
- VS Lock: Lock the host or device to abort all vendor specific and reserved commands.
- VS Set General Protocol: Determine the General Protocol Code to be used for all subsequent vendor specific commands (if unlocked via a VS Unlock Vendor Specific command) and reserved commands (if unlocked via a VS Unlock Reserved command).
- VS Set Command Protocol: Select protocols for individual vendor specific and reserved commands (if unlocked via a VS Unlock Individual command). A Command Protocol Table will be maintained. Commands set up via this will follow the protocol set in this command instead of the original command protocol defined in Table 10-1. Hence, commands can be "overloaded" using this method.

10.3.1.1 Potential Conflicts with other Vendor Specific Commands

The commands chosen use Subcommand (Features) code F1h under the SMART command (B0h). While this code is not expected to be used by device manufacturers, there is always the possibility that it is used. If such conflict happens, the device manufacturers must reassign a new code to the conflicting command in order to use this scheme.

10.3.1.2 Other Expanded Features Codes

The commands above use some of the l Expanded Features Codes. All Expanded Features Codes under Command Code B0h and Subcommand (Features) Code F1h are reserved as Silicon Image Vendor Specific commands.

10.3.2 Vendor Specific, Reserved, Retired and Obsolesced Commands

These types of commands are treated differently:

- Vendor specific commands: Expect for those commands whose protocols are individually set (via the VS Unlock Individual and VS Set Command Protocol commands), the host or device must be unlocked via the VS Unlock Vendor Specific command before such commands can be issued. Otherwise, vendor specific commands are aborted.
- Reserved commands: Expect for those commands whose protocols are individually set (via the VS Set Unlock Individual and VS Set Command Protocol commands), the host or device must be unlocked via the VS Unlock Reserved command before such commands can be issued. Otherwise, reserved commands are aborted.
- Obsolesced and Retired commands: Implementation of such commands is optional.

10.3.3 Definitions

Command - Unless otherwise stated, this is the value written to the ATA Command Register.
Command Code - This is the code corresponding to the ATA command. It is also a field in the Command Protocol Table.
Command Protocol Table - The table that contains the individual vendor specific and reserved commands supported (see Table 10-3
Features - Unless otherwise stated, this is the value written to the ATA Features Register.
Features Code - This is the code corresponding to the ATA Features register. It is also a field in the Command Protocol Table.
Features Mask - This is a field in the Command Protocol Table that allows several Features Codes to be used for the same command.
General Protocol Code - On a VS Set General Protocol command after a VS Unlock Vendor Specific or VS Unlock Reserved command, the General Protocol Code will be set as the protocol for all undefined vendor specific (if unlocked) and/or undefined reserved (if unlocked) commands. An undefined vendor specific/reserved command is one that does not have an entry in the Command Protocol Table.
Protocol Code - This code determines the protocol associate with a command. It is also a field in the Command Protocol Table.
Subcommand Code - Same as Features Code.
VS Features Set - The commands needed to support this scheme (See Section 10.4).
VS State Machine - The state machine that determines what vendor specific and reserved commands are to be supported (see Section 10.5).

10.3.4 Scheme

10.3.4.1 Reset

Upon any hardware reset or the Serial ATA COMRESET, or COMINIT, the VS State Machine in the SiI3112A will be initialized to the locked state (the "default" state), which will abort all vendor specific and reserved commands.
Soft Reset (via Device Control register bit 2) does NOT affect the VS State Machine.

10.3.4.2 Operation

The following summarizes how the vendor specific/reserved commands are supported. Detailed operations are described in later sections.

1. The default state is locked. All vendor specific commands will be aborted.
2. Unlock:
   - To unlock the SiI3112A and/or device to support vendor specific commands: Issue a VS Unlock Vendor Specific command. The SiI3112A will also send this command to the Serial ATA device. If the downstream Serial ATA device is a bridge, the device bridge may optionally issue this command to the attached parallel ATA device. Note that the unlock will take effect in the SiI3112A even if an ABORT status is reported.
   - To unlock the SiI3112A and/or device to support reserved commands: Issue a VS Unlock Reserved command. The SiI3112A will also send this command to the Serial ATA device. If the downstream Serial ATA device is a bridge, the device bridge may optionally issue this command to the attached parallel ATA device. Note that the unlock will take effect in the SiI3112A even if an ABORT status is reported.
   - To support individual vendor specific or reserved command: Issue a VS Unlock Individual command.

   Combinations of the above can be supported by simply issuing the appropriate combinations of VS Unlock Vendor Specific, VS Unlock Reserved and VS Unlock Individual commands.
3. Set protocol. There are two ways to set up protocol(s):
   - Issue a VS Set Command Protocol command to set up a protocol for a specific command. The information is logged in a Command Protocol Table inside the SiI3112A. This protocol will remain valid until overwritten by a VS Set Command Protocol command that overwrites the Command Protocol Table entry, the VS Lock command, hardware reset, COMRESET, or COMINIT. The SiI3112A will also send this command to the Serial ATA device. If the downstream Serial ATA device is a bridge, the device bridge may optionally issue this command to the attached parallel ATA device. Note that the protocol will be set in the SiI3112A even if an ABORT status is reported. If more than one command protocol has to be set up, a VS Set Command protocol will have to be issued for each command.
   - Issue a VS Set General Protocol command to set the General Protocol Code for the next vendor specific command. This protocol will remain valid until the next VS Set General Protocol command, VS Lock command, hardware reset, COMRESET, or COMINIT. The SiI3112A will also send this command to the Serial ATA device. If the downstream Serial ATA device is a bridge, the device bridge may optionally issue this command to the attached

parallel ATA device. Note that the protocol will be set in the SiI3112A even if an ABORT status is reported. Commands already set up via the VS Set Command Protocol will follow the protocol set in the VS Set Command Protocol command instead of the one set in this command.

4. Issue any command:
   - Any vendor specific commands (if unlocked for vendor specific commands) or reserved commands (if unlocked for reserved commands) that has an associated protocol set via the VS Set Command Protocol command will be executed using that protocol.
   - Any vendor specific commands (if unlocked for vendor specific commands) or reserved commands (if unlocked for reserved commands) that does not have an associated protocol, i.e. not set up by the VS Set Command Protocol command, will be executed using the protocol loaded from the latest VS Set General Protocol command.
   - Other supported commands will follow the predefined protocols.
   - Other unsupported commands will be aborted.
5. To change the protocol for vendor specific commands, simply reissue the VS Set General Protocol or the VS Set Command Protocol command with the new protocol.
6. When done, issue the VS Lock command to return to the default VS state. The SiI3112A will also send the VS Lock command to the Serial ATA device. If the downstream Serial ATA device is a bridge, the device bridge may optionally issue this command to the attached parallel ATA device. Note that the lock will take effect in the SiI3112A even if an ABORT status is reported.

10.4 SiI3112A Vendor Specific Commands

10.4.1 Feature Set/Command Summary

Table 10-3 Vendor Specific Command Summary

Command	Command Code	Features Code	Expanded Features Code	Description
VS Lock	B0h	F1h	D5h	Return VS state machine to VS_LOCKED (Section 10.5).
VS Unlock Vendor Specific	B0h	F1h	12h	Unlock VS state machine to support vendor specific commands.
VS Unlock Reserved	B0h	F1h	22h	Unlock VS state machine to support reserved commands.
VS Unlock Individual	B0h	F1h	32h	Unlock VS state machine to support reserved commands.
VS Set General Protocol	B0h	F1h	F0h	Set the General Protocol Code for all vendor specific commands and reserved commands, if the corresponding command types are unlocked. The vendor specific and reserved commands that are individually set via VS Set Command Protocol commands will not follow the protocol set by this command.
VS Set Command Protocol	B0h	F1h	87h	Set protocol for an individual vendor specific or reserved command. The information is logged in a Command Protocol Table entry.
	B0h	F1h	Other than above	Reserved.

Compared with other features sets, The VS Features Set ignores the bit 0 (ERR) in the Status register together with the Error register. All commands are considered completed once BSY = 0 and DRDY = 1 in the Status register.

10.4.2 VS Lock

10.4.2.1 Command/Subcommand/Expanded Features Code

Command Code: B0h
Subcommand (Features) Code: F1h
Expanded Features Code: D5h

10.4.2.2 Protocol

Non-data (Ext)

10.4.2.3 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	F1h							
	Previous (Expanded)	D5h							
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Command		B0h							

1. The DEV bit usage in the Serial ATA specification must be followed.

10.4.2.4 Outputs

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	na	na	na
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Status		BSY	DRDY	na	na	na	na	na	na[2]

1. The DEV bit usage in the Serial ATA specification must be followed.
2. Error bit will be ignored. Completion is determined by by BSY = 0 and DRDY = 1 only.

10.4.2.5 Description

This command locks the SiI3112A from supporting vendor specific commands. All vendor specific and reserved commands issued afterwards will be aborted.
Non-data (ext) protocol will be used with this command. The SiI3112A will send this command to the Serial ATA device. The following situations may happen:

- Case 1: The Serial ATA device (native or bridge) responds with a completed status. Both sides are set up to support this scheme.
- Case 2: The Serial ATA device bridge supports this scheme. It may optionally pass this command to a parallel ATA device:
    - If passed to a parallel ATA device, the parallel ATA device responds with an abort status, which may be reported back to the SiI3112A
    - If not passed to a parallel ATA device, the device bridge should still respond with a device-to-host Register FIS to terminate BSY in the SiI3112A.

  However, both the SiI3112A and the device bridge will ignore the abort status and will consider the VS block locked.
- Case 3: The Serial ATA device is a native device and responds with an abort. The SiI3112A will ignore the abort status and will consider the VS block locked.

In other words, regardless of the status reported (aborted or complete), the SiI3112A and device that support this scheme will be locked.

10.4.3 VS Unlock Vendor Specific

10.4.3.1 Command/Subcommand/Expanded Features Code

Command Code: B0h
Subcommand (Features) Code: F1h
Expanded Features Code: 12h

10.4.3.2 Protocol

Non-data (Ext)

10.4.3.3 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	F1h							
	Previous (Expanded)	12h							
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Command		B0h							

1. The DEV bit usage in the Serial ATA specification must be followed.

10.4.3.4 Outputs

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	na	na	na
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Status		BSY	DRDY	na	na	na	na	na	na[2]

1. The DEV bit usage in the Serial ATA specification must be followed.
2. Error bit will be ignored. Completion is determined by by BSY = 0 and DRDY = 1 only.

10.4.3.5 Description

This command unlocks the SiI3112A to support vendor specific commands. Once this command is executed, the SiI3112A will remain unlocked until:

- A VS Lock command that returns the VS state to the default locked state, or;
- A hardware reset, or COMINIT or COMRESET.

Note that the VS Unlock Individual command, the VS Unlock Reserved command and Soft Reset have no effect on the VS state.

- If a VS Unlock Individual command is issued afterwards, the SiI3112A will be unlocked for both individual vendor specific/reserved commands and other vendor specific commands.
- If a VS Unlock Reserved command is issued afterwards, the SiI3112A willl be unlocked for both vendor specific and reserved commands.
- If both VS Unlock Individual and VS Unlock Reserved are issued afterwards, the SiI3112A will be unlocked for individual vendor specific/reserved commands, as well as other vendor specific and reserved commands.

The SiI3112A will use the non-data (ext) protocol with this command. The SiI3112A will send this command to the Serial ATA device. The following situations may happen:

- Case 1: The Serial ATA device (native or bridge) responds with a completed status. Both sides are set up to support this scheme.
- Case 2: The Serial ATA device bridge supports this scheme. It may optionally pass this command to a parallel ATA device:
    - If passed to a parallel ATA device, the parallel ATA device responds with an abort status, which may be reported back to the SiI3112A.
    - If not passed to a parallel ATA device, the device bridge should still respond with a device-to-host Register FIS to terminate BSY in the SiI3112A.

  However, the SiI3112A will ignore the abort status and will consider the unlock event successful.
- The Serial ATA device is a native device and responds with an abort. The SiI3112A will ignore the abort status and will consider the unlock event successful.

In other words, regardless of the status reported (aborted or complete), the SiI3112A will be unlocked to support vendor specific commands.

10.4.4 VS Unlock Reserved

10.4.5 Command/Subcommand/Expanded Features Code

Command Code: B0h
Subcommand (Features) Code: F1h
Expanded Features Code: 22h

10.4.5.1 Protocol

Non-data (Ext)

10.4.5.2 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	F1h							
	Previous (Expanded)	22h							
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Command		B0h							

1. The DEV bit usage in the Serial ATA specification must be followed.

10.4.5.3 Outputs

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	na	na	na
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Status		BSY	DRDY	na	na	na	na	na	na[2]

1. The DEV bit usage in the Serial ATA specification must be followed.
2. Error bit will be ignored. Completion is determined by by BSY = 0 and DRDY = 1 only.

10.4.5.4 Description

This command unlocks the SiI3112A to support reserved commands. Once this command is executed, the SiI3112A will remain unlocked until:

- A VS Lock command that returns the VS state to the default locked state, or;
- A hardware reset, or COMINIT or COMRESET.

Note that the VS Unlock Vendor Specific command, the VS Unlock Individual command and Soft Reset have no effect on the VS state.

- If a VS Unlock Vendor Specific command is issued afterwards, the SiI3112A will be unlocked for both reserved and vendor specific commands.
- If a VS Unlock Individual command is issued afterwards, the SiI3112A will be unlocked for both individual vendor specific/reserved command protocols and other reserved commands.
- If both VS Unlock Vendor Specific and VS Unlock Individual are issued afterwards, the SiI3112A be unlocked for individual vendor specific/reserved command protocols, as well as other vendor specific and reserved commands.

The SiI3112A will use the non-data (ext) protocol with this command. The SiI3112A will send this command to the Serial ATA device. The following situations may happen:

- Case 1: The Serial ATA device (native or bridge) responds with a completed status. Both sides are set up to support this scheme.
- Case 2: The Serial ATA device bridge supports this scheme. It may optionally pass this command to a parallel ATA device:
    - If passed to a parallel ATA device, the parallel ATA device responds with an abort status, which may be reported back to the SiI3112A.
    - If not passed to a parallel ATA device, the device bridge should still respond with a device-to-host Register FIS to terminate BSY in the SiI3112A.

  However, the SiI3112A will ignore the abort status and will consider the unlock event successful.
- Case 3:The Serial ATA device is a native device and responds with an abort. The SiI3112A will ignore the abort status and will consider the unlock event successful.

In other words, regardless of the status reported (aborted or complete), the SiI3112A will be unlocked to support reserved commands.

10.4.6 VS Unlock Individual

10.4.6.1 Command/Subcommand/Expanded Features Code

Command Code: B0h
Subcommand (Features) Code: F1h
Expanded Features Code: 32h

10.4.6.2 Protocol

Non-data (Ext)

10.4.6.3 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	F1h							
	Previous (Expanded)	32h							
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Command		B0h							

1. The DEV bit usage in the Serial ATA specification must be followed.

10.4.6.4 Outputs

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	na	na	na
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Status		BSY	DRDY	na	na	na	na	na	na[2]

1. The DEV bit usage in the Serial ATA specification must be followed.
2. Error bit will be ignored. Completion is determined by by BSY = 0 and DRDY = 1 only.

10.4.6.5 Description

This command unlocks the SiI3112A to support individual vendor specific and reserved commands. Once this command is executed, the SiI3112A will remain unlocked until:

- A VS Lock command that returns the VS state to the default locked state, or;
- A hardware reset, or COMINIT or COMRESET.

Note that the VS Unlock Vendor Specific command, the VS Unlock Reserved command and Soft Reset have no effect on the VS state.

- If a VS Unlock Vendor Specific command is issued afterwards, the SiI3112A will be unlocked for both individual command protocols and other vendor specific commands..
- If a VS Unlock Reserved command is issued afterwards, the SiI3112A will be unlocked for both individual vendor specific/reserved command and other reserved commands..
- If both VS Unlock Vendor Specific and VS Unlock Reserved are issued afterwards, SiI3112A will be unlocked for individual vendor specific/reserved command, as well as other vendor specific and reserved commands.

The SiI3112A will use the non-data (ext) protocol with this command. The SiI3112A will send this command to the Serial ATA device. The following situations may happen:

- Case 1: The Serial ATA device (native or bridge) responds with a completed status. Both sides are set up to support this scheme.
- Case 2: The Serial ATA device bridge supports this scheme. It may optionally pass this command to a parallel ATA device:
    - If passed to a parallel ATA device, the parallel ATA device responds with an abort status, which may be reported back to the SiI3112A.
    - If not passed to a parallel ATA device, the device bridge shouldl still respond with a device-to-host Register FIS to terminate BSY in the SiI3112A.

  However, the SiI3112A will ignore the abort status and will consider the unlock event successful.
- Case 3: The Serial ATA device is a native device and responds with an abort. The SiI3112A will ignore the abort status and will consider the unlock event successful.

In other words, regardless of the status reported (aborted or complete), the SiI3112A willl be unlocked to support individual vendor specific/reserved commands.

10.4.7 VS Set General Protocol

10.4.7.1 Command/Subcommand Code/Expanded Features Code

Command Code: B0h
Subcommand (Features) Code: F1h
Expanded Features Code: F0h

10.4.7.2 Protocol

Non-data (Ext)

10.4.7.3 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	F1h							
	Previous (Expanded)	F0h							
Sector Count	Current	na							
	Previous (Expanded)	Protocol Code (See Section 10.6)							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Command		B0h							

1. The DEV bit usage in the Serial ATA specification must be followed.

10.4.7.4 Outputs

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	na	na	na
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Status		BSY	DRDY	na	na	na	na	na	na[2]

1. The DEV bit usage in the Serial ATA specification must be followed.
2. Error bit will be ignored. Completion is determined by by BSY = 0 and DRDY = 1 only.

10.4.7.5 Description

If the VS state is unlocked for vendor specifc or for reserved, this command will set the General Protocol Code for the next vendor specific/reserved command(s), except for those individually set via the VS Set Command Protocol commands. The protocol will return to, Abort (Protocol Code = 00h) upon a lock event, i.e.:

- A VS Lock command to return the VS state to the default locked state, or;

- A hardware reset, or COMINIT or COMRESET.

The General Protocol is passed to the SiI3112A and device via the Expanded Sector Count register. The protocols and codes are described in Table10-6.
The SiI3112A will use the non-data (ext) protocol with this command. The SiI3112A will send this command to the Serial ATA device. The following situations may happen:

- Case 1: The Serial ATA device (native or bridge) responds with a completed status. Both sides are set up to support this scheme.
- Case 2: The Serial ATA device bridge supports this scheme. It may optionally pass this command to a parallel ATA device:
    - If passed to a parallel ATA device, the parallel ATA device responds with an abort status, which may be reported back to the SiI3112A.
    - If not passed to a parallel ATA device, the device bridge should still respond with a device-to-host Register FIS to terminate BSY in the SiI3112A.

  However, the SiI3112A will ignore the abort status and will consider the protocol set.
- Case 3: The Serial ATA device is a native device and responds with an abort. SiI3112A will ignore the abort status and will consider the protocol set.

In other words, regardless of the status reported (aborted or complete), the SiI3112A willl accept the protocol as valid.

10.4.8 VS Set Command Protocol

10.4.8.1 Command/Subcommand/Expanded Features Code

Command Code: B0h
Subcommand (Features) Code: F1h
Expanded Features Code: 87h

10.4.8.2 Protocol

Non-data (Ext)

10.4.8.3 Inputs

Register		7	6	5	4	3	2	1	0
Features	Current	F1h							
	Previous (Expanded)	87h							
Sector Count	Current	0	0	0	0	Code Tag			
	Previous (Expanded)	Protocol Code (See Section 10-6)							
LBA Low	Current	Command Code							
	Previous (Expanded)	na							
LBA Mid	Current	Features Code							
	Previous (Expanded)	Features Mask							
LBA High	Current	00h							
	Previous (Expanded)	00h							
Device		obs	na	obs	DEV[1]	na	na	na	na
Command		B0h							

1. The DEV bit usage in the Serial ATA specification must be followed.

10.4.8.4 Outputs

Register		7	6	5	4	3	2	1	0
Error		na	na	na	na	na	na	na	na
Sector Count	Current	na							
	Previous (Expanded)	na							
LBA Low	Current	na							
	Previous (Expanded)	na							
LBA Mid	Current	na							
	Previous (Expanded)	na							
LBA High	Current	na							
	Previous (Expanded)	na							
Device		obs	na	obs	DEV[1]	na	na	na	na
Status		BSY	DRDY	na	na	na	na	na	na[2]

1. The DEV bit usage in the Serial ATA specification must be followed.
2. Error bit will be ignored. Completion is determined by by BSY = 0 and DRDY = 1 only.

10.4.8.5 Description

If the VS state is unlocked for individual vendor specifc/reserved commands, this command will set the protocol for the specific commands. Up to 16 individual vendor specific/reserved commands are supported via a Command Protocol Table. The 16 entries are organized as follows:

Table 10-4 16-Entry Command Protocol Table

Code Tag (Entry #)	Command Code	Features Code	Features Mask	Protocol Code
0h				
1h				
...				
Eh				
Fh				

When a command is issued, its Command and Features registers will be compared against all of the above entries. If the following conditions are all met, the protocol for that entry will be used:

- Command = Command Code, and;
- (Features ⊕ Features Code) & Features Mask = 00h.

Note that:

- If a vendor specific or reserved command is mapped to more than one entry the result is indeterminate.
- Commands set up using this command will follow the new protocol instead of the original protocol defined for the command, i.e., commands can be “overloaded” using this mechanism.

Upon a lock event, all Command Codes will be initialized to NOP (00h) and all Protocol Codes will be initialized to Abort (00h). The following conditions are considered lock events:

- A VS Lock command to return the VS state to the default locked state, or;
- A hardware reset, or COMINIT or COMRESET.

The following registers are used when issuing the command (but have no meaning for outputs):

Register		Bit(s)	Field	Description
Sector Count	Current	7-4	0h	Must be 0h. Reserved for expansion if more than 16 individual vendor specific/reserved commands are supported.
		3-0	Code Tag	Up to 16 individual vendor specific/reserved commands are supported. This code tag is to select which of the 16 entries the code is to be written to. Earlier content in that entry will be replaced with the new information.
	Previous (Expanded)	7-0	Protocol Code	See Section 10-6
LBA Low	Current	7-0	Command Code	The Command register value for the individual vendor specific/reserved command.
	Previous (Expanded)	7-0	na	Not used.
LBA Mid	Current	7-0	Features Code	The Features register value for the individual vendor specific/reserved command.
	Previous (Expanded)	7-0	Features Mask	One single protocol can be assigned to a group of commands with the same Command Code but different Features Codes. If a Features Mask bit is '0', the corresponding Features Code bit will be ignored for comparison.
LBA High	Current	7-0	00h	Reserved for Expanded Features Code.
	Previous (Expanded)	7-0	00h	Reserved for Expanded Features Mask.

The SiI3112A will use the non-data (ext) protocol with this command. The SiI3112A will send this command to the Serial ATA device. The following situations may happen:

- Case 1: The Serial ATA device (native or bridge) responds with a completed status. Both sides are set up to support this scheme.
- Case 2: The Serial ATA device bridge supports this scheme. It may optionally pass this command to a parallel ATA device:
    - If passed to a parallel ATA device, the parallel ATA device responds with an abort status, which may be reported back to the SiI3112A.
    - If not passed to a parallel ATA device, the device bridge should still respond with a device-to-host Register FIS to terminate BSY in the SiI3112A

  However, the SiI3112A will ignore the abort status and will consider the protocol set.
- Case 3: The Serial ATA device is a native device and responds with an abort. The SiI3112A will ignore the abort status and will consider the protocol set.

In other words, regardless of the status reported (aborted or complete), the SiI3112A will accept the protocol as valid.

10.5 State Transitions

VS_LOCKED	• Vendor specific/Reserved commands not supported. All vendor specific and reserved commands will result in an ABORT status. • General Protocol Code will be 00h. • Command Protocol Table initialized with all Command Codes = 00h and all Protocol Codes = 00h.		
1	Received VS Unlock Vendor Specific command	→	VS_VS
2	Received VS Unlock Reserved command	→	VS_RSV
3	Received VS Unlock Individual command	→	VS_IND
4	Otherwise	→	VS_LOCKED

Figure 10-1 Default state - VS_LOCKED

VS_VS	• On VS Set General Protocol command, set General Protocol Code. • Commands other than vendor specific or reserved commands will be executed according to the predefined protocol. • All vendor specific commands will be executed according to the General Protocol Code. • All reserved commands will result in an ABORT status.		
1	Received VS Unlock Reserved command	→	VS_VS_RSV
2	Received VS Unlock Individual command	→	VS_VS_IND
3	Received VS Lock command	→	VS_LOCKED
4	Otherwise	→	VS_VS

Figure 10-2 VS_VS

VS_RSV	• On VS Set General Protocol command, set General Protocol Code. • Commands other than vendor specific or reserved commands will be executed according to the predefined protocol. • All reserved commands will be executed according to the General Protocol Code. • All vendor specific commands will result in an ABORT status.		
1	Received VS Unlock Vendor Specific command	→	VS_VS_RSV
2	Received VS Unlock Individual command	→	VS_RSV_IND
3	Received VS Lock command	→	VS_LOCKED
4	Otherwise	→	VS_RSV

Figure 10-3 VS_RSV

VS_IND	• On VS Set Command Protocol command, update the corresponding Command Protocol Table entry. • All commands with entries in the Command Protocol Table will be executed according to the Protocol Code in the corresponding Command Protocol entry. • All other non-vendor-specific and non-reserved commands will be executed according to the predefined protocol. • All other commands will result in an ABORT status.			
	1	Received VS Unlock Reserved command	→	VS_VS_RSV
	2	Received VS Unlock Vendor Specific command	→	VS_VS_IND
	3	Received VS Lock command	→	VS_LOCKED
	4	Otherwise	→	VS_IND

Figure 10-4 VS_IND

VS_VS_RSV	• On VS Set General Protocol command, set General Protocol Code. • Commands other than vendor specific or reserved commands will be executed according to the predefined protocol. • All vendor specific/reserved commands will be executed according to the General Protocol Code.			
	1	Received VS Unlock Individual command	→	VS_VS_RSV_IND
	2	Received VS Lock command	→	VS_LOCKED
	3	Otherwise	→	VS_VS_RSV

Figure 10-5 VS_VS_RSV

VS_VS_IND	• On VS Set General Protocol command, set General Protocol Code. • On VS Set Command Protocol command, update the corresponding Command Protocol Table entry. • All commands with entries in the Command Protocol Table will be executed according to the Protocol Code in the corresponding Command Protocol entry. • All other vendor specific commands will be executed according to the General Protocol Code. • All other non-reserved commands will be executed according to the predefined protocol. • All other commands will result in an ABORT status.			
	1	Received VS Unlock Reserved command	→	VS_VS_RSV_IND
	2	Received VS Lock command	→	VS_LOCKED
	3	Otherwise	→	VS_VS_IND

Figure 10-6 VS_VS_IND

VS_RSV_IND	• On VS Set General Protocol command, set General Protocol Code. • On VS Set Command Protocol command, update the corresponding Command Protocol Table entry. • All commands with entries in the Command Protocol Table will be executed according to the Protocol Code in the corresponding Command Protocol entry. • All other reserved commands will be executed according to the General Protocol Code. • All other non-vendor-specific commands will be executed according to the predefined protocol. • All other commands will result in an ABORT status.

1	Received VS Unlock Vendor Specific command	→	VS_VS_RSV_IND
2	Received VS Lock command	→	VS_LOCKED
3	Otherwise	→	VS_RSV_IND

Figure 10-7 VS_RSV_IND

VS_VS_RSV_IND	• On VS Set General Protocol command, set General Protocol Code. • On VS Set Command Protocol command, update the corresponding Command Protocol Table entry. • All commands with entries in the Command Protocol Table will be executed according to the Protocol Code in the corresponding Command Protocol entry. • All other vendor specific/reserved commands will be executed according to the General Protocol Code. • All other commands will be executed according to the predefined protocol.

1	Received VS Lock command	→	VS_LOCKED
2	Otherwise	→	VS_VS_RSV_IND

Figure 10-8 VS_VS_RSV_IND

10.6 Protocols Summary

Table 10-5 Protocol Code Encoding Scheme

Protocol Code	Protocol	Codes Defined	Bit Assignment
00h	Abort	00h	
01h-3Fh A2h-AFh B3h-BFh E0h-EFh F1h-FFh			Reserved
40h-4Fh			Vendor Specific
80h-8Fh C0h-CFh (1x00xxxxb)	PIO Data in/Out	80h, 81h, 82h, 87h, 88h, 89h, 8Ah, 8Bh, 8Fh, C0h, C2h, C8h, CAh	Bit 6: • 0 - legacy addressing • 1 - 48-bit LBA addressing Bit 3: • 0 - data in (read) • 1 - data out (write) Bits 2-0: • 000b - sector count is given by the Sector Count register. • 001b - only one sector, Sector Count is ignored. • 010b - blocks of multiple sectors, e.g., Read/Write Multiple. • 011b - sector count is given by Sector Number and Sector Count registers, e.g. Download Microcode. • 100b-110b - reserved • 111b - 512 plus vendor specific bytes, e.g. Read/Write Long.
90h-9Fh D0h-DFh (1x01xxxxb)	DMA	90h, 91h, 98h, 99h, D0h, D1h, D8h, D9h	Bit 6: • 0 - legacy addressing • 1 - 48-bit LBA addressing Bit 3: • 0 - data in (read) • 1 - data out (write) Bits 2-1: • 00b - currently defined • 01b-11b - reserved. Bit 0: • 0 - not queued. • 1 - queued.
A0h	Packet	A0h	
A1h	Service	A1h	
B0h,F0h (1x110000b)	Non-Data	B0h, F0h	Bit 6: • 0 - legacy addressing • 1 - 48-bit LBA addressing
B1h	Execute Device Diagnostic	B1h	
B2h	Device Reset	B2h	

Table 10-6 Vendor Specific Protocol Code (in Alphabetical Order)

Protocol	Protocol Code	Description
Abort	00h	Abort command. Status =51h and Error = 04h. Command will not be passed to downstream device(s).
Device Reset	B2h	Device Reset protocol.
Execute Device Diagnostic	B1h	Execute Device protocol (for host bridges arranged in master-slave configuration, both will respond regardless of the DEV bit in the Device register.
Non-Data	B0h	Non-Data protocol.
Non-Data (Ext)	F0h	Non-Data (Ext) protocol.
Packet	A0h	Packet protocol.
PIO Data In (Read Multiple)	82h	PIO Data In protocol for reading blocks of multiple sectors, e.g., Read Multiple.
PIO Data In (Read Multiple, Ext)	C2h	PIO Data In protocol for reading blocks of multiple sectors for 48-bit LBA commands, e.g., Read Multiple Ext.
PIO Data In (Sectors)	80h	PIO Data In protocol, sector count is given by the Sector Count register.
PIO Data In (Sectors, Ext)	C0h	PIO Data In protocol for 48-bit LBA commands, sector count is given by the Sector Count register.
PIO Data In (Single Sector)	81h	PIO Data In protocol, only one sector, Sector Count is ignored.
PIO Data Out (Download Microcode)	8Bh	PIO Data Out protocol, sector count is given by Sector Number and Sector Count registers.
PIO Data Out (Sectors)	88h	PIO Data Out protocol, sector count is given by the Sector Count register.
PIO Data Out (Sectors, Ext)	C8h	PIO Data Out protocol for 48-bit LBA commands, sector count is given by the Sector Count register.
PIO Data Out (Single Sector)	89h	PIO Data Out protocol, only one sector, Sector Count is ignored.
PIO Data Out (Write Multiple)	8Ah	PIO Data Out protocol for writing blocks of multiple sectors, e.g., Write Multiple.
PIO Data Out (Write Multiple, Ext)	CAh	PIO Data Out protocol for writing blocks of multiple sectors for 48-bit LBA commands, e.g., Write Multiple Ext
Read DMA	90h	Read DMA protocol.
Read DMA (Ext)	D0h	Read DMA protocol for 48-bit LBA commands.
Read DMA Queued	91h	Read DMA Queued protocol.
Read DMA Queued (Ext)	D1h	Read DMA Queued for 48-bit LBA commands.
Read Long	87h	PIO Data In protocol, 512 plus vendor specific bytes, e.g. Read Long.
Service	A1h	Service protocol.
Write DMA	98h	Write DMA protocol.
Write DMA (Ext)	D8h	Write DMA protocol for 48-bit LBA commands.
Write DMA queued	99h	Write DMA queued protocol.
Write DMA queued (Ext)	D9h	Write DMA queued for 48-bit LBA commands.
Write Long	8Fh	PIO Data Out protocol, 512 plus vendor specific bytes, e.g. Write Long

Table 10-7 Vendor Specific Protocol Code (by Protocol Code)

Protocol Code	Protocol	Description
00h	Abort	Abort command. Status =51h and Error = 04h. Command will not be passed to downstream device(s).
80h	PIO Data In (Sectors)	PIO Data In protocol, sector count is given by the Sector Count register.
81h	PIO Data In (Single Sector)	PIO Data In protocol, only one sector, Sector Count is ignored.
82h	PIO Data In (Read Multiple)	PIO Data In protocol for reading blocks of multiple sectors, e.g., Read Multiple.
87h	Read Long	PIO Data In protocol, 512 plus vendor specific bytes, e.g. Read Long.
88h	PIO Data Out (Sectors)	PIO Data Out protocol, sector count is given by the Sector Count register.
89h	PIO Data Out (Single Sector)	PIO Data Out protocol, only one sector, Sector Count is ignored.
8Ah	PIO Data Out (Write Multiple)	PIO Data Out protocol for writing blocks of multiple sectors, e.g., Write Multiple.
8Bh	PIO Data Out (Download Microcode)	PIO Data Out protocol, sector count is given by Sector Number and Sector Count registers.
8Fh	Write Long	PIO Data Out protocol, 512 plus vendor specific bytes, e.g. Write Long
90h	Read DMA	Read DMA protocol.
91h	Read DMA Queued	Read DMA Queued protocol.
98h	Write DMA	Write DMA protocol.
99h	Write DMA queued	Write DMA queued protocol.
A0h	Packet	Packet protocol.
A1h	Service	Service protocol.
B0h	Non-Data	Non-Data protocol.
B1h	Execute Device Diagnostic	Execute Device protocol (for host bridges arranged in master-slave configuration, both will respond regardless of the DEV bit in the Device register.
B2h	Device Reset	Device Reset protocol.
C0h	PIO Data In (Sectors, Ext)	PIO Data In protocol for 48-bit LBA commands, sector count is given by the Sector Count register.
C2h	PIO Data In (Read Multiple, Ext)	PIO Data In protocol for reading blocks of multiple sectors for 48-bit LBA commands, e.g., Read Multiple Ext.
C8h	PIO Data Out (Sectors, Ext)	PIO Data Out protocol for 48-bit LBA commands, sector count is given by the Sector Count register.
CAh	PIO Data Out (Write Multiple, Ext)	PIO Data Out protocol for writing blocks of multiple sectors for 48-bit LBA commands, e.g., Write Multiple Ext
D0h	Read DMA (Ext)	Read DMA protocol for 48-bit LBA commands.
D1h	Read DMA Queued (Ext)	Read DMA Queued for 48-bit LBA commands.
D8h	Write DMA (Ext)	Write DMA protocol for 48-bit LBA commands.
D9h	Write DMA queued (Ext)	Write DMA queued for 48-bit LBA commands.
F0h	Non-Data (Ext)	Non-Data (Ext) protocol.

10.7 Reading and Writing of Task File and Device Control Registers

10.7.1 48-Bit LBA Addressing

The SiI3112A PCI to Serial ATA Controller supports 48-bit LBA. The SiI3112A PCI to Serial ATA Controller does not differentiate a non-extended command (one that does not use 48-bit LBA address) from an extended command (one that uses the 48-bit LBA address). The "expanded" registers can be read with the HOB bit of the Device Control register se to '1'.

10.7.2 Device Control Register and Soft Reset

When the Device Control register is written, a Register FIS for Control will be sent downstream upon one of the following conditions:

- There is a change in the SRST bit, or;
- With SRST bit being '0', there is a change in the NIEN bit.

Note that:

- When the SRST is '1', the NIEN bit in the Register FIS sent is insignificant.
- Any change in the HOB bit will not initiate any Register FIS to be sent. In fact, HOB bit is always '0' in the Register FIS sent.
- If the Serial ATA channel is in PARTIAL or SLUMBER state, a COMWAKE will be automatically initiated to wake up the channel before the Register FIS is sent. However, the channel will stay at the ON state at the end of the operation, even if no soft reset occurs.

A soft reset will do the following:

- Wake up the downstream Serial ATA device from ATA IDLE, STANDBY or SLEEP.

11 FLASH and EEPROM Programming Sequences

11.1 FLASH Memory Access

The SiI3112A supports an external FLASH memory device up to 4 Mbits in capacity. Access to the FLASH memory is available through two means: PCI Direct Access and Register Access.

11.1.1 PCI Direct Access

Access to the Expansion Rom is enabled by setting bit 0 in the Expansion Rom Base Address register at Offset 30h of the PCI Configuration Space. When this bit is set, bits [31:19] of the same register are programmable by the system to set the base address for all FLASH memory accesses. Read and write operations with the FLASH memory are initiated by Memory Read and Memory Write commands on the PCI bus. Accesses may be as Bytes, Words, or DWords.

11.1.2 Register Access

This type of FLASH memory access is carried out through a sequence of internal register read and write operations. The proper programming sequences are detailed below.

FLASH Write Operation

Verify that bit 25 is cleared in the register at Offset 50_H of Base Address 5. The bit reads one when a memory access is currently in progress.

It reads zero when the memory access is complete and ready for another operation.

Program the write address for the FLASH memory access. The address field is defined by bits [18:00] in the FLASH Memory Address – Command + Status register.

Program the write data for the FLASH memory access. The data field is defined by bits [07:00] in the FLASH Memory Data register at Offset 54 of Base Address 5.

Program the memory access type . The memory access type is defined by bit 24 in the FLASH Memory Address – Command + Status register. The bit must be cleared for a memory write access.

Initiate the FLASH memory access by setting bit 25 in the FLASH Memory Address – Command + Status register.

FLASH Read Operation

Verify that bit 25 is cleared in the FLASH Memory Address – Command + Status register at Offset 50_H of Base Address 5. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete and ready for another operation.

Program the read address for the FLASH memory access. The address field is defined by bits [18:00] in the FLASH Memory Address – Command + Status register.

Program the memory access type. The memory access type is defined by bit 24 in the FLASH Memory Address – Command + Status register. The bit must be set for a memory read access.

Initiate the FLASH memory access by setting bit 25 in the FLASH Memory Address – Command + Status register.

Verify that bit 25 is cleared in the FLASH Memory Address – Command + Status register. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete.

Read the data from the FLASH memory access. The data field is defined by bits [07:00] in the FLASH Memory Data register at Offset 54_H of Base Address 5.

11.2 EEPROM Memory Access

The SiI3112A supports an external 256-byte EEPROM memory device. Access to the EEPROM memory is available through internal register operations in the SiI3112A.

EEPROM Write Operation

Verify that bit 25 is cleared in the EEPROM Memory Address – Command + Status register at Offset 58_H of Base Address 5. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete and ready for another operation.

Write '1' to clear bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

Program the write address for the EEPROM memory access. The address field is defined by bits [07:00] in the EEPROM Memory Address – Command + Status register. Program bits [15:08] to zero.

Program the write data for the EEPROM memory access. The data field is defined by bits [07:00] in the EEPROM Memory Data register at Offset $5C_H$ of Base Address 5.

Program the memory access type. The memory access type is defined by bit 24 in the EEPROM Memory Address – Command + Status register. The bit must be cleared for a memory write access.

Initiate the EEPROM memory access by setting bit 25 in the EEPROM Memory Address – Command + Status register.

Poll bit 25 in the EEPROM Memory Address – Command + Status register. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete.

Check bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

EEPROM Read Operation

Verify that bit 25 is cleared in the EEPROM Memory Address – Command + Status register at Offset 58_H of Base Address 5. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete and ready for another operation.

Write '1' to clear bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

Program the read address for the EEPROM memory access. The address field is defined by bits [07:00] in the EEPROM Memory Address – Command + Status register. Program bits [15:08] to zero.

Program the memory access type. The memory access type is defined by bit 24 in the EEPROM Memory Address – Command + Status register. The bit must be set for a memory read access.

Initiate the EEPROM memory access by setting bit 25 in the EEPROM Memory Address – Command + Status register.

Poll bit 25 in the EEPROM Memory Address – Command + Status register. The bit reads one when a memory access is currently in progress. It reads zero when the memory access is complete.

Check bit 28 in the EEPROM Memory Address – Command + Status register. The bit is set if an error occurred during a previous memory access.

Read the data from the EEPROM memory access. The data field is defined by bits [07:00] in the EEPROM Memory Data register at Offset $5C_H$ of Base Address 5.

12 Power Sequencing 1.8V and 3.3V Supplies

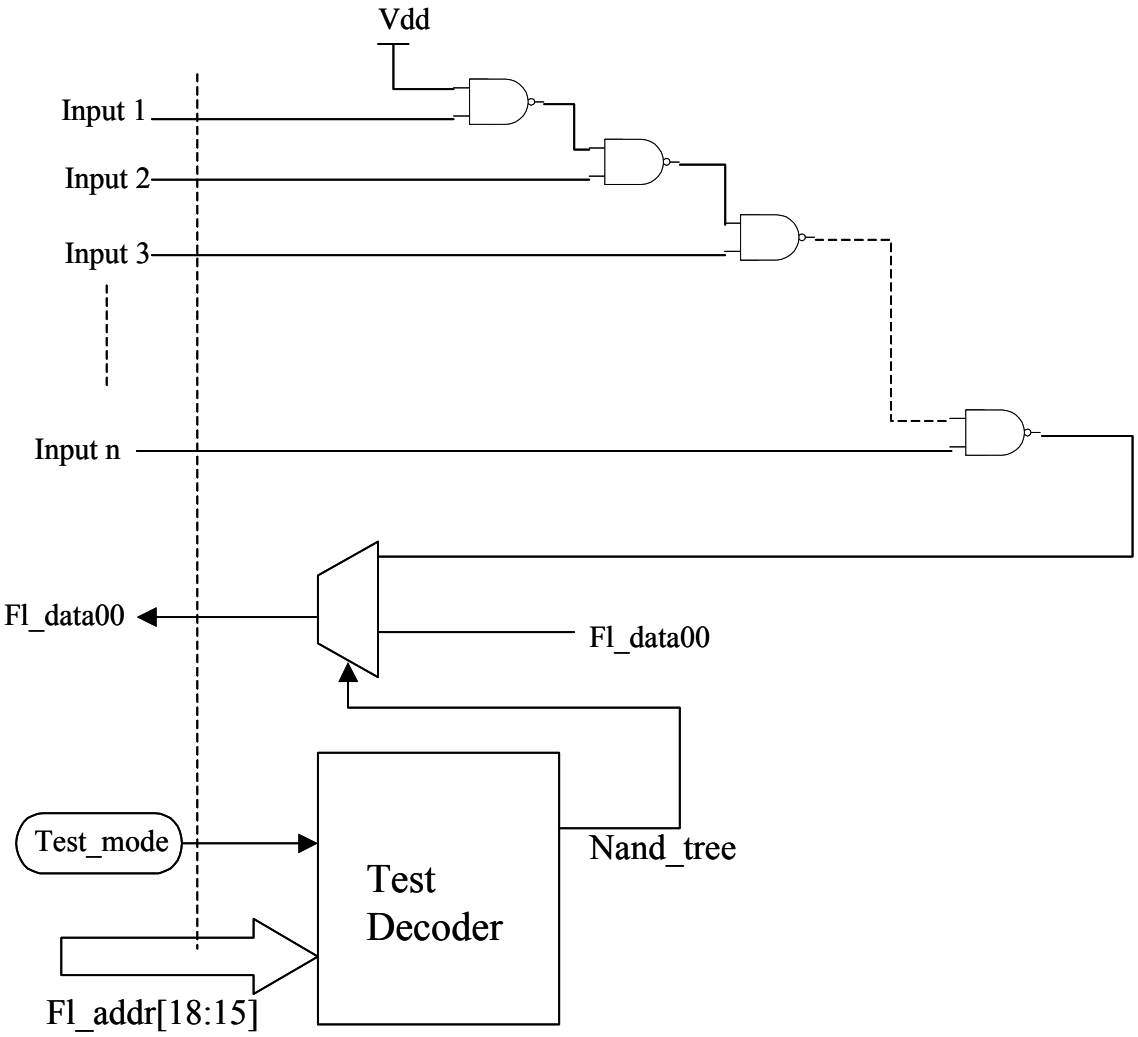
The SiI3112A operates with 1.8V for the digital logic (VDDI) and the analog circuitry (VDDD), and 3.3V (VDDO) supplies for the I/O's. The voltage difference between the 1.8V supply and the 3.3V supplies must never be greater than 2.0V. It is possible for the 1.8V supply to rise faster than the 3.3V supply on power up without violating this rule, as long as the difference never exceeds 2.0V.

Appendix 1 : SiI3112A NAND Tree

A NAND tree is available in the SiI3112A for functional testing of input pins. The NAND tree test mode can be invoked by setting the following signals in the SiI3112A:

Pin Name	Pin Number	Logic State
TEST_MODE	67	1
FL_ADDR[18]	66	0
FL_ADDR[17]	65	0
FL_ADDR[16]	64	1
FL_ADDR[15]	63	0

The NAND tree is shown in the following diagram:



The test decoder generates the nand_tree signal. This signal performs the following functions:

a) Drives the enable pins of all the bi-directional I/Os and set them in input mode. The only exception is the fl_data00 pin, which is used as the output for the NAND tree.
b) Drives the output multiplexer to direct the output of the NAND tree to the fl_data00 pin.

All the input cells and bidirectionals (except fl_data00) are connected to the NAND tree. The following table lists the order of inputs by pin name and number.

Order	Pin Number	Pin Name
1	143	MEM_CS_N
2	142	PCI_AD00
3	141	PCI_AD01
4	140	PCI_AD02
5	139	PCI_AD03
6	138	PCI_AD04
7	137	PCI_AD05
8	136	PCI_AD06
9	135	PCI_AD07
10	134	PCI_CBE0
11	133	PCI_AD08
12	132	PCI_AD09
13	131	PCI_M66EN
14	130	PCI_AD10
15	127	PCI_AD11
16	126	PCI_AD12
17	125	PCI_AD13
18	124	PCI_AD14
19	123	PCI_AD15
20	122	PCI_CBE1
21	121	PCI_PAR
22	117	PCI_TRDY_N
23	116	PCI_DEVSEL_N
24	115	PCI_STOP_N
25	114	PCI_PERR_N
26	113	PCI_IRDY_N
27	112	PCI_FRAME_N
28	111	PCI_CBE2
29	110	PCI_AD16
30	107	PCI_AD17
31	106	PCI_AD18
32	105	PCI_AD19
33	104	PCI_AD20
34	103	PCI_AD21
35	102	PCI_AD22
36	101	PCI_AD23
37	100	PCI_IDSEL
38	97	PCI_CBE3
39	96	PCI_AD24
40	95	PCI_AD25
41	94	PCI_AD26
42	93	PCI_AD27
43	92	PCI_AD28
44	91	PCI_AD29
45	90	PCI_AD30
46	89	PCI_AD31
47	85	PCI_GNT_N
48	84	PCI_CLK
49	83	PCI_RST_N

Order	Pin Number	Pin Name
50	77	FL_DATA[07]
51	76	FL_DATA[06]
52	75	FL_DATA[05]
53	74	FL_DATA[04]
54	71	FL_DATA[03]
55	70	FL_DATA[02]
56	69	FL_DATA[01]
57	62	FL_ADDR[14]
58	61	FL_ADDR[13]
59	60	FL_ADDR[12]
60	59	FL_ADDR[11]
61	58	FL_ADDR[10]
62	55	FL_ADDR[09]
63	54	FL_ADDR[08]
64	53	FL_ADDR[07]
65	52	FL_ADDR[06]
66	51	FL_ADDR[05]
67	50	FL_ADDR[04]
68	49	FL_ADDR[03]
69	48	FL_RD_N
70	45	FL_WR_N
71	44	FL_ADDR[02]
72	43	FL_ADDR[01] / BA5_EN
73	42	FL_ADDR[00] / IDE_CFG
74	41	EEPROM_SCLK
75	40	EEPROM_SDAT