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# PCI0643

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## Bus Master DMA PCI-IDE Chip Specification

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# Table of Contents

<b>1</b>	<b>Chip Structure</b>	<b>1</b>
1.1	Pin Descriptions	1
1.2	Register Definition	7
1.2.1	Standard Configuration Header	7
1.2.2	Base Address Registers	7
1.2.3	Status/Command Register (04h)	8
1.2.4	Configuration Registers	9
1.2.5	IDE Timing Control Registers	9
1.3	PCI Master Control Registers	12
1.4	Active Count Function	15
1.5	Recovery Count Function	15
1.6	Task File Registers	16
1.7	Configuration Setup	16
1.7.1	Notes	16
1.7.2	Configuration Mechanism #2	16
1.8	PIO Mode Interrupt Processing	16
1.9	DMA Programming	17
1.10	Read Ahead Operation	17
1.11	PCI0643 IDE Controller Pinout	18
1.11.1	Host Interface Pinout	18
1.11.2	Drive Interface Pinout	19
1.11.3	VDD/VSS Pins	20
1.12	Pinout Diagram	21
1.13	Jumper Settings	21
<b>2</b>	<b>Power Specifications</b>	<b>23</b>
2.1	DC Specifications	23
2.1.1	Maximum Ratings	23
2.1.2	Recommended Operating Conditions (Vss = 0V)	23
2.2	DC Characteristics	23
2.3	AC Specifications	24
2.3.1	Timing Waveform	24
2.3.2	Clock Timing	24
2.3.3	Host Interface Timing (loading = 50 pf)	24
2.3.4	IDE Drive Timing (loading = 75 pf)	24
2.3.5	IDE Drive Timing (loading = 120 pf)	25
2.4	Output Test Load	25
2.5	IDE Write Timing	25
2.6	Host Read/Write Timing	26

2.7 PCI Read/Write Timing in Target Mode	26
2.8 IDE Timing	27
2.9 PCI DMA Master Read Timing (33MHz PCICLK)	28
2.10 PCI DMA Master Write Timing (33MHz PCICLK)	29

# 1 Chip Structure

## 1.1 Pin Descriptions

The following is an alphabetical listing of PCI mode signals and their pin assignments. A numerically sorted pinout may be found on page 18. Please refer to the PCI mode pinout diagram for the locations of the pins.

Signal	Pin	Type
2NDIDEEN#/DMACK0#	87	B/T

### Function

This signal normally is used in response to DMARQ0 to either acknowledge that data has been accepted, or that data is available. At power-up reset, the state of this signal is used to enable or disable the secondary channel.

Signal	Pin	Type
2NDIOR#	77	T/O

### Function

Secondary Channel Disk IO Read is an active low output which enables data to be read from the drive. The duration and repetition rate of DIOR# cycles is determined by PCI0643 programming. DIOR# is driven high when inactive.

Signal	Pin	Type
2NDIOW#	78	T/O

### Function

Secondary Channel Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition rate of DIOW# cycles is determined by PCI0643 programming. DIOW# is driven high when inactive.

Signal	Pins	Type
AD[31..0]	7-14, 17-20, 23-26, 28-35, 42-49	B/T

### Function

Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME # is asserted. During the address phase AD[31..0] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. During data phases AD[7..0] contain the least significant byte (lsb) and AD[31..24] contain the most significant byte (msb). Write data are stable and valid when IRDY# is asserted and read data are stable and valid when TRDY# is asserted. Data are transferred during those clocks where both IRDY# and TRDY# are asserted.

Signal	Pins	Type
C/BE[3..0]#	3-6	B/T

### Function

Byte Enable bits 0 through 3 form the host CPU address bus. These inputs are active low and specify which bytes will be valid for master read/write data transfers.



Signal	Pin	Type
DMACK1#	88	B/T

**Function**

This signal normally is used in response to DMARQ1 to either acknowledge that data has been accepted, or that data is available.

Signal	Pin	Type
DCHRDY	76	IN

**Function**

Drive Channel Ready is an active high input that indicates that the IDE disk drive has completed the current command cycle. A 1K-ohm pull-up resistor is recommended.

Signal	Pins	Type
DCS0#	55	O

**Function**

Drive Chip Select for 1Fx.

Signal	Pins	Type
DCS1#	56	O

**Function**

Drive Chip Select for 3F6.

Signal	Pin	Type
DCS2#	80	O

**Function**

Drive Chip Select 2 is used to select the second IDE port command registers in the drive.

Signal	Pin	Type
DCS3#	79	O

**Function**

Drive Chip Select 3. Used to select second IDE port auxiliary register.

Signal	Pin	Type
DEVSEL#	93	S/T/S

**Function**

Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.

Signal	Pin	Type
TEST1#	61	I

**Function**

This pin is used with TEST0 when PCIMODE = 0 to select different DC tests for this chip.



Signal	Pin	Type
DIOR#	57	T/O

**Function**

Primary Channel Disk IO Read is an active low output which enables data to be read from the drive. The duration and repetition rate of DIOR# cycles is determined by PCI0643 programming. DIOR# is driven high when inactive.

Signal	Pin	Type
DLOW#	58	T/O

**Function**

Primary Channel Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition rate of DLOW# cycles is determined by PCI0643 programming. DLOW# is driven high when inactive.

Signal	Pin	Type
DIRQ1	75	I

**Function**

Disk Interrupt is an input to the PCI0643 used to generate the IRQ14 output when the primary IDE channel is in legacy mode. When the primary IDE channel is in native mode, this pin generates the INTA# output. DIRQ1 is asserted low then high by the drive at the beginning of a block transfer. This input should have a 1K pull-down resistor connected to it.

Signal	Pin	Type
DIRQ2	86	I

**Function**

Disk Interrupt is an input to the PCI0643 used to generate the IRQ15 output when the secondary IDE channel is in legacy mode. When the secondary IDE channel is in native mode, this pin generates the INTA# output. DIRQ2 is asserted low then high by the drive at the beginning of a block transfer. This input should have a 1K pull-down resistor connected to it.

Signal	Pin	Type
DMARQ0	94	I

**Function**

This signal is used in a handshake manner with DMACK0#, and shall be asserted HIGH by the primary drive when it is ready to transfer data to or from the host.

Signal	Pin	Type
DMARQ1	60	I

**Function**

This signal is used in a handshake manner with DMACK1# and shall be asserted HIGH by the secondary drive when it is ready to transfer data to or from the host.



Signal	Pin	Type
DRST#	59	O

**Function**

Disk ReSeT is an active low output which signals the IDE drive(s) to initialize its control registers. DRST# is a buffered version of the RESET# input and connects directly to the ATA connector.

Signal	Pins	Type
DSA[0]	68	O
DSA[1]	69	B/T
DSA[2]	70	O

**Function**

Disk Address bits 0 through 2 are normally outputs to the ATA connector for register selection in the drive(s). These signals are decoded from the AD[2] and C/BE[3..0] inputs. DSA[1] is also sampled as an input on the falling edge of RESET#. DSA[1] has an internal pull-up resistor. A 1k resistor is recommended where pull-down is required. (See "Jumper Settings" on page 21.)

Signal	Pins	Type
DSD[15..0]	36-39, 50-53, 62-65, 71-74	B/T

**Function**

Disk Data bits 0 through 15 are the 16-bit bi-directional data bus which connects to the IDE drive(s). DSD[7..0] define the lowest data byte while DSD[15..8] define the most significant data byte. The DSD bus is normally in a high-impedance state and is driven by the PCI0643 only during the DIOW# command pulse.

Signal	Pin	Type
ENIDE	21	I

**Function**

ENable IDE is an active high input that controls the PCI0643's default disk operation mode following reset. When set low, the PCI0643's IDE cycles are disabled following reset. This mode allows software to scan for system hardware and enable the PCI0643 via the PCICMD register (index 4). When left floating or pulled high, the PCI0643 is enabled and cannot be disabled via software.

Signal	Pin	Type
FRAME #	98	S/T/S

**Function**

Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME # is asserted to indicate a bus transaction is beginning. While FRAME # is asserted, data transfers continue. When FRAME # is deasserted, the transaction is in the final data phase.

Signal	Pin	Type
IDSEL	100	I

**Function**

Initialization Device Select is used as a chip select during configuration read and write transactions.

Signal	Pin	Type
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INTA#	84	O/D
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**Function**

Interrupt A is used to request an interrupt in PCI IDE Native Mode. INTA# is open collector and is pulled up when both IDE ports are in Legacy Mode.

<b>Signal</b>	<b>Pin</b>	<b>Type</b>
IRDY#	99	S/T/S

**Function**

Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.

<b>Signal</b>	<b>Pin</b>	<b>Type</b>
IRQ14	22	T/O

**Function**

IRQ14 is used to request an interrupt in PCI IDE Legacy Mode. (For PC-AT compatibles.) IRQ14 is tri-stated when IDE port 0 is in Native Mode.

<b>Signal</b>	<b>Pin</b>	<b>Type</b>
IRQ15	83	T/O

**Function**

IRQ15 is used to request an interrupt for secondary IDE port in PCI IDE Legacy Mode. (PC-AT compatible.) IRQ15 is tri-stated when IDE port 1 is in Native Mode.

<b>Signal</b>	<b>Pin</b>	<b>Type</b>
PAR	96	B/T

**Function**

PAR is even parity across AD[31..0] and C/BE[3..0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31..0] but delayed by one clock.)

<b>Signal</b>	<b>Pin</b>	<b>Type</b>
PCICLK	89	I

**Function**

Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RESET and IRQ, are sampled on the rising edge of PCICLK, and all other timing parameters are defined with respect to this edge.

<b>Signal</b>	<b>Pin</b>	<b>Type</b>
PCIGNT#	82	I

**Function**

This signal indicates to the agent that access to the PCI bus has been granted.

<b>Signal</b>	<b>Pin</b>	<b>Type</b>
PCIMODE	2	I

**Function**

PCIMODE is set to high when chip is used in PCI bus.

Signal	Pin	Type
PCIREQ#	81	T/O

**Function**

This signal indicates to the arbiter that this agent desires use of the PCI bus.

Signal	Pin	Type
PERR#	95	S/T/S

**Function**

Error may be pulsed active by an agent that detects a parity error. PERR# can be used by any agent to signal data corruptions. However, on detection of a PERR# pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies that the system will be unable to continue operation once error processing is complete.

Signal	Pin	Type
RESET#	1	I

**Function**

RESET# is an active low input that is used to set the internal registers of the PCI0643 to their initial state. RESET# is typically the system power-on reset signal as distributed on the PCI bus.

Signal	Pin	Type
STOP#	97	S/T/S

**Function**

STOP# indicates the current target is requesting the master to stop the current transaction.

Signal	Pin	Type
TEST0	85	I

**Function**

This pin is used with TEST1# when PCIMODE = 0 to select different DC tests for this chip.

Signal	Pin	Type
TRDY#	92	S/T/S

**Function**

Target Ready indicates the target agent's ability to complete the current data phase of the transaction. TRDY# is used with IRDY#. A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD(31..0). During a write, it indicates the target is prepared to accept data.



Signal	Pins	Type
VDD	16, 41, 67, 91	I
<b>Function</b>		
Positive power supply input.		

Signal	Pins	Type
VSS	15, 27, 40, 54, 66, 90	I
<b>Function</b>		
Ground reference power supply input.		

## 1.2 Register Definition

### 1.2.1 Standard Configuration Header

31	16	15	0	
Device ID = 0643		Vendor ID = 1095h		00h
Status		Command		04h
Class-code = 01018Ah		Revision ID=00h		08h
BIST = 00000000b	Header Type = 00000000b	Latency Time = 00000000b	Cache Line Size = 00000000b	0Ch

### 1.2.2 Base Address Registers

Base-Address 0 29 valid bits IDE CS0 (I/O map) Default I/O Range = 000001F0h-000001F7h			Bit 2:0 = 001b	10h
Base-Address 1 30 valid bits IDE CS1 (I/O map) Default I/O Range = 000003F4h-000003F7h			Bit 1:0 = 01b	14h
Base-Address 2 29 valid bits IDE CS2 (I/O map) Default I/O Range = 00000170h-00000177h			Bit 2:0 = 001b	18h
Base-Address 3 30 valid bits IDE CS3 (I/O map) Default I/O Range = 00000374h-00000377h			Bit 1:0 = 01b	1Ch
Base-Address 4 28 valid bits PCI Bus Master/DMA Registers & IDE Timing CNT REGS			Bit 3:0 = 0001b	20h
Base Address 5 Not used — return zero				24h
ROM Expansion Not Used — return zeros				30h
Max_lat = 00000100b	Min_Gnt = 000000010b	Interrupt Pin = 00000001b	Interrupt Line = 00000000b	3Ch

### 1.2.3 Status/Command Register (04h)

Bit	Read/Write	Description
0	R/W	Controls the response to the I/O space specified in the Base Address Register. Default value is determined by the ENIDE pin. 1—chip enable 0—chip disable
1	R	Memory space access enable 0—disable
2	R/W	Bus Master enable. Default is disable. 1—enable 0—disable
3	R	Special cycle response 0—disable
4	R	Invalidate command 0—disable
5	R	VGA 0—
6	R/W	Parity error response 0—ignore the parity error
7	R	Address and DATA stepping 0—address/data stepping disable
8	R	PCI signal SERR# driver enable 0—disable
9	R	Fast back-to-back transfer 0—disable
23	R	Fast back-to-back capable 1—enable
24	R/W	Master Data Parity Error Detected 0—no action 1—reset
25- 26	R	Devscl Timing 01—medium timing
27	R	Target Abort 0—
28	R/W	Received Target Abort 1—reset 0—no action
29	R/W	Received Master Abort 1—reset 0—no action
30	R	Signaled SERR# (Master or Slave) 0—
31	R/W	Slave Data Parity Error Detected 1—reset 0—no action

All other bits are not implemented and will be read back with all zeros.



### 1.2.4 Configuration Registers

Name	Function	Index
PROGIF	Programming interface = 80h (RO) when DSA1 is pulled down at reset = 8Ah (RW) when DSA1 is not pulled down at reset. Bits 0-3 are used to toggle between Legacy and Native Modes  See the PCI SIG's PCI IDE Controller Specification Rev. 0.9 for a detailed description.	9
Name	Function	Index
INTLINE	Interrupt Line (R/W) Default = 14 (0Eh)	3Ch

### 1.2.5 IDE Timing Control Registers

Name	Function	Index
CFR	Configuration (R)	50h
<b>Bits</b>		
6	DSA1 Jumper 0—Disable Base address register; R=0 1—Enable Base address register R/W	
2	IDE drive 0/1 interrupt status Read CFR will clear this bit 0—no interrupt pending 1—interrupt pending	
Name	Function	Index
CNTRL	Drive 0/1 Control Register (RW)	51h
<b>Bits</b>		
7	Drive 1 read ahead control register 0—enable 1—disable	
6	Drive 0 read ahead control register 0—enable 1—disable	
3	Second channel control (default value determined by 2NDIDEEN# jumper) 0—disable 1—enable	
Name	Function	Index
CMDTIM	IDE Task File Timing Control Register (RW) All four devices on both channels use the same command timing.	52h
<b>Bits</b>		
7-4	IOR/IOW active count	
3-0	IOR/IOW recovery count	



Name	Function	Index
ARTTIM0	Drive 0 Address Setup Register (RW)	53h
<b>Bits</b>		
7-6	Address setup time count	
	00—4 clocks	
	01—2 clocks	
	10—3 clocks	
	11—5 clocks	

**Note**

Whichever has the higher count between ARTTIM0 and ARTTIM1 will be selected for the primary channel.

Name	Function	Index
DRWTIM0	Drive 0 Data Read/Write or DACK Timing Register (RW)	54h
<b>Bits</b>		
7-4	Active count	
3-0	Recovery count	

Name	Function	Index
ARTTIM1	Drive 1 Address Setup Register (RW)	55h
<b>Bits</b>		
7-6	Address setup time count	
	00—4 clocks	
	01—2 clocks	
	10—3 clocks	
	11—5 clocks	

**Note**

Whichever has the higher count between ARTTIM0 and ARTTIM1 will be selected for the primary channel.



Name	Function	Index
DRWTIM1	Drive 1 Data Read/Write or DACK Timing Register (RW)	56h
<b>Bits</b>		
7-4	Active count	
3-0	Recovery count	
Name	Function	Index
ARTTIM23	Drive 2/3 Control/Status Register (RW)	57h
<b>Bits</b>		
7-6	Drive 2/3 Address Setup Count Register	
5	Reserved	
4	IDE drive 2/3 interrupt status Read ARTTIM23 will clear this bit 0—no interrupt pending 1—interrupt pending	
3	Drive 3 read ahead 0—enable 1—disable (default)	
2	Drive 2 read ahead 0—enable 1—disable (default)	
1-0	Reserved	
Name	Function	Index
DRWTIM2	Drive 2 Data Read/Write or DACK Timing Register (RW)	58h
<b>Bits</b>		
7-4	Active count	
3-0	Recovery count	
Name	Function	Index
BRST	Read Ahead Count Register (R/W) Default = 40h  This value equals the read-ahead count in quad words. Example: 40h x 8 = 200h (512) bytes	59h
Name	Function	Index
DRWTIM3	Drive 3 Data Read/Write or DACK Timing Register (RW)	5Bh
<b>Bits</b>		
7-4	Active count	
3-0	Recovery count	

### 1.3 PCI Master Control Registers

These registers can be addressed through either the offset of Base Address #4 or the PCI configuration space.

Name	Function	Index
BMIDECR0	Bus Master IDE Command Register 0 for Primary IDE Channel. (R/W)	PCI Configuration Space 70h or Base Address #4 + 00h

#### Bit

7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Read or Write Control 0—PCI bus master reads are performed 1—PCI bus master writes are performed
2	Reserved
1	Reserved
0	Start/Stop Bus Master 0—disable bus master operation 1—enable bus master operation

Name	Function	Index
MRDMODE	DMA Master Read Mode Select (W)	PCI Configuration Space 71h or Base Address #4 + 01h

#### Bits

1,0	Bit 1	Bit 0	Mode
	0	0	Memory Read (Default)
	0	1	Memory Read Multiple
	1	x	Memory Read Line





Name	Function	Index
BMIDESR0	Bus Master IDE Status Register 0 for IDE Primary Channel (R/W)	PCI Configuration Space 72h or Base Address #4 + 02h
<b>Bit</b>		
7	Simplex only (R)	
6	Drive 1 DMA Capable 0—no DMA capability 1—DMA capability	
5	Drive 0 DMA capable 0—no DMA capability 1—DMA capability	
4	Reserved	
3	Reserved	
2	Interrupt 0—no interrupt occurs on IDE bus 1—interrupt generated on IDE bus (software writes 1 to clear bit)	
1	Errors 0—no error 1—error (write 1 to clear error)	
0	Bus Master IDE Active 0—all data transfer completely 1—data transfer not complete	
<b>Name</b>	<b>Function</b>	<b>Index</b>
DTPR0	Descriptor Table Pointer Register 0 for IDE Primary Channel (R/W) 4 bytes	PCI Configuration Space 74h or Base Address #4 + 04h
<b>Bit</b>		
31-2	Base address of descriptor table	
1-0	Reserved	



Name	Function	Index
BMIDECR1	Bus Master IDE Command Register 1 for Second Channel (R/W)	PCI Configuration Space 78h or Base Address #4 + 08h

**Bit**

7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Read or Write Control 0—PCI bus master reads are performed 1—PCI bus master writes are performed
2	Reserved
1	Reserved
0	Start/Stop Bus Master 0—disable bus master operation 1—enable bus master operation

Name	Function	Index
BMIDESR1	Bus Master IDE Status Register 0 for Second Channel (R/W)	PCI Configuration Space 7Ah or Base Address #4 + 0Ah

**Bit**

7	Simplex only (R)
6	Drive 3 DMA Capable 0—no DMA capability 1—DMA capability
5	Drive 2 DMA capable 0—no DMA capability 1—DMA capability
4	Reserved
3	Reserved
2	Interrupt 0—no interrupt occurs on IDE bus
1	Errors 0—no error 1—error (write 1 to clear error)
0	Bus Master IDE Active 0—all data transfer completely 1—data transfer not complete

Name	Function	Index
DTPR1	Descriptor Table Pointer Register 1 for Second Channel (R/W) 4 bytes	PCI Configuration Space 7Ch or Base Address #4 + 0Ch

**Bit**

31-2	Base address of descriptor table
1-0	Reserved

## 1.4 Active Count Function

Active Count	R/W Active Time
0000	16 clocks
0001	1 clock
0010	2 clocks
0011	3 clocks
0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	13 clocks
1110	14 clocks
1111	15 clocks

## 1.5 Recovery Count Function

Recovery Count	Read/Write Recovery Time
0000	16 clocks
0001	2 clocks
0010	3 clocks
0011	4 clocks
0100	5 clocks
0101	6 clocks
0110	7 clocks
0111	8 clocks
1000	9 clocks
1001	10 clocks
1010	11 clocks
1011	12 clocks
1100	13 clocks
1101	14 clocks
1110	15 clocks
1111	1 clock

## 1.6 Task File Registers

Name	Host Addr	Function
HDATA*	1F0(170)	data register (RW)
HDWPC	1F1(171)	write pre-comp (WO)
HDERR	1F1(171)	error register (RO)
HDSCCT	1F2(172)	sector count (RW)
HDSSN	1F3(173)	starting sector # (RW)
HDCLL	1F4(174)	cylinder low (RW)
HDCLH	1F5(175)	cylinder high (RW)
HDS DH	1F6(176)	SDH (RW)
HDCMD	1F7(177)	command (WO)
HDSTT	1F7(177)	status (RO)
HDFDR	3F6(376)	fixed disk control auxiliary register (WO)
HDASR	3F6(376)	alternate status auxiliary register (RO)

\*HDATA can be accessed as a 16- or 32-bit-wide register, for all commands.

## 1.7 Configuration Setup

Depending on your motherboard chip set, either Configuration Mechanism #1 or Configuration Mechanism #2 is applicable. Configuration Mechanism #2 is described below. For Configuration #1 methodology, refer to the PCI Spec 2.1.

### 1.7.1 Notes

- 1) Although PCI BIOS (INT 1Ah) is a portable alternative to mechanism #1 and #2, it is not recommended because MS-DOS's EMM386.SYS causes the system to hang when function FIND PCI DEVICE is accessed
- 2) The PCI0643 supports byte, word, and dword reads/writes of configuration space.

### 1.7.2 Configuration Mechanism #2

- 1) Enter PCI Configuration Mode by writing 10h to port CF8h.
- 2) Scan the PCI device IDs from 0h to Fh for the presence of a PCI0643 controller. (There should be 1095h in port Cx00h and 0643h in port Cx02h, where x=device ID.)
- 3) To read or write internal registers, read or write to port Cxyyh, where x=device ID from (2) and yy=configuration register's index.
- 4) Exit PCI Configuration Mode by writing 00 to port CF8h.

## 1.8 PIO Mode Interrupt Processing

When DSA1 is pulled low during reset, both IDE ports are in PCI IDE Legacy Mode. When DSA1 has no pull-down during reset, each IDE port may independently be set to PCI IDE Legacy Mode or Native Mode via the Programming Interface Byte (configuration register PROGIF, Index 9h).

When an IDE port is in PCI IDE Legacy Mode, the PCI0643 is compatible with standard ISA IDE. The IDE task file registers are mapped to the standard ISA port addresses, and IDE drive interrupts occur at IRQ14 (primary) or IRQ15 (secondary).

When an IDE port is in PCI IDE Native Mode, the IDE task file registers may be mapped to non-standard port addresses, and IDE drive interrupts occur at PCI INTA. Therefore, if both IDE ports are in PCI IDE Native Mode, drive interrupts from both IDE ports are multiplexed into PCI INTA. In this case, the interrupt status bits must be polled to determine which IDE port generated the interrupt, or whether the interrupt was generated by another PCI device sharing INTA on the bus.

- 1) The host reads CFR (index 50h). If bit 2 is set, then the interrupt occurred on the primary IDE port.
- 2) The host reads ARTTIM23. If bit 4 is set, then the interrupt occurred on the secondary IDE port.
- 3) If 1) and 2) are both false, then the interrupt was generated by another PCI device sharing INTA with the PCI0643.

## 1.9 DMA Programming

See Revision 1.0 of Intel's "Programming Interface for Bus Master IDE Controller" for information about bus master DMA programming.

## 1.10 Read Ahead Operation

The chip will snoop the IDE command register. If a read or read multiple command is written to it, then the chip will load the readahead count according to the current BRST register (index 59h) setting.

## 1.11 PCI0643 IDE Controller Pinout

### 1.11.1 Host Interface Pinout

Name	Pin #	Type	Function
RESET#	1	I	Reset input
PCIMODE	2	I	Tied HIGH if PCI mode
C/BE<3>#	3	B/T	
C/BE<2>#	4	B/T	
C/BE<1>#	5	B/T	
C/BE<0>#	6	B/T	
AD<31>	7	B/T	
AD<30>	8	B/T	
AD<29>	9	B/T	
AD<28>	10	B/T	
AD<27>	11	B/T	
AD<26>	12	B/T	
AD<25>	13	B/T	
AD<24>	14	B/T	
AD<23>	17	B/T	
AD<22>	18	B/T	
AD<21>	19	B/T	
AD<20>	20	B/T	
ENIDE	21	I	Enable chip operation
IRQ14	22	T/O	Tri-state output to interrupt 14 (PC-AT compatible)
AD<19>	23	B/T	
AD<18>	24	B/T	
AD<17>	25	B/T	
AD<16>	26	B/T	
AD<15>	28	B/T	
AD<14>	29	B/T	
AD<13>	30	B/T	
AD<12>	31	B/T	
AD<11>	32	B/T	
AD<10>	33	B/T	
AD<9>	34	B/T	
AD<8>	35	B/T	
AD<7>	42	B/T	
AD<6>	43	B/T	
AD<5>	44	B/T	
AD<4>	45	B/T	
AD<3>	46	B/T	
AD<2>	47	B/T	
AD<1>	48	B/T	
AD<0>	49	B/T	
TEST1#	61	I	Select DC test
PCIREQ#	81	T/O	



Name	Pin #	Type	Function
PCIGNT#	82	I	
IRQ15	83	T/O	To interrupt 15 (PC-AT compatible)
INTA#	84	O/D	Interrupt request to PCI host
TEST0	85	I	Select DC test.
PCICLK	89	I	Clock input
TRDY#	92	S/T/S	
DEVSEL#	93	S/T/S	
PERR#	95	S/T/S	
PAR	96	B/T	
STOP#	97	S/T/S	
FRAME#	98	S/T/S	
IRDY#	99	S/T/S	
IDSEL	100	I	

### 1.11.2 Drive Interface Pinout

PCI	Pin #	Type	Function
DSD<15>	36	B/T	
DSD<14>	37	B/T	
DSD<13>	38	B/T	
DSD<12>	39	B/T	
DSD<11>	50	B/T	
DSD<10>	51	B/T	
DSD<9>	52	B/T	
DSD<8>	53	B/T	
DCSO#	55	O	Drive chip select for 1Fx
DCS1#	56	O	Chip select for 3F6
DIOR#	57	T/O	Drive IOR#
DIOW#	58	T/O	Drive IOW#
DRST#	59	O	Drive Reset
DMARQ1	60	I	
DSD<7>	62	B/T	
DSD<6>	63	B/T	
DSD<5>	64	B/T	
DSD<4>	65	B/T	
DSA<0>	68	O	Drive address 0
DSA<1>	69	B/T	Drive address 1. Select "Compatibility Mode" (Legacy) or "Native Mode" at power-up.
DSA<2>	70	O	Drive address 2
DSD<3>	71	B/T	
DSD<2>	72	B/T	
DSD<1>	73	B/T	
DSD<0>	74	B/T	
DIRQ1	75	I	Drive IRQ
DCHRDY	76	I	Drive channel ready
2NDIOR#	77	T/O	IOR# for the secondary IDE port
2NDIOW#	78	T/O	IOW# for the secondary IDE port



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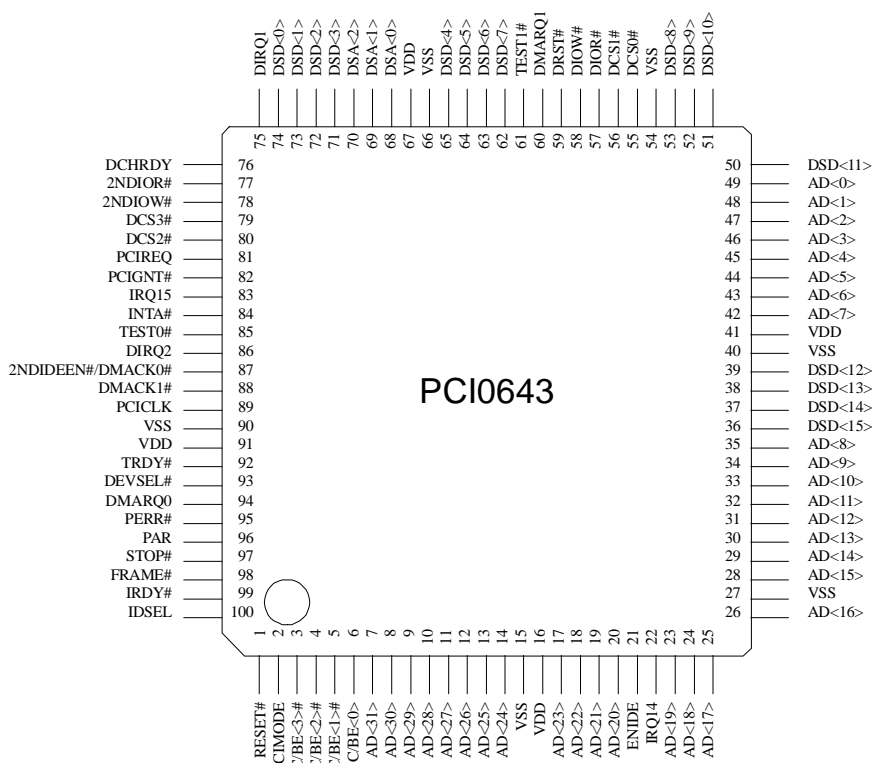
PCI	Pin #	Type	Function
DCS3#	79	O	Drive chip select for 376
DCS2#	80	O	Drive chip select for 17x
DIRQ2	86	I	
2NDIDEEN#/ DMACK0#	87	B/T	
DMACK1#	88	B/T	
DMARQ0	94	I	

### 1.11.3 VDD/VSS Pins

VDD Pins	VSS Pins
16	15
41	27
67	40
91	54
	66
	90



## 1.12 Pinout Diagram



## 1.13 Jumper Settings

- DSA1**      0—Disable Base Address Registers. Base Address Registers always return 0. Primary channel uses IRQ14. Secondary channel uses IRQ15. IDE task file registers are mapped to the default port addresses of 1Fx (primary) and 17x (secondary).
- 1—Enable Base Address Registers. Base Address Registers respond as defined in PCI IDE spec 0.6 under control of PROGIF register. (See page 9.)

**NOTE:**    0 = 1K pull-down  
              1 = no pull-down



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## 2 Power Specifications

### 2.1 DC Specifications

#### 2.1.1 Maximum Ratings

Symbol	Parameter	Limits	Units
VDD	DC supply voltage	-0.3 to +4.6	Volts
Vin	DC Input Voltage	-0.3 to 5.5	Volts
Stg	Storage Temperature	-55 to +125	Deg. C
Iin	DC Input Current	±10	µA

#### 2.1.2 Recommended Operating Conditions (Vss = 0V)

Symbol	Parameter	Min	Max	Units
VDD	DC supply voltage	3.0	3.6	Volts
Vin	Input Voltage	VSS	VDD	Volts
Topr	Operating Temperature	0	+70	Deg. C

### 2.2 DC Characteristics

(For VDD= 3.3V, 0 to 70 Deg. C)

Symbol	Parameter	Min	Max	Units	Notes
VIL	Input Voltage Low	-0.3	0.8	Volts	Note 2
VIH	Input Voltage High	2.0	5.5	Volts	Note 2
VOL	Output Voltage Low		0.40	Volts	Note 3
VOH	Output Voltage High	2.4		Volts	
ILO	Output Leakage Current	-10	10	UA	
ILI	Input High Leakage Current Vin = VDD	-10	10	UA	Note 1
IIL	Input Low Leakage Current Vin = VSS	-10	10	UA	Note 1
CIN	Input or I/O Capacitance		10	PF	

#### Notes

All PCI signals are PCI-compliant driver pins. See specification.

DCHRDY, DIRQ1, DIRQ2, DMARQ0, DMARQ1 and DSD[0..15] are TTL Schmitt trigger pins.

IOL = 16mA: DCS3#, DCS2#, IRQ14, IRQ15, DRST#, CS0#, CS1#, DSA[0..2], DIOR#, DIOW#, 2NDIOR#, 2NDIOW#, DSD[0..15], DMACK0# and DMACK1#.

## 2.3 AC Specifications

### 2.3.1 Timing Waveform

All AC timing is measured from the 0.8V and 2.0V on the source signal to the 0.8V and 2.0V level on the signal under test.

### 2.3.2 Clock Timing

Parameter	Min	Max	Units
CLK Frequency	0	40	MHz
CLK Period	25		ns
CLK High Time	10		ns
CLK Low Time	10		ns
CLK Rise Time		2	ns
CLK Fall Time		2	ns

### 2.3.3 Host Interface Timing (loading = 50 pf)

Signal		Min (ns)	Max (ns)
FRAME#, IRDY#, TRDY#, CBE#, AD[0..31], STOP#, PAR, PERR#, DEVSEL#, IDSEL, PCIGNT#	Setup time to CLK high	7	
DEVSEL#, FRAME#, STOP#, IRDY#, TRDY#, PAR, PERR#, PCIREQ#	High to low from CLK high	4	11
	Low to high from CLK high	3	10
AD[0..31]	Read delay from CLK high in Target mode	4	11
AD[0..31]	Active to float delay from CLK high	8	28
AD[0..31], CBE#	Write delay from CLK high in Master mode	4	11

### 2.3.4 IDE Drive Timing (loading = 75 pf)

Signal		Min (ns)	Max (ns)
DCS0#, DCS1#, DSA[0..2]	High to low from CLK high	6	21
	Low to high from CLK high	5	18
DIOR#, DIOW#	High to low from CLK high	5	18
	Low to high from CLK high	4	15
DSD to DIOW# (2 CLKS)	Low to high setup time	45	56
	Hold time	50	57
DCS0# low to DIOW#, DIOR# low for port 1F0h		52	59
IOCHRDY to CLK high setup time		2	

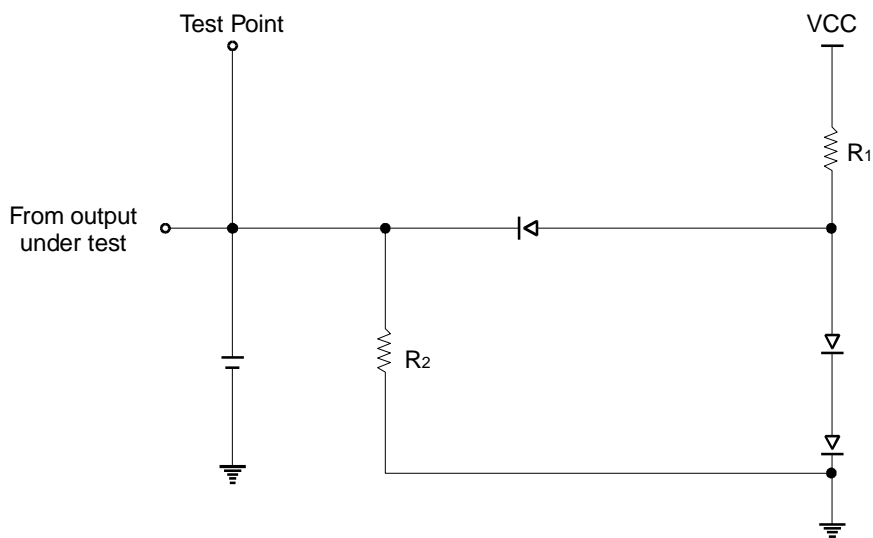
### 2.3.5 IDE Drive Timing (loading = 120 pf)

Signal		Min (ns)	Max (ns)
DCS0#, DCS1#, DSA[0..2]	High to low from CLK high	9	33
	Low to high from CLK high	7	24

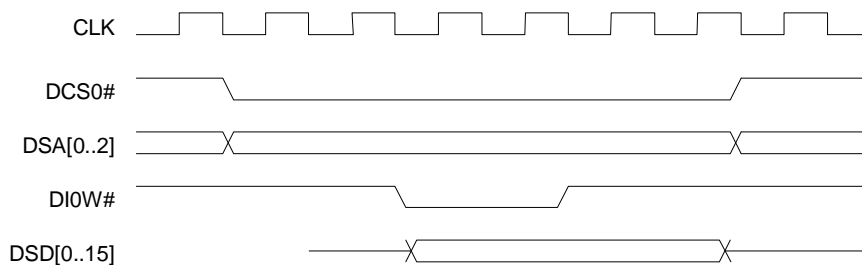


DIOR#, DIOW#	High to low from CLK high	7	26
	Low to high from CLK high	6	20
DSD[0..15] to DIOW# (2 CLKS)	Low to high setup time	45	56
	Hold time	50	57
DCS0# low to DIOW#, DIOR# low for port 1F0h		52	59
IOCHRDY to CLK high setup time		2	

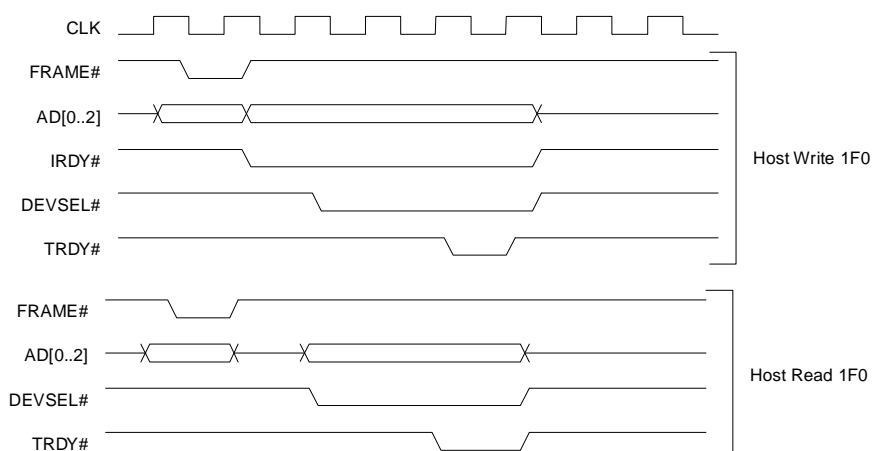
## 2.4 Output Test Load



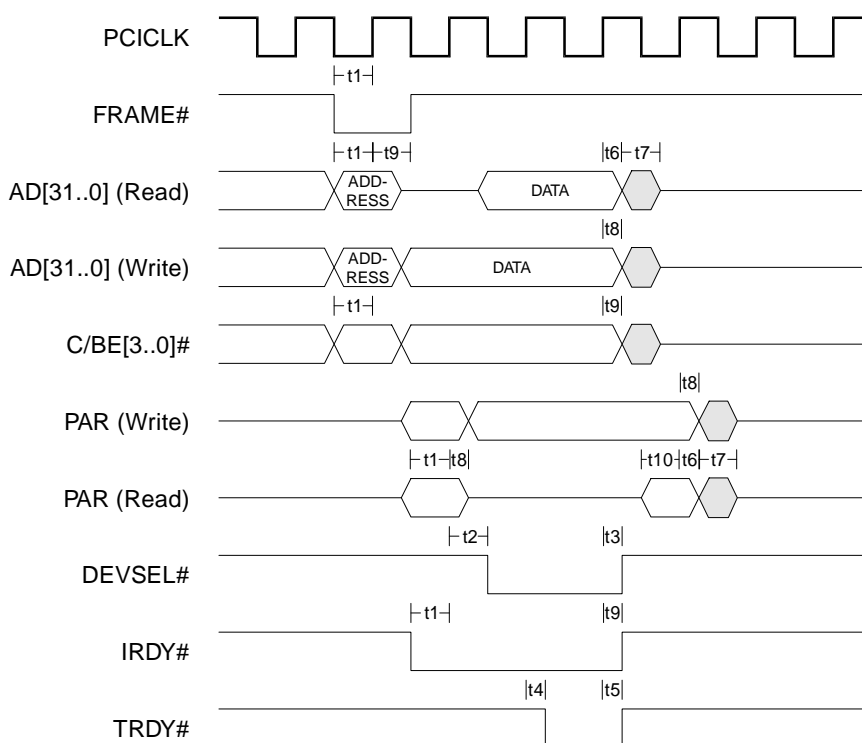
## 2.5 IDE Write Timing



## 2.6 Host Read/Write Timing



## 2.7 PCI Read/Write Timing in Target Mode

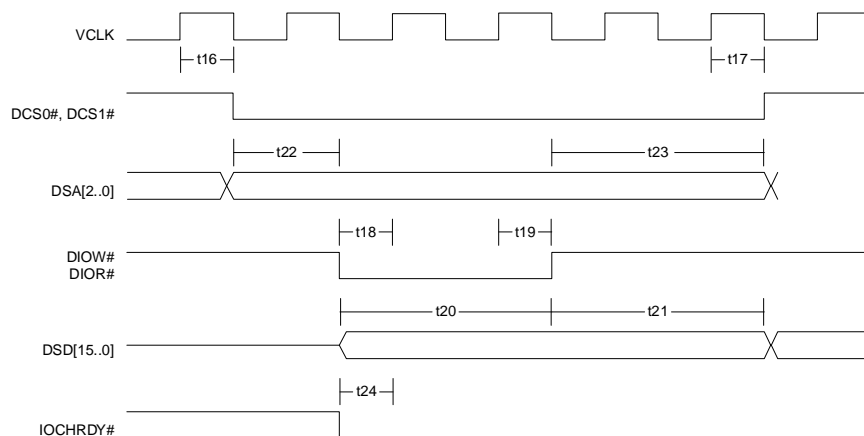


Symbol	Parameter	Timing
t1	FRAME#, IRDY#, C/BE[3..0]#, AD[31..0], PAR setup time	7 ns
t2	DEVSEL#, high to low from CLK high	4-11 ns
t3	DEVSEL#, low to high from CLK high	3-10 ns
t4	TRDY#, high to low from CLK high	4-11 ns
t5	TRDY#, low to high from CLK high	3-10 ns
t6	AD[31..0], PAR hold time in Read	4-11 ns



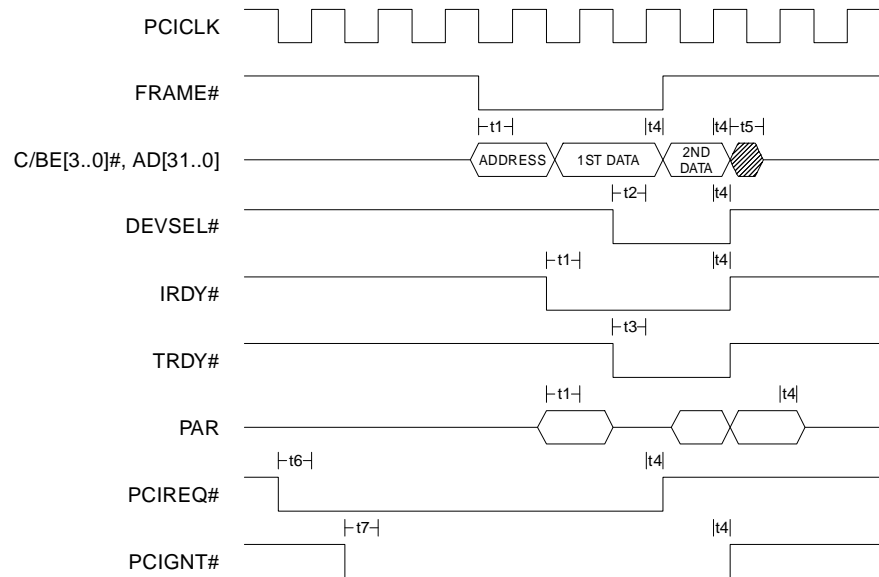
t7	active to float delay from CLK	8-28 ns
t8	AD[31..0], PAR hold time in Write	0 ns
t9	IRDY#, C/BE[3..0]#, FRAME# hold time	0 ns
t10	AD[31..0], PAR setup time in Read	19-26 ns

## 2.8 IDE Timing



Symbol	Parameter	Timing
t16	DCS0#, DCS1#, DSA[2..0] high to low from CLK high	6-21 ns
t17	DCS0#, DCS1#, DSA[2..0] low to high from CLK high	5-18 ns
t18	DIOR#, DIOW# high to low from CLK high	5-18 ns
t19	DIOR#, DIOW# low to high from CLK high	5-17 ns
t20	DSD[15..0] to DIOW# setup time (2 CLKS)	45-56 ns
t21	DSD[15..0] to DIOW# hold time (2 CLKS)	50-57 ns
t22	DCS0# low to DIOW#, DIOR# low for port 1F0 (2CLKS)	52-59 ns
t23	DIOW#, DIOR# high to DCS0# high for port 1F0 (2CLKS)	53-60 ns
t24	IOCHRDY to CLK high setup time	2 ns

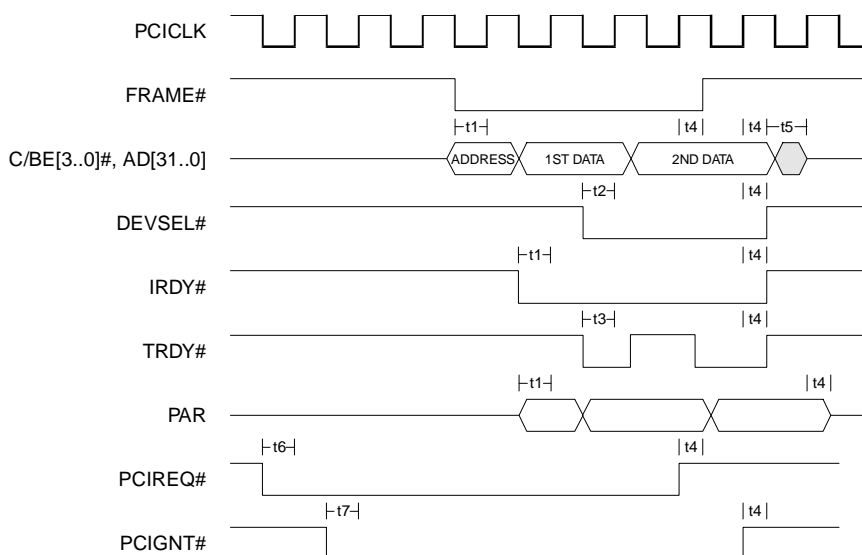
## 2.9 PCI DMA Master Read Timing (33MHz PCICLK)



See table in next section for an explanation of timing symbols.



## 2.10 PCI DMA Master Write Timing (33MHz PCICLK)



Symbol	Parameter	Timing
t1	FRAME#, IRDY#, C/BE[3..0]#, AD[31..0], PAR setup time	19-26 ns
t2	DEVSEL# setup time	7 ns
t3	TRDY# setup time	7 ns
t4	AD[31..0], FRAME#, IRDY#, C/BE[3..0]#, DEVSEL#, TRDY#, PAR, PCIREQ#, PCIGNT# hold time	0-11 ns
t5	Active to float delay from CLK	8-28 ns
t6	PCIREQ# setup time	18-25 ns
t7	PCIGNT# setup time	7 ns

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# Index

- active count function, 15
- address lines, 1
- clock signal, 5
- data lines, 1
- disk address bits, 4
- disk data bits, 4
- disk reset, 4
- DMA handshake, 1, 3
- DMA programming, 17
- drive channel ready, 2
- enable IDE, 4
- host CPU address bus, 1
- initiator ready, 5
- interrupt A, 5
- interrupt processing, 16
- IRQ 14, 3, 5
- IRQ 15, 5
- jumper settings, 21
- legacy mode, 5
- operating conditions, 1
- output test load, 3
- parity, 5
- parity error, 6
- PCI DMA master read, 6
- PCI DMA master write, 7
- Pin descriptions
  - AD[31..0], 1
  - C/BE[3..0]#, 1
  - DCHRDY, 2
- power specifications
  - AC, 2
  - DC, 1
- primary channel
  - read, 3
  - write, 3
- read ahead operation, 17
- recovery count function, 15
- registers
  - base address, 7
  - configuration, 9
  - IDE timing control, 9
  - PCI master control, 12
  - standard configuration, 7
  - status/command, 8
- reset internal registers, 6
- secondary channel
  - enabling and disabling, 1
  - reads, 1
  - write, 1
- target ready, 6
- task file registers, 16
- testing, 2, 6
- timing
  - clock, 2
  - host interface, 2
  - host read/write, 4
  - IDE, 5
  - IDE drive, 2, 3
  - IDE write, 3
  - PCI read/write target mode, 4

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