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PCI-649

Bus Master Ultra DMA PCI-IDE/ATA Chip

Product Specification

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1. Overview

CMD's PCI-649 is a single chip solution for a PCI to IDE/ATA controller. It accepts host commands through the PCI bus, processes them and transfers data between the host and IDE/ATA devices. It can be used to control two independent IDE/ATA channels: primary and secondary. Each channel has its own IDE/ATA bus and will support up to two ATA/ATAPI devices for a maximum of four devices. The PCI-649 supports up to a 100 MB/sec transfer rate as specified in ATA/ATAPI-6.

This controller provides OEMs with an enabling solution for interfacing to storage media such as hard disk drives. For personal computer manufacturers, using the PCI-649 will differentiate them from the competition by allowing for the addition of more drives and incorporating the newest drive standards, all at a lower cost. For non-personal computer manufacturers, it will allow a cost-effective solution with hard disk drives to be implemented in their system.

Key Benefits

CMD's PCI-649 stand-alone Ultra ATA/100 PCI to IDE/ATA host controller is the perfect single chip solution for designs based on chipsets without an integrated IDE host controller, or designs which need to expand the number of IDE channels to accommodate the growing number of storage peripherals with IDE interface. Any system with a PCI bus interface can simply add the Ultra ATA/100 interface by adding a card with the PCI-649 and loading the driver into the system.

The PCI-649 comes complete with drivers for DOS, Windows 95/98, Windows Millennium, Windows NT 4.0, and Windows 2000. It is also fully operational and compatible with default IDE drivers from Microsoft.

Features

- 2 independent IDE/ATA Channels
    - Supports up to four IDE/ATA devices
    - 128 Bytes buffer
- Supports ultra and multiword DMA timing modes
- CRC (Cyclical Redundancy Check)
- Built in 80-Pin cable detect circuitry
- Supports External BIOS
- 32-bit 33 MHz PCI Interface
- Supports bus master DMA at 133 MB/sec PCI burst rate
- Supports maximum IDE/ATA data transfer rate of 100 MB/sec
- Compatible with Microsoft IDE/ATA drivers (Windows 95/98, Windows Millennium, WIndows NT 4.0 and Windows 2000)
- 3.3V Operating Voltage with 5V tolerant I/O
- Available in 160-pin TQFP

PCI-649 Technical Description

The PCI-649 is available in a 160-pin TQFP (Thin Quad Flat Package) including more ground pins in order to accommodate the new higher data transfer rate specified in the ATA/ATAPI-6 specification. It is compliant with ATA/ATAPI-6 and will support transfer rates up to the Ultra ATA/100 rate in both channels. Each channel is independent and will support up to two IDE/ATA devices (such as hard disk drives, DVD drives, etc.) for a total of four devices per controller. The selected PCI bus targeted for this device is the 32-bit wide bus at 33MHz. The chip has an internal phase lock loop that will provide the 100MHz internal clock, allowing a data transfer rate of 100MB/sec on IDE/ATA interface. A built-in 80-pin cable detector provides users the ability to determine whether a cable can support the latest Ultra ATA/100 transfer rate. The PCI-649 is capable of supporting Native mode, external BIOS, Legacy mode, Enhanced IDE mode (ultra DMA and multi-word DMA mode).

References

For more details about the IDE/ATA technology, the reader is referred to the following industry specifications:

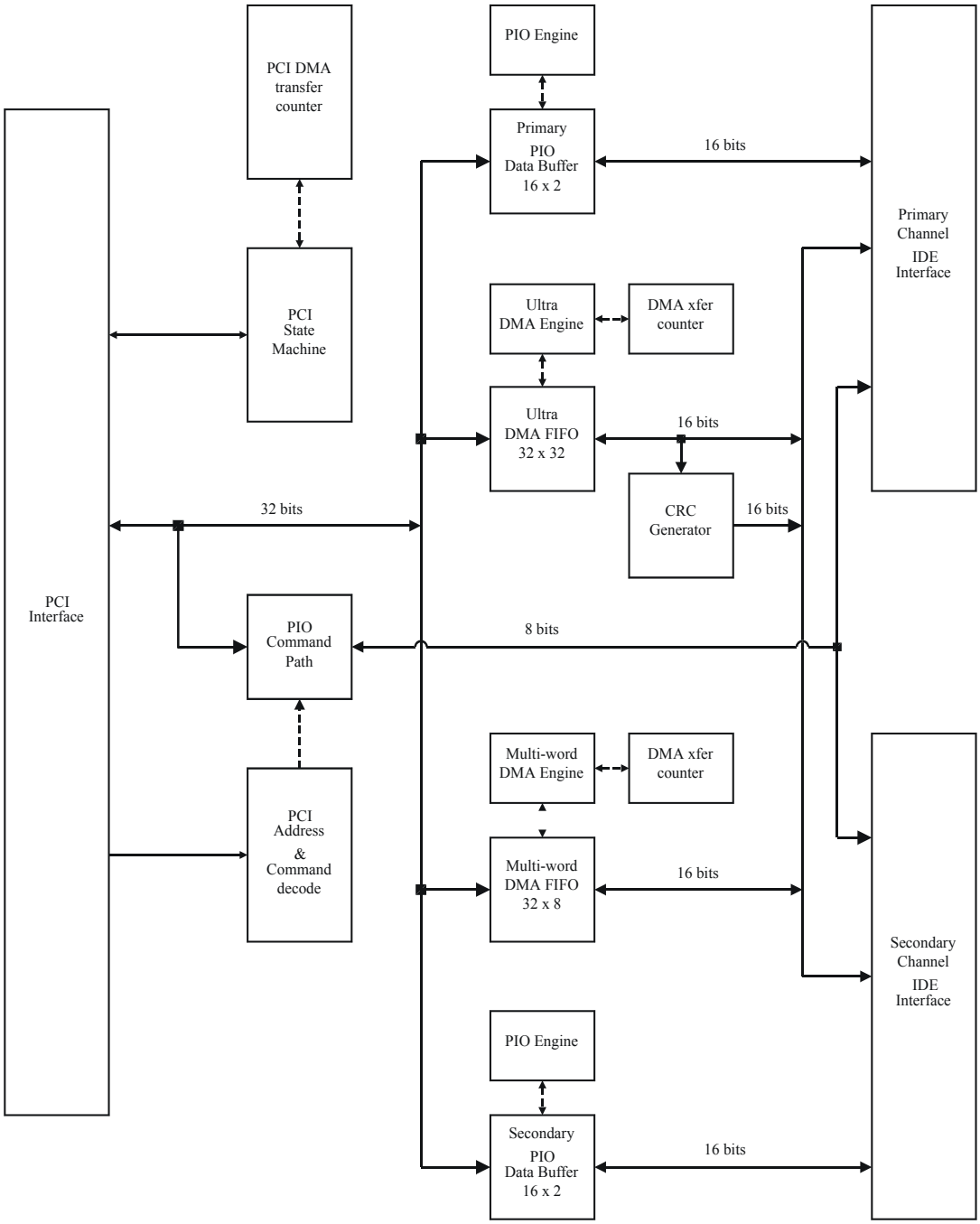
- ATA/ATAPI-6
- PCI Local Bus Specification Revision 2.1
- Advanced Power Management Specification Revision 1.0
- PCI IDE Controller Specification Revision 1.0
- Programming Interface for Bus Master IDE Controller, Revision 1.0

Functional Description

PCI-649 is more than a PCI-to-IDE/ATA bridge chip that transfers data between the PCI bus and storage media (e.g hard disk drive, etc) over the IDE/ATA bus. As a host controller, it also performs functions associated with the host, such as storing configuration information, and processing data for errors. The PCI-649 can be described in the following functional blocks:

- PCI Interface. Provides the interface to any system that has a PCI bus. Instructions and system clocks are based on this interface.
- IDE/ATA Interface. Two separate channels (Primary and Secondary) to access storage media such as hard disk drive, floppy disk drive, CD-ROM.
- Controller Interface. Additional hardware interface for controlling and configuring the Host Controller.
- Host Function.

Functional Block Diagram



PCI Interface

The PCI-649 PCI interface is compliant with the PCI Local Bus Specification (Revision 2.1, June 1, 1995). PCI stands for Peripheral Component Interconnect, a high-performance and robust interconnect bus that provides a processor-independent data path between the CPU and high-speed peripherals. The standard for PCI is monitored by the PCI Special Interest Group (PCI-SIG). The PCI-SIG is an unincorporated association of members of the microcomputer industry created to monitor and enhance the development of PCI architecture. The PCI-SIG is led by a nine-member steering committee and governed by PCI-SIG bylaws (HTTP://www.pcisig.com/).

The PCI-649 can act as a PCI master and a PCI slave, and contains the PCI-649 PCI configuration space and internal registers. When the PCI-649 needs to access shared memory, it becomes the bus master of the PCI bus and completes the memory cycle without external intervention. In the mode when it acts as a bridge between the PCI bus and the IDE/ATA bus it will behave as a PCI slave.

PCI Initialization

Generally, when a system initializes a module containing a PCI device, the configuration manager reads the configuration space of each PCI device on the PCI bus. Hardware signals select a specific PCI device based on a bus number, a slot number, and a function number. If a device that is addressed (via signal lines) responds to the configuration cycle by claiming the bus, then that function's configuration space is read out from the device during the cycle. Since any PCI device can be a multifunction device, every supported function's configuration space needs to be read from the device. Based on the information read, the configuration manager will assign system resources to each supported function within the device. Sometimes new information needs to be written into the function's configuration space. This is accomplished with a configuration write cycle.

PCI Bus Operations

PCI-649 behaves either as a PCI bus master or a PCI slave device at any time and switches between these modes as required during device operation.

As a PCI slave, the PCI-649 responds to the following PCI bus operations:

- I/O Read
- I/O Write
- Configuration Read
- Configuration Write
- Memory Read

All other PCI cycles are ignored by the PCI-649.

As a PCI bus master, the PCI-649 generates the following PCI bus operations:

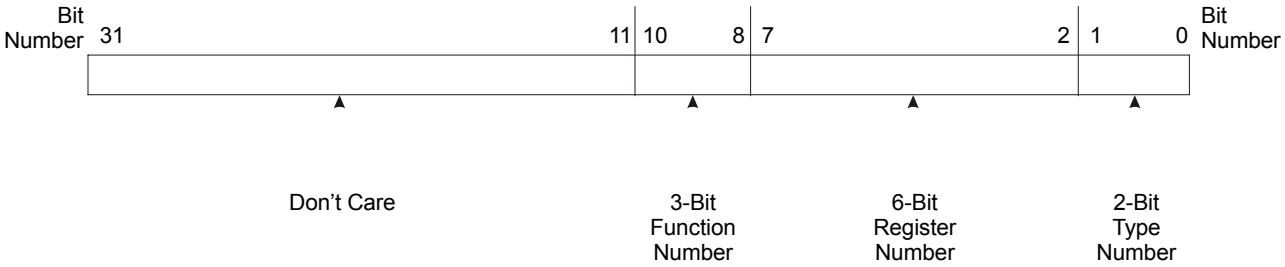
- Memory Read Multiple
- Memory Read Line
- Memory Read
- Memory Write

PCI Configuration Space

This section describes how the PCI-649 implements the required PCI configuration register space. The intent of PCI configuration space definition is to provide an appropriate set of configuration registers which satisfy the needs of current and anticipated system configuration mechanisms, without specifying those mechanisms or otherwise placing constraints on their use. These registers allow for:

- Full device relocation (including interrupt binding)
- Installation, configurations, and booting without user interventions
- System address map construction by device-independent software

Address Lines During Configuration Cycle



PCI-649 only responds to Type 0 configuration cycles. Type 1 cycles, which pass a configuration request on to another PCI bus, are ignored.

The PCI controller in PCI-649 responds to configuration and I/O cycles.

The address phase during a PCI-649 configuration cycle indicates the function number and register number being addressed which can be decoded by observing the status of the address lines AD[31:0].

The value of the signal lines AD[7:2] during the address phase of configuration cycles selects the register of the configuration space to access. Valid values are between 0 and 15, inclusive. Accessing registers outside this range results in an all-0s value being returned on reads, and no action being taken on writes.

The Class Code register contains the Class Code, Sub-Class Code, and Register-Level Programming Interface registers.

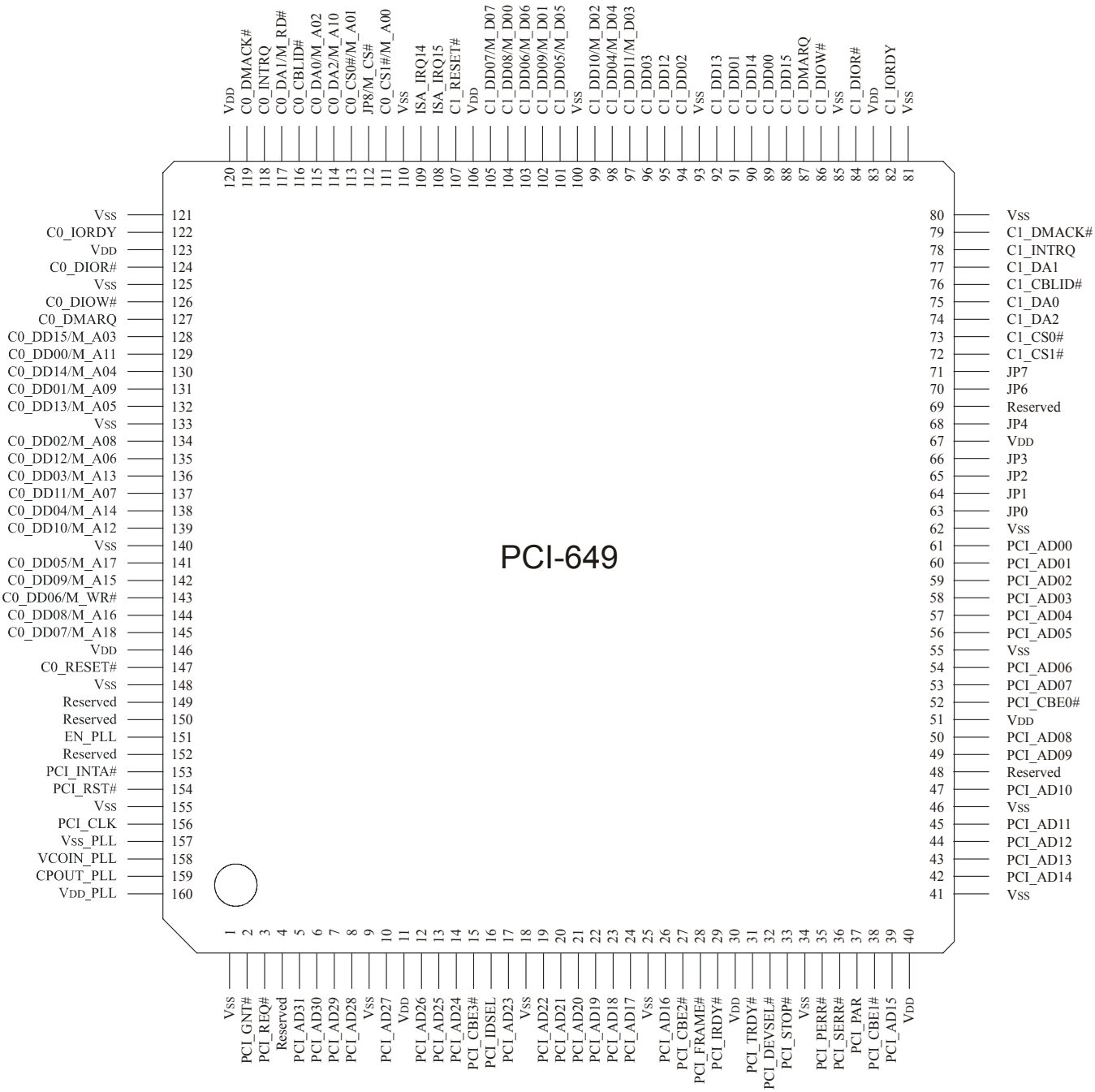
All writable bits in the configuration space are reset to 0 by the hardware reset, PCI RESET (RST#) asserted. After reset, PCI-649 is disabled and will only respond to PCI configuration write and PCI configuration read cycles. Write cycles to reserved bits and registers will have no effect. Read cycles to reserved bits will always result in 0 being read.

Deviations from the Specification

The PCI-649 product has been developed and tested to the specification listed in this document. As a result of testing and customer feedback, we may become aware of deviations to the specification that could affect the component's operation. To ensure awareness of these deviations by anyone considering the use of the PCI-649, we have included Appendix C, Deviations to the Specification. Please ensure that Appendix C is carefully reviewed. It is also important that you have the most current version of this specification. If there are any questions, please contact CMD Technology, Inc.

2. Pin Descriptions

Pin-Out Diagram



Pin Descriptions (in numerical order)

Pin #	Name	Type	External Damping Resistor	External Pull Up/ Pull Down Resistor	Description
1	V_{SS}	G	-	-	Ground
2	PCI_GNT#	I	-	-	PCI Grant. This signal indicates to the agent that access to the bus has been granted.
3	PCI_REQ#	T/O	-	-	PCI Request.This signal indicates to the arbiter that this agent desires use of bus.
4	Reserved	-	-	-	Do not connect
5	PCI_AD31	B	-	-	PCI Address and Data Pin
6	PCI_AD30	B	-	-	PCI Address and Data Pin
7	PCI_AD29	B	-	-	PCI Address and Data Pin
8	PCI_AD28	B	-	-	PCI Address and Data Pin
9	V_{SS}	G	-	-	Ground
10	PCI_AD27	B	-	-	PCI Address and Data Pin
11	V_{DD}	P	-	-	3.3 Volts
12	PCI_AD26	B	-	-	PCI Address and Data Pin
13	PCI_AD25	B	-	-	PCI Address and Data Pin
14	PCI_AD24	B	-	-	PCI Address and Data Pin
15	PCI_CBE3#	B	-	-	Bit 3 of the PCI Bus Command and Byte Enable pins
16	PCI_IDSEL	I	-	-	PCI Idsel is used as a chip select during configuration read and write transactions.
17	PCI_AD23	B	-	-	PCI Address and Data Pin
18	V_{SS}	G	-	-	Ground
19	PCI_AD22	B	-	-	PCI Address and Data Pin
20	PCI_AD21	B	-	-	PCI Address and Data Pin
21	PCI_AD20	B	-	-	PCI Address and Data Pin
22	PCI_AD19	B	-	-	PCI Address and Data Pin
23	PCI_AD18	B	-	-	PCI Address and Data Pin
24	PCI_AD17	B	-	-	PCI Address and Data Pin
25	V_{SS}	G	-	-	Ground
26	PCI_AD16	B	-	-	PCI Address and Data Pin
27	PCI_CBE2#	B	-	-	Bit 2 of the PCI Bus Command and Byte Enable pins
28	PCI_FRAME#	B	-	-	PCI Frame is a cycle frame driven by the current master to indicate the beginning and duration of an access.
29	PCI_IRDY#	B	-	-	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.

Pin #	Name	Type	External Damping Resistor	External Pull Up/ Pull Down Resistor	Description
30	V_{DD}	P	-	-	3.3 Volts
31	PCI_TRDY#	B	-	-	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
32	PCI_DEVSEL#	B	-	-	Device select, when actively driven, indicates the driving device has decoded its addresses as target of the current access.
33	PCI_STOP#	B	-	-	Stop indicates that the current target is requesting the master to stop the current transaction.
34	V_{SS}	G	-	-	Ground
35	PCI_PERR#	B	-	-	Parity Error is used exclusively for the reporting of data parity errors on all PCI transactions except a Special Cycle. The minimum duration of PCI_PERR# is one clock for each data phase that a data parity error is detected.
36	PCI_SERR#	O/D	-	-	System Error is used for other error signaling, including address parity and data parity on Special Cycle commands, and may optionally be used on any other non-parity or system errors.
37	PCI_PAR	B	-	-	Parity on PCI provides a mechanism to determine transaction by trans-action if the master is successful in addressing the desired target and if data transfers correctly between them.
38	PCI_CBE1#	B	-	-	Bit 1 of the PCI Bus Command and Byte Enable pins
39	PCI_AD15	B	-	-	PCI Address and Data Pin
40	V_{DD}	P	-	-	3.3 Volts
41	V_{SS}	G	-	-	Ground
42	PCI_AD14	B	-	-	PCI Address and Data Pin
43	PCI_AD13	B	-	-	PCI Address and Data Pin
44	PCI_AD12	B	-	-	PCI Address and Data Pin
45	PCI_AD11	B	-	-	PCI Address and Data Pin
46	V_{SS}	G	-	-	Ground
47	PCI_AD10	B	-	-	PCI Address and Data Pin
48	Reserved		-	-	Do not connect
49	PCI_AD09	B	-	-	PCI Address and Data Pin
50	PCI_AD08	B	-	-	PCI Address and Data Pin
51	V_{DD}	P	-	-	3.3 Volts
52	PCI_CBE0#	B	-	-	Bit 0 of the PCI Bus Command and Byte Enable pins
53	PCI_AD07	B	-	-	PCI Address and Data Pin
54	PCI_AD06	B	-	-	PCI Address and Data Pin

Pin #	Name	Type	External Damping Resistor	External Pull Up/ Pull Down Resistor	Description
55	V_{SS}	G	-	-	Ground
56	PCI_AD05	B	-	-	PCI Address and Data Pin
57	PCI_AD04	B	-	-	PCI Address and Data Pin
58	PCI_AD03	B	-	-	PCI Address and Data Pin
59	PCI_AD02	B	-	-	PCI Address and Data Pin
60	PCI_AD01	B	-	-	PCI Address and Data Pin
61	PCI_AD00	B	-	-	PCI Address and Data Pin
62	V_{SS}	G	-	-	Ground
63	JP0	I	-	-	Configuration Pin. See Chapter 4.
64	JP1	I	-	-	Configuration Pin. See Chapter 4.
65	JP2	I	-	-	Configuration Pin. See Chapter 4.
66	JP3	I	-	-	Configuration Pin. See Chapter 4.
67	V_{DD}	P	-	-	3.3 Volts
68	JP4	I	-	-	Configuration Pin. See Chapter 4.
69	Reserved	-	-	-	Do not connect
70	JP6	I	-	-	Configuration Pin. See Chapter 4.
71	JP7	I	-	-	Configuration Pin. See Chapter 4.
72	C1_CS1#	O	51Ω	-	Secondary Channel Chip Select for Command Block registers
73	C1_CS0#	O	51Ω	-	Secondary Channel Chip Select for Command Block registers
74	C1_DA2	O	51Ω	-	Bit 2 of Secondary IDE Channel's Device Address
75	C1_DA0	O	51Ω	-	Bit 0 of Secondary IDE Channel's Device Address
76	C1_CBLID#	I	-	-	Secondary IDE Channel's Cable Detect pin
77	C1_DA1	O	51Ω	-	Bit 1 of Secondary IDE channel's Device Address
78	C1_INTRQ	I	51Ω	-/10 KΩ	Secondary IDE Channel's Interrupt Request
79	C1_DMACK#	O	51Ω	-	Secondary IDE Channel's DMA Acknowledge pin
80	V_{SS}	G	-	-	Ground
81	V_{SS}	G	-	-	Ground
82	C1_IORDY	I	51Ω	4.7 KΩ/ -	Secondary IDE Channel's I/O Ready pin
83	V_{DD}	P	-	-	3.3 Volts
84	C1_DIOR#	O	51Ω	-	Secondary IDE Channel's Device I/O Read pin
85	V_{SS}	G	-	-	Ground
86	C1_DIOW#	O	51Ω	-	Secondary IDE Channel's Disk I/O Write pin

Pin #	Name	Type	External Damping Resistor	External Pull Up/ Pull Down Resistor	Description
87	C1_DMARQ	I	51Ω	-/5.6 KΩ	Secondary IDE Channel's DMA Request pin
88	C1_DD15	B	51Ω	-	Secondary IDE Channel's Device Data Bit 15
89	C1_DD00	B	51Ω	-	Secondary IDE Channel's Device Data Bit 0
90	C1_DD14	B	51Ω	-	Secondary IDE Channel's Device Data Bit 14
91	C1_DD01	B	51Ω	-	Secondary IDE Channel's Device Data Bit 1
92	C1_DD13	B	51Ω	-	Secondary IDE Channel's Device Data Bit 13
93	V_{SS}	G	-	-	Ground
94	C1_DD02	B	51Ω	-	Secondary IDE Channel's Device Data Bit 2
95	C1_DD12	B	51Ω	-	Secondary IDE Channel's Device Data Bit 12
96	C1_DD03	B	51Ω	-	Secondary IDE Channel's Device Data Bit 3
97	C1_DD11/M_D03	B	51Ω	-	Secondary IDE Channel's Device Data bit 11 / EPROM Data pin 3
98	C1_DD04/M_D04	B	51Ω	-	Secondary IDE Channel's Device Data bit 4 / EPROM Data pin 4
99	C1_DD10/M_D02	B	51Ω	-	Secondary IDE Channel's Device Data bit 10 / EPROM Data pin 2
100	V_{SS}	G	-	-	Ground
101	C1_DD05/M_D05	B	51Ω	-	Secondary IDE Channel's Device Data bit 5 / EPROM Data pin 5
102	C1_DD09/M_D01	B	51Ω	-	Secondary IDE Channel's Device Data bit 9 / EPROM Data pin 1
103	C1_DD06/M_D06	B	51Ω	-	Secondary IDE Channel's Device Data bit 6 / EPROM Data pin 6
104	C1_DD08/M_D00	B	51Ω	-	Secondary IDE Channel's Device Data bit 8 / EPROM Data pin 0
105	C1_DD07/M_D07	B	51Ω	-/10 KΩ	Secondary IDE Channel's Device Data bit 7 / EPROM Data pin 7
106	V_{DD}	P	-	-	3.3 Volts
107	C1_RESET#	O	51Ω	-	Secondary IDE Channel's Disk Reset pin
108	ISA_IRQ15	T/O	-		ISA_IRQ15 is used to request an interrupt for secondary IDE/ATA channel in the PCI IDE/ATA legacy mode It is tri-stated when the IDE/ATA channel is in native mode.
109	ISA_IRQ14	T/O	-		ISA_IRQ14 is used to request an interrupt for primary IDE/ATA channel in the PCI IDE/ATA legacy mode It is tri-stated when the IDE/ATA channel is in native mode.
110	V_{SS}	G	-	-	Ground
111	C0_CS1#/M_A00	O	51Ω	-	Primary IDE Channel's Chip Select Pin for Command Block registers / EPROM Address pin 0
112	JP8 / M-CS#	B	-	-	Configuration Pin/EPROM chip select. Refer to section A-2.
113	C0_CS0#/M_A01	O	51Ω	-	Primary IDE Channel's Chip Select Pin for Command Block registers / EPROM Address pin 1
114	C0_DA2/M_A10	O	51Ω	-	Primary IDE Channel's Device Address bit 2 / EPROM Address pin 10
115	C0_DA0/M_A02	O	51Ω	-	Primary IDE Channel's Device Address bit 0 / EPROM Address pin 2

Pin #	Name	Type	External Damping Resistor	External Pull Up/ Pull Down Resistor	Description
116	C0_CBLID#	I	-	-	Primary IDE Channel's Cable Detect Pin
117	C0_DA1 / M_RD#	O	51Ω	-	Primary IDE Channel's Device Address bit 1 / EPROM Read Pin
118	C0_INTRQ	I	51Ω	-/10 KΩ	Primary IDE Channel's Interrupt Request pin
119	C0_DMACK#	O	51Ω	-	Primary IDE Channel's DMA Acknowledge
120	V_{DD}	P	-	-	Power
121	V_{SS}	G	-	-	Ground
122	C0_IORDY	I	51Ω	4.7 KΩ/-	Primary IDE Channel's I/O Ready pin
123	V_{DD}	P	-	-	3.3 Volts
124	C0_DIOR#	O	51Ω	-	Primary IDE Channel's Disk I/O Read pin
125	V_{SS}	G	-	-	Ground
126	C0_DIOW#	O	51Ω	-	Primary IDE Channel's Disk I/O Write pin
127	C0_DMARQ#	I	51Ω	-/5.6 K	Primary IDE Channel's DMA Request pin
128	C0_DD15/M_A03	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 15 / EPROM Address pin 3
129	C0_DD00/M_A11	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 0 / EPROM Address pin 11
130	C0_DD14/M_A04	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 14 / EPROM Address pin 4
131	C0_DD01/M_A09	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 1 / EPROM Address pin 9
132	C0_DD13/M_A05	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 13 / EPROM Address pin 5
133	V_{SS}	G	-	-	Ground
134	C0_DD02/M_A08	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 2 / EPROM Address pin 8
135	C0_DD12/M_A06	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 12 / EPROM Address pin 6
136	C0_DD03/M_A13	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 3 / EPROM Address pin 13
137	C0_DD11/M_A07	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 11 / EPROM Address pin 7
138	C0_DD04/M_A14	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 4 / EPROM Address pin 14
139	C0_DD10/M_A12	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 10 / EPROM Address pin 12
140	V_{SS}	G	-	-	Ground
141	C0_DD05/M_A17	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 5 / EPROM Address pin 17
142	C0_DD09/M_A15	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 9 / EPROM Address pin 15
143	C0_DD06	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 6
144	C0_DD08/M_A16	B	51Ω	-	Primary IDE Channel's Device Disk Data bit 8 / EPROM Address pin 16
145	C0_DD07/M_A18	B	51Ω	-/10 KΩ	Primary IDE Channel's Device Disk Data bit 7 / EPROM Address pin 18
146	V_{DD}	P	-	-	3.3 Volts
147	C0_RESET#	O	51Ω	-	Primary IDE Channel Disk Reset

Pin #	Name	Type	External Damping Resistor	External Pull Up/ Pull Down Resistor	Description
148	V_{SS}	G	-	-	Ground
149	Reserved	-	-	-	Do not connect
150	Reserved	-	-	-	Do not connect
151	EN_PLL	I	-	-	Enable PLL Test Pin
152	Reserved	-	-	-	Do not connect
153	PCI_INTA#	O/D	-	-	Interrupt A is used to request an interrupt.
154	PCI_RST#	I	-	-	Reset is used to bring all PCI specific registers, sequencers, and signals to a consistent state.
155	V_{SS}	G	-	-	Ground
156	PCI_CLK	I	-	-	Clock provides timing for all transaction on PCI and is an input to every PCI device.
157	VSS_PLL	G	-	-	Phase Locked Loop signal / Ground
158	VCOIN_PLL	I	-	-	Phase Locked Loop signal / RC Circuit required
159	CPOUT_PLL	O	-	-	Phase Locked Loop signal / RC Circuit required
160	VDD_PLL	P	-	-	Phase Locked Loop signal / Power

Notes: *The values for the damping, pull up and pull down resistors are taken from the ATA specification's recommendation.*

 # following a signal name denotes an active low signal.

KEY TO PIN TYPE

Each pin is assigned a type, which identifies the pin category as determined by the PCI specification. The types are as follows:

Type	Description
B	Bi-directional Tri-state Input/Output
I	Input
O	Output
O/D	Open Drain
T/O	Tri-state Output
G	Ground
P	3.3 Volts

Pin Descriptions (by category/alphabetical order)

IDE/ATA Primary Channel

Cable Detect

Pin Names: C0_CBLID#
Pin Numbers: 116
C0_CBLID# (Cable Detect) determines the type of cable attached to the primary channel. Drives using 80-pin cables will be allowed to transfer data at a rate up to 100MB/sec; otherwise, the maximum data transfer rate is 33 MB/sec.

Chip Select

Pin Names: C0_CS0#; C0_CS1#
Pin Numbers: 113, 111
C0_CS0# is the Drive Chip Select for Command Block Register Access to the Primary Channel. C0_CS1# is the Drive Chip Select for Control Block Register access to the Primary Channel.

Disk Address

Pin Names: C0_DA[2..0]
Pin Numbers: 114, 117, 115
Disk Address bits 0 through 2 are normally outputs to the ATA connector selecting the register in the drive's Command Block register. C0_DA[2::0] sends address signals to the primary channel. These address signals are decoded from the AD[2::0] and C/BE[3::0] inputs. All of these pins have internal pull-up resistors.

Disk Data Bus

Pin Names: C0_DD[15..0]
Pin Numbers: 128, 130, 132, 135, 137, 139, 142, 144, 145, 143, 141, 138, 136, 134, 131, 129
Disk Data bits 0 through 15 are the 16-bit bi-directional data bus which connects to the IDE/ATA drive(s). C0_DD[15::0] are data signals to the primary Channel. C0_DD[7::0] defines the low byte while C0_DD[15::8] defines the high byte of this 16-bit data register. The data bus is normally in a high impedance state and is driven by the PCI-649 during the DIOW# command pulse in either single/multi-word DMA mode, or valid at every edge of C0_DIOR# (HSTROBE) or C0_IORDY (DSTROBE) in Ultra DMA mode. C0_DD07 is a multifunction pin which allows a host to recognize the absence of an ATA/ATAPI device at power-up. A 10KΩ pull down resistor is recomended to be connected to this pin. Variation in an ATA/ATAPI device may require that the designer change the resistor to 6.8KΩ on some systems.

Disk I/O Read

Pin Name: C0_DIOR#
Pin Number: 124
Primary Channel Disk I/O Read is an active low output which enables data to be read from the drive. The duration and repetition rate of C0_DIOR# cycles is determined by PCI-649 programming. C0_DIOR# to the primary channel is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the primary channel drive. This signal is also defined as primary channel HDMARDY# in Ultra DMA read mode.

Disk I/O Write

Pin Name: C0_DIOW#
Pin Number: 126
Primary Channel Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition of C0_DIOW# cycles is determined by PCI-649 Programming. C0_DIOW# to the primary channel is driven high when inactive. This signal is defined as primary channel STOP in ultra DMA mode.

DMA Acknowledge

Pin Name: C0_DMACK#
Pin Number: 119
This signal is normally used by the PCI-649 in response to C0_DMARQ to either acknowledge that the primary channel is ready to accept data, or that data is available. This signal is also used to write CRC code to the primary channel drive at the end of each Ultra DMA burst transfer.

DMA Request

Pin Name: C0_DMARQ
Pin Number: 127
This signal is used in a handshake manner with C0_DMACK#, and shall be asserted high by the currently selected drive attached to the primary IDE/ATA Channel when it is ready to transfer data to or from the host.

Interrupt Request

Pin Name: C0_INTRQ
Pin Number: 118
Primary channel interrupt request is an input signal used to generate the ISA_IRQ14 output when the primary IDE/ATA channel is in legacy mode. When the primary IDE/ATA channel is in native mode, this pin generates the PCI_INTA# Output. This input should have a 1kΩ pull-down resistor connected to it.

I/O Ready

Pin Name: C0_IORDY
Pin Number:122
The Primary channel drive I/O ready is an active high input. It indicates that the IDE/ATA disk drive has completed the current command cycle. A 1kΩ pull-up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the currently selected drive to the primary channel. This signal is also defined as DDMARDY# in Ultra DMA write mode.

Disk Reset

Pin Name: C0_RESET#
Pin Number: 147
Disk Reset is an active low output which signals the IDE/ATA drive to initialize its control register. C0_RESET# is a buffered version of the PCI_RST# input and can be generated by programming the PCI-649 register and connects directly to the ATA connector. C0_RESET# asserts reset to the primary IDE/ATA channel.

Interrupt

Pin Name: ISA_IRQ14
Pin Number: 109
ISA_IRQ14 is used to generate an interrupt for primary IDE/ATA channel in PCI IDE/ATA Legacy Mode (For PC-AT compatibles). ISA_IRQ14 is tri-stated when IDE/ATA port 0 is in Native Mode.

IDE/ATA Secondary Channel

Cable Detect

Pin Names: C1_CBLID#
Pin Number: 76
C1_CBLID# (Cable Detect) determines the type of cable attached to the secondary channel. Attached drives using 80-pin cables will be allowed to transfer data at a rate up to 100MB/sec; otherwise, the maximum data transfer rate is 33 MB/sec.

Chip Select

Pin Names: C1_CS0#; C1_CS1#
Pin Numbers: 73, 72
C1_CS0# is the Drive Chip Select for Command Block Register access to the Secondary Channel's master drive. C1_CS1# is the Drive Chip Select for Control Block Register access to the Secondary Channel's slave drive.

Disk Address

Pin Names: C1_DA[2..0]
Pin Numbers: 74, 77, 75
Disk Address bits 0 through 2 are normally outputs to the ATA connector to select the register in the drive's Command Block register. C1_DA [2..0] sends address signals to the secondary channel. These address signals are decoded from the AD[2::0] and C/BE[3::0] inputs. All of these pins have internal pull-up resistors.

Disk Data Bus

Pin Names: C1_DD[15..0]
Pin Numbers: 88, 90, 92, 95, 97, 99, 102, 104, 105, 103, 101, 98, 96, 94, 91, 89
Disk Data bits 0 through 15 are the 16-bit bi-directional data bus which Connects to the IDE/ATA drive(s). C1_DD[15::0] are data signals to the secondary channel. C1_DD[7::0] defines the low data byte while C1_DD[15::8] defines the high data byte of this 16-bits data register. The data bus is normally in a high impedance state and is driven by the PCI-649 during the DIOW# command pulse in enhanced mode, or valid at every edge of C1_DIOR# (HSTROBE) or C1_IORDY (DSTROBE) in Ultra DMA mode. C1_DD07 is a multifunction pin which allows a host to recognize the absence of an ATA/ATAPI device at power-up. A 10KΩ pull down resistor is recomended to be connected to this pin. Variation in an ATA/ATAPI device may require that the designer change it to 6.8KΩ on some systems.

Disk I/O Read

Pin Name: C1_DIOR#
Pin Number: 84
This is an active low output which enables data to be read from the drive. The duration and repetition rate of C1_DIOR# cycles is determined by programming the PCI-649 PIO timing registers. C1_DIOR# to the secondary channel is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the secondary channel drive. This signal is also defined as secondary channel HDMARDY# in Ultra DMA read mode.

Disk I/O Write

Pin Name: C1_DIOW#
Pin Number: 86
This is an active low output that enables data to be written to the drive. The duration and repetition rate of C1_DIOW# cycles is determined by programming the PCI-649 PIO timing registers. C1_DIOW# to the Secondary channel is driven high when inactive. This signal is also defined as secondary channel STOP in Ultra DMA mode.

DMA Acknowledge

Pin Name: C1_DMACK#
Pin Number: 79
This signal is normally used by the PCI-649 in response to C1_DMARQ to either acknowledge that the secondary channel is ready to accept data, or that data is available. This signal is also used to write CRC code to the secondary channel drive at the end of each Ultra DMA burst transfer.

DMA Request

Pin Name: C1_DMARQ
Pin Number: 87
This signal is used in a handshake manner with C1_DMACK# and shall be asserted high by the currently selected drive attached to the secondary IDE/ATA channel when it is ready to transfer data to or from the host.

Interrupt Request

Pin Name: C1_INTRQ
Pin Number: 78
Secondary Channel Interrupt Request is an input used to generate the ISA_IRQ15 output when the secondary IDE/ATA channel is in legacy mode. When the secondary IDE/ATA channel is in native mode, this pin generates the PCI_INTA# output. This input should have a 1KΩ pull-down resistor connected to it.

I/O Ready

Pin Name: C1_IORDY
Pin Number: 82
The Secondary Channel Drive Channel's Initiator Ready is an active high input. It indicates that the IDE/ATA disk drive has completed the current command cycle. A 1KΩ pull-up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the currently selected drive attached to the secondary channel. This signal is also defined as DDMARDY# in Ultra DMA write mode.

Disk Reset

Pin Name: C1_RESET#
Pin Number: 107
Disk Reset is an active low output which signals the IDE/ATA drive to initialize its control register. C1_RESET# is a buffered version of the PCI_RST# input and can be generated by programming the PCI-649 register and connects directly to the ATA connector. C1_RESET# asserts reset to the secondary IDE/ATA channel.

Interrupt

Pin Name: ISA_IRQ15
Pin Number: 108
ISA_IRQ15 is used to generate an interrupt for secondary IDE/ATA channel in PCI IDE/ATA Legacy Mode (PC-AT compatible.). ISA_IRQ15 is tri-stated when IDE/ATA port 1 is in Native Mode.

PCI Interface

PCI Address and Data

Pin Names: PCI-AD[31..0]
Pin Numbers: 5-8, 10, 12-14, 17, 19-24, 26, 39, 42-45, 47, 49-50, 53-54, 56-61
Address and Data buses are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the first clock cycle in which FRAME# signal is asserted. During the address phase, AD[31::0] contain a physical address (32 bits). For I/O, this can be a byte address. For configuration and memory it is a DWORD address. During data phases, AD[7::0] contain the least significant byte (LSB) and AD[31::24] contain the most significant byte (MSB). Write data is stable and valid when IRDY# is asserted; read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.

PCI Command and Byte Enables

Pin Names: PCI-C/BE[3..0]
Pin Numbers: 15, 27, 38, 52
Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase, C/BE[3::0]# are used as Byte Enables. Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. Byte Enable bits 0 through 3 from the host CPU address bus. These inputs are active low and specify which bytes will be valid for master read and/or write data transfers.

PCI Clock Signal

Pin Names: PCI_CLK
Pin Number: 156
Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals (except PCI_RST#, and PCI_INTA#) are sampled on the rising edge of PCI_CLK. All other timing parameters are defined with respect to this edge.

PCI Device Select

Pin Name: PCI_DEVSEL#
Pin Number: 32
Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, PCI_DEVSEL# indicates to a master whether any device on the bus has been selected.

PCI Cycle Frame

Pin Name: PCI_FRAME#
Pin Number: 28
Cycle Frame is driven by the current master to indicate the beginning and duration of an access. PCI_FRAME # is asserted to indicate that a bus transaction is beginning. While PCI_FRAME # is asserted, data transfers continue. When PCI_FRAME # is de-asserted, the transaction is in the final data phase or has completed.

PCI Grant

Pin Name: PCI_GNT#
Pin Number: 2
This signal indicates to the agent that access to the PCI bus has been granted. In response to a PCI request, this is a point-to-point signal. Every master has its own PCI_GNT# which must be ignored while PCI_RST# is asserted.

PCI ID Select

Pin Name: PCI_IDSEL
Pin Number: 16
This signal is used as a chip select during configuration read and write transactions.

PCI Interrupt A

Pin Name: PCI_INTA#
Pin Number: 153
Interrupt A is used to request an interrupt in PCI IDE/ATA native mode. PCI_INTA# is open collector and is pulled up when both IDE/ATA ports are in legacy mode. See also the JP2 definition (Jumper Number 2) in the boot strap jumper section.

PCI Initiator Ready

Pin Name: PCI_IRDY#
Pin Number: 29
Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with PCI_TRDY#. A data phase is completed on any clock when both PCI_IRDY# and PCI_TRDY# are sampled as asserted. Wait cycles are inserted until both PCI_IRDY# and PCI_TRDY# are asserted together.

PCI Parity

Pin Name: PCI_PAR
Pin Number: 37
PCI_PAR is even parity across AD[31..0] and C/BE[3..0]#. Parity generation is required by all PCI agents. PCI_PAR is stable and valid one clock after the address phase. For data phases PCI_PAR is stable and valid one clock after either PCI_IRDY# is asserted on a write transaction or PCI_TRDY# is asserted on a read transaction. Once PCI_PAR is valid, it remains valid until one clock after the completion of the current data phase. (PCI_PAR has the same timing as AD[31..0] but delayed by one clock.)

PCI Request

Pin Name: PCI_REQ#
Pin Number: 3
This signal indicates to the arbiter that this agent desires use of the PCI bus.

PCI Reset

Pin Name: PCI_RST#
Pin Number: 154
PCI_RST# is an active low input that is used to set the internal registers to their initial state. PCI_RST# is typically the system power-on reset signal as distributed on the PCI bus.

PCI System Error

Pin Name: PCI_SERR#
Pin Number: 36
System Error is for reporting address parity errors, data parity errors on Special Cycle Command, or any other system error where the result will be catastrophic. The PCI_SERR# is a pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of PCI_SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of PCI_SERR# to the de-asserted state is accomplished by a weak pull-up. Note that if an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

PCI Stop

Pin Name: PCI_STOP#
Pin Number: 33
PCI_STOP# indicates the current target is requesting the master to stop the current transaction.

PCI Target Ready

Pin Name: PCI_TRDY#
Pin Number: 31
Target Ready indicates the target agent's ability to complete the current data phase of the transaction. PCI_TRDY# is used with PCI_IRDY#. A data phase is completed on any clock when both PCI_TRDY# and PCI_IRDY# are sampled asserted. During a read, PCI_TRDY# indicates that valid data is present on AD[31..0]. During a write, it indicates the target is prepared to accept data.

Miscellaneous I/O

Configuration Signal

Pin Names: JP[8..6], JP[4..0]
Pin Numbers: 112, 71, 70, 68, 66, 65, 64, 63
These are the configuration signal pins. Refer to the bootstrap jumper setting section for jumper usage information. JP5 is currently reserved and is used as TEST1.

PLL Enable

Pin Name: EN_PLL
Pin Number: 151
PLL's VCO enable signal.

Ground

Pin Name: V_{SS}
Pin Number: 1, 9, 18, 25, 34, 41, 46, 55, 62, 80, 81, 85, 93, 100, 110, 121, 125, 133, 140, 148, 155
Ground reference point to power supply.

PLL GND

Pin Name: V_{SS}_PLL
Pin Number: 157
Dedicated PLL Ground.

PLL V_{COIN}

Pin Name: V_{COIN}_PLL
Pin Number: 158
Dedicated Analog input from off-chip loop filter.

PLL V_{DD}

Pin Name: V_{DD}_PLL
Pin Number: 160
Dedicated PLL power supply.

PLL C_{POUT}

Pin Name: C_{POUT}_PLL
Pin Number: 159
Dedicated PLL output to off-chip filter.

Power Supply Input

Pin Name(s): V_{DD}
Pin Number(s): 11, 30, 40, 51, 67, 83, 106, 120, 123, 146
Power Supply Input (3.3 volts +/- .3 Volts)

3. Bootstrap Jumper Settings

No.	Pin Name	Description	Pull-Down (Set Low)	No Pull-Down (Set High)*	Pull-Down Resistor Value
0	JP0	At power-up reset, the state of this signal determines whether the chip powers up as an IDE/ATA device or a RAID device. Note that by configuring the device to RAID mode, PCI IDE/ATA 0648 can avoid the conflicts arising from the motherboard BIOS's IDE/ATA special handling side. PCI Configuration Space Register Index 0Ah (Sub-class).	RAID Device (Sub - Class code = 04)*	IDE/ATA Device (Sub - Class code = 01)	1 KΩ
1	JP1	When the status of this pin is low, base address registers always return 0. Primary IDE/ATA channel will use IRQ14 and secondary IDE/ATA channel will use IRQ15. IDE/ATA task file registers are mapped to the default port addresses of 1Fx (Primary) and 17x (Secondary). Both channels are operating in legacy mode and can not be switched to native mode by software. When the status of this pin is high, it is native mode capable and it can power up either in native mode or in legacy mode, depending on JP2's status. PCI Configuration Space Register Index 09h (bit 1 and 3)	Not native mode capable	Native mode capable*	1 KΩ
2	JP2	When JP1 is low, the status of JP2 does not matter. It is always legacy mode. When JP1 is high, the status of JP2 determines whether the chip powers up in native mode or legacy mode. If JP2 is low, then chip powers up in native mode. If JP2 is high, then chip powers up in legacy mode. The software can switch the modes by programming the Programmable Interface Register (PCI Configuration Space Register Index 9: bit 0 and 2). It can be programmed only if JP0 is set to IDE Device. If it is set to RAID device, Index 9h is always 00h.	Native Mode*	Legacy Mode	1 KΩ
3	JP3	When the status of this pin is low, disable Primary IDE/ATA channel access. Primary IDE/ATA Channel interrupt is disabled. When the status of this pin is high and I/O space bit (PCI configuration Index 4: bit 0) is set, it enables Primary IDE/ATA Channel access and interrupt. (PCI Configuration Space Register Index 51h: bit 2)	Disable Primary IDE/ATA channel	Enable Primary IDE/ATA channel*	1 KΩ
4	JP4	At power-up reset, the state of this signal is used to enable/disable the Secondary IDE/ATA channel. (PCI Configuration Space Register Index 51h: bit 3)	Enable Secondary IDE/ATA channel*	Disable Secondary IDE/ATA channel	1 KΩ

No.	Pin Name	Description	Pull-Down (Set Low)	No Pull-Down (Set High)*	Pull-Down Resistor Value
6	JP6	This signal is an active high input that controls the default disk operation mode following reset. When set low, the IDE/ATA cycles are disabled following reset. This mode allows software to first scan for system hardware and then enable the chip later via the command register ...(PCI Configuration Space Register index 4h: bit 0). By default, it has to be '0' according to PCI spec. When left floating or pulled high, the chip is enabled and cannot be disabled via software.	Value = 0 Disable IDE/ATA*	Value = 1 Enable IDE/ATA	1 KΩ
7	JP7	At power-up reset, the state of this signal will determine whether to load the CMD ID into the subsystem ID and subsystem vendor ID configuration registers. (PCI Configuration Space Register Index 4Fh: bit 1)	Do not overwrite the Subsystem ID and Subsystem Vendor ID at PCI_RST#	Replace with CMD value at PCI_RST#*	1 KΩ
8	JP8	At power-up reset the state of this signal determines whether or not EPROM access is enabled. EPROM support will be disabled if this pin is set low. EPROM support is for add-on card design. (PCI Configuration Space Register Index 04h: bit 1)	No EPROM Support *	EPROM Support	1 KΩ

Notes: ** = default jumper setting*

No two jumpers may be connected to the same resistor.

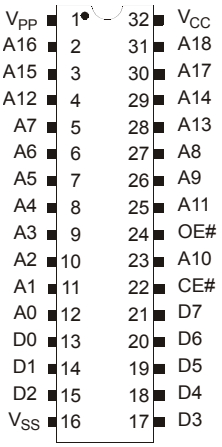
See Appendix C for Jumper Termination recommendation.

4. External EPROM Pin-out Diagram

For the PCI-649 bus master Ultra DMA PCI-IDE/ATA chip can operate with or without the presence of an EPROM. The sole purpose of the EPROM is for add-on card design. This is to resolve any compatibility issues with the mother-board BIOS. For the system integrator, use of the EPROM is not necessary.

For the PCI-649 PCI-IDE/ATA chip, the size of the EPROM used can be up to 4 Megabit (512K x 8) UV Erasable CMOS EPROM at 55ns, 90ns, 120ns. The following is a pin-out of the typical 4 Megabit (512K x 8) EPROM for your reference.

EPROM Diagram:



Notes: *The 32-pin DIP to 32-pin PLCC configuration varies from the JEDEC 28-pin DIP to 32-pin PLCC configuration.*

Pin Name	Description
A0 - A18	Address Inputs
CE#	Chip Enable
D0-D7	Data Ouput
OE#	Output Enable
V_{CC}	Vcc Supply Voltage
V_{PP}	Program Voltage Input
V_{SS}	Ground Logic Symbol

For add-on card design, please refer to pin-out diagram of the PCI-649 chip and the following table for EPROM connection information.

EPROM Pin No.	EPROM Pin Name	PCI-649 Pin No.	PCI-649 Pin Name
1	VPP	-	-
2	A16	144	C0_DD08
3	A15	142	C0_DD09
4	A12	139	C0_DD10
5	A07	137	C0_DD11
6	A06	135	C0_DD12
7	A05	132	C0_DD13
8	A04	130	C0_DD14
9	A03	128	C0_DD15
10	A02	115	C0_DA0
11	A01	113	C0_CS0#
12	A00	111	C0_CS1#
13	D0	104	C1_DD08
14	D1	102	C1_DD09
15	D2	99	C1_DD10
16	GND	-	-
17	D3	97	C1_DD11
18	D4	98	C1_DD04
19	D5	101	C1_DD05
20	D6	103	C1_DD06
21	D7	105	C1_DD07
22	CE#	112	JP8
23	A10	114	C0_DA2
24	OE#	117	C0_DA1
25	A11	129	C0_DD00
26	A09	131	C0_DD01
27	A08	134	C0_DD02
28	A13	136	C0_DD03
29	A14	138	C0_DD04
30	A17	141	C0_DD05
31	A18	145	C0_DD07
32	VCC	-	-

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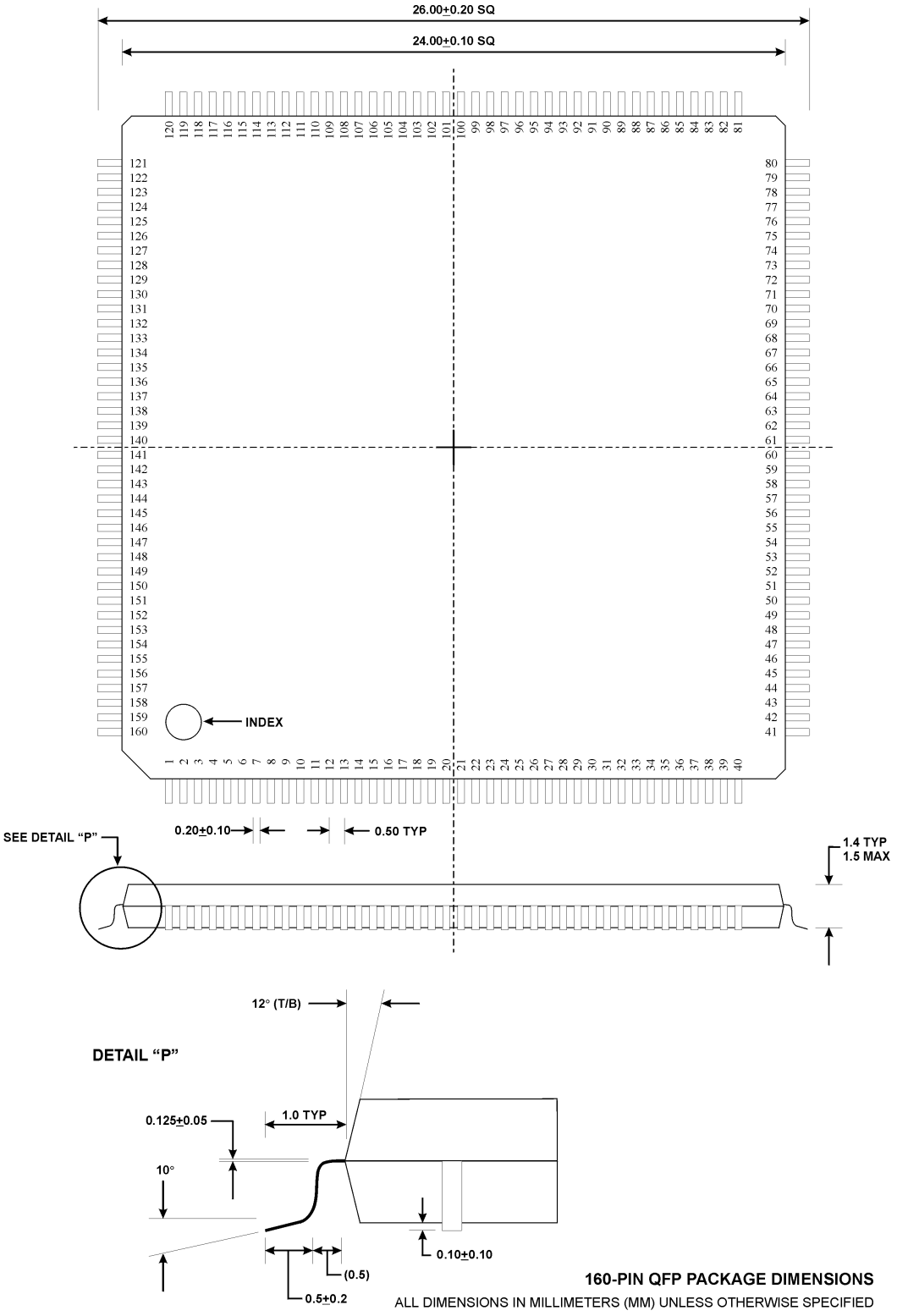
5. Mechanical Dimensions (TQFP)

PCI-649 Dimensions

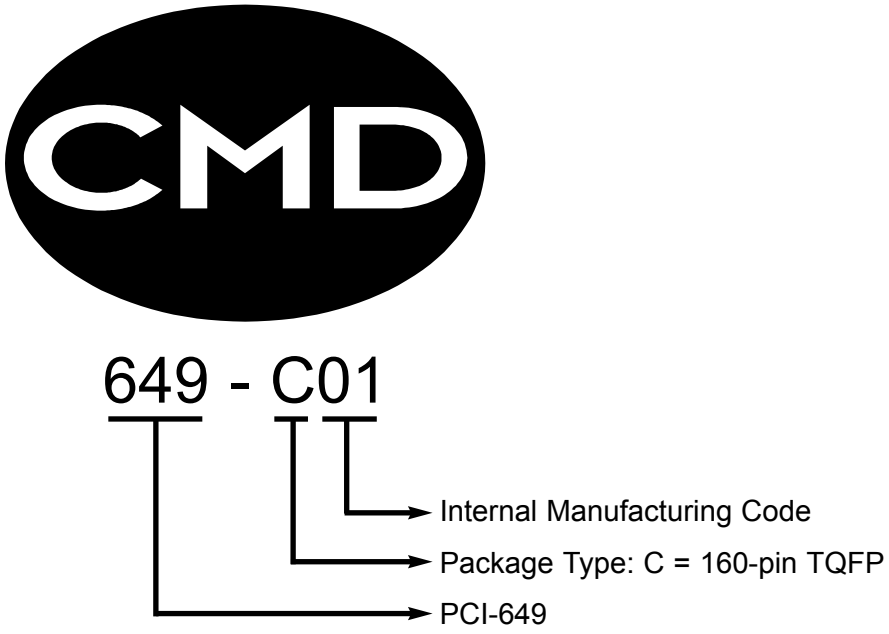


160-PIN QFP PACKAGE DIMENSIONS

ALL DIMENSIONS IN MILLIMETERS (MM) UNLESS OTHERWISE SPECIFIED

Physical Part Markings

The latest revision of the PCI-649 will be physically marked as follows:



Part Number to Order

For customers ordering the PCI-649 that do not care whether the part is manufactured by Kawasaki or NFI, order part number ICS-000649-CA1. By doing so you will receive either the Kawasaki part or the NFI part, whichever one is available at the time of the order. If a specific manufacturer is required order either the Kawasaki or NFI-specific part, and you will receive PCI-649s made only by that manufacturer.

ICS-000649-C01 - Kawasaki
ICS-000649-C02 - NFI
ICS-000649-CA1 - First available

6. Register Definitions

6.1 PCI Configuration Space Registers

PCI Configuration Registers Map

Address	Byte 3	Byte 2	Byte 1	Byte 0
	[31:24]	[23:16]	[15:8]	[7:0]
00h	Device_ID (0649h)		Vendor_ID (1095h)	
04h	Command / Status Register			
08h	Class Code		PROGIF	Revision ID
0Ch	BIST	Header Type	Latency Timer	Cache Line Size
10h	Base_Address_0 (01F1h)			
14h	Base_Address_1 (03F1h)			
18h	Base_Address_2 (0171h)			
1Ch	Base_Address_3 (0371h)			
20h	PCI_Bus_Master_Base_Address_Register (X1h)			
24h	Reserved			
28h	Reserved			
2Ch	Sub_System_ID (0649h Default) *		Sub_System_Vendor_ID (1095h Default) *	
30h	ROM Expansion Address			
34h	Reserved			Capability Pointer
38h	Reserved			
3Ch	Max_Latency (04h)	Min_Gnt (02h)	Interrupt_Pin (01h)	INTLINE (0x0E)
40h	Reserved			
44h	Reserved			
48h	Reserved			
4Ch	SUBCONF	Reserved		
50h	ARTTIM0	CMDTIM	CNTRL	CFR
54h	ARTTIM23	DRWTIM1	ARTTIM1	DRWTIM0
58h	DRWTIM3	Reserved	BRST	DRWTIM2
5Ch	Reserved			
60h	Pwr_Management_Cap_Reg		Next_Item_Ptr = 00h	CAP_ID = 01h
64h	Pwr_Data_Reg	Reserved	Power_Management_Control/StatusReg (PMCSR)	
68h	Reserved			
6Ch	Reserved			
70h	UDIDETCR0	BMIDESR0	MRDMODE	BMIDECR0
74h	DTPR0 (IDE0_Scatter_Gather_List_Pointer)			
78h	UDIDETCR1	BMIDESR1	BMIDECSR	BMIDECR1
7Ch	DTPR1 (IDE1_Scatter_Gather_List_Pointer)			
80h	Reserved			
84h	Reserved			
88h	Reserved			
8Ch	Shadow of Sub System ID Reg (0649h)		Shadow of Sub Vendor ID Reg (1095h)	

Notes:

* The Sub-System Identification and Sub-Vendor Identification may vary. Refer to JP7 of the bootstrap jumper section for details.

Vendor/Device ID

Address	bit	rst	r/w	Description
00h	[31:16]	0649h	sw:r/-	This unique device identification is assigned by CMD Technology, Inc. This field always returns the value 0649h.
	[15:0]	1095h	sw:r/-	This unique vendor identification is assigned by CMD Technology, Inc. This field always returns the value 1095h.

Command/Status Register

Address	bit	rst	r/w	Description
04h	0	1b	sw:r/w	Controls a device's response to I/O space accesses as specified in the Base Address Register. Default value is determined by JP6 (Refer to the Bootstrap Jumper section for more details about jumper number 6). 1: Device access to I/O space is enabled (Default) 0: Device access to I/O space is disabled
	1	0b	sw:r/w	Controls a device's response to Memory Space accesses. Default value is determined by JP8 (Refer to the Bootstrap Jumper section for details). 1: Device access to Memory Space is enabled 0: Device access to Memory Space is disabled (Default).
	2	0b	sw:r/w	Controls a device's ability to act as a master on the PCI bus. 1: Enable device to behave as a master on the PCI bus. 0: Disable the device from generating PCI accesses (Default)
	3	0b	sw:r/-	Controls a device's action on special cycle operations. 1: Enable the device to monitor special cycle operations. 0: Disable the device's response to special cycle operations (Default).
	4	0b	sw:r/-	This is an enable bit for using the Memory Write and Invalidate command. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command. 1: Masters may generate the command. 0: Memory Write must be used instead (Default)
	5	0b	sw:r/-	This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. 1: VGA palette snooping is enabled. 0: VGA pallete snooping is viewed as all other accesses (Default).
	6	0b	sw:r/w	This bit controls the device's response to Parity Error. 1: Device must take its normal action when a parity error is detected. 0: Device must set its parity errors detection status bit (bit15 in the status register) when an error occurred but does not assert PERR# and continues its normal operation (Default).
	7	0b	sw:r/-	This bit is used to control whether or not a device does address/data stepping. 1: Devices can do address/data stepping 0: Devices do not do address/data stepping (Default). ***Note:*** *Devices that can do either must make this bit read/write and have it initialize to 1 after RST#*

Address	bit	rst	r/w	Description
	8	0b	sw:r/w	This is the enable bit for the SERR# driver. All devices that have an SERR# pin must implement this bit; also bit6 must be on to report address parity errors when SERR# is 1. 1: Enable SERR# driver 0: Disable SERR# driver (Default)
	9	0b	sw:r/-	This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. 1: Master is allowed to generate fast back-to-back transactions to different agents. 0: Fast back-to-back transactions are only allowed to the same agent (Default).
	[15:10]	000000b		Reserved (end of Command Register Bits)
	[19:16]	0000b		Reserved (beginning of Device Status Register Bits)
	20	1b	sw:r/-	This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34H. 1: This value read at offset 34H is a pointer in configuration space to a linked list of new capabilities (Default). 0: No New Capabilities linked list is available.
	21	0b	sw:r/-	This optional read only bit indicates whether or not the target is capable of running at 66MHz. 0: Target is capable of running at 33MHz (Default) 1: Target is capable of running at 66MHz.
	22			Reserved
	23	1b	sw:r/-	This optional read only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. 1: Device is capable of accepting back-to-back transactions from different agent (Default). 0: Device is not capable of accepting back-to-back transaction from different agent.
	24	0b	sw:r/w	This bit is only implemented by bus master. It is set when three conditions are met: 1). the bus agent asserted PERR# itself on a read or observed PERR# asserted on a write; 2). the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3). the Parity Error Respond bit (Command Register's bit 6) is set 1: Reset 0: No action (Default)
	[26:25]	01b	sw:r/-	These two bits encode the timing of DEVSEL#. 00: Fast timing 01: Medium timing (Default) 10: Slow timing
	27	0b	sw:r/w	This bit must set by a target device whenever it terminates a transaction with target abort. Devices that will never signal target abort do not need to implement this bit. 1: Reset 0: No action (Default)
	28	0b	sw:r/w	This bit must be set by a master device whenever its transaction is terminated with Target Abort. All master devices must implement this bit. 1: Reset 0: No action (Default)

Address	bit	rst	r/w	Description
	29	0b	sw:r/w	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master Abort. All master devices must implement this bit. 1: Reset 0: No action (Default)
	30	0b	sw:r/w; hw: -/w	This bit must be set whenever the device asserts SERR#. Devices who will never assert SERR# do not need to implement this bit. 1: SERR# asserted 0: No SERR# asserted (Default)
	31	0b	sw:r/w	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the command register bit). 1: Reset 0: No action (Default)

Notes: *All other bits are not implemented and will be read back with all zeros; sw denotes software driver; hw denotes hardware*

Class/Revision ID Register

The Class Code register contains the Base Class Code, Sub-Class Code, and Programming Interface fields. These are used to specify the generic function of the PCI-649. The Revision ID register denotes the version of the device.

Address	bit	rst	r/w	Description
08h	31:24	01h	sw:r/-	Class Code's function is Mass Storage.
	23:16		sw:r/w	Sub Class Code: 01-IDE Controller; 04-RAID Controller.
	15:8		sw:r/-	Programming Interface indicates there is nothing special about programming PCI-649. Only defined in IDE mode.
	7:0	01h	sw:r/-	Revision ID denotes the revision number of PCI-649.

Programming Interface Byte Register (PROGIF)

Address	bit	rst	r/w	Description
09h	0	1b	s/w: r/w	Determines the mode that the primary IDE/ATA channel is operating in. 1: Native - PCI mode. 0: Legacy (compatibility mode). This bit is implemented as Read Only if the channel supports only one mode, or Read-Write if both modes are supported. The power up state for this bit (when writable) can either be 0 or 1.
	1	1b	s/w: r/-	This bit indicates whether or not the primary channel has a fixed mode of operation. 1: Channel supports both modes and may be set to either mode by writing bit 0. (JP1 jumper out) 0: Operating mode is fixed and determined by the (Read Only) value of bit 0.
	2	1b	s/w: r/w	Determines the mode that the secondary IDE/ATA channel is operating in. 1: Native-PCI mode. 0: Legacy (compatibility mode). This bit is implemented as Read Only if the channel supports only one mode, or Read-Write if both modes are supported. The power up state for this bit (when writable) can be either 0 or 1.

Address	bit	rst	r/w	Description
	3	1b	sw: r/-	This bit indicates whether or not the secondary channel has a fixed mode of operation. 1: Channel supports both modes and may be set to either mode by writing to bit 2. (JP1 jumper out) 0: Operating mode is fixed and determined by the (Read Only) value of bit 2.
	[7:4]	1000b	sw: r/-	When bit 7 is One, this corresponds to IDE/ATA mode. When Bit7 - 4 are zero, this corresponds to RAID mode. Bit 7 can not be 1 unless register 0AH and 0BH are both 01h.

Notes: *bits [3:0]: are used to toggle between legacy and native modes.*
bits [7:4]: are used to identify the mode of operation, IDE/ATA mode versus RAID mode.
Refer to Appendix D of PCI Specification 2.1 (page 252) and PCI SIG's PCI IDE/ATA controller specification revision 1.0 for the description of the Programming Interface Byte Register.

Only bit 0 and 2 of the configuration register 9 is read/writable at certain condition.

1. When the chip is configured as IDE class device (configuration register 10-11 = 0x0101) bit 0 and 2 are read/writeable; bit 1 and 3 are read only and will be 1 if enable JP1 jumper is set; bit 4-7 will always be 0x80.

   The possible binary value for register 9 is 1000_0x0x if enable JP1 is not set and 1000_1x1x if enable JP1 is set.

2. When the chip is configured as RAID class device (ie. configuration register 0A-0B = 0x0104) configuration register 9 is 0 and is not writeable.

Interrupt Line Register (INTLINE)

Address	bit	rst	r/w	Description
3Ch	31:24	04h	sw:r/-	Maximum Latency specifies how often PCI-649 needs to gain access to the PCI bus. The value is specified in 0.25 µs increments and assumes a 33 MHz clock. 0Fh means PCI-649 needs to gain access to the PCI bus every 130 PCI clocks, expressed as 3.75 µs in this register.
	23:16	02h	sw:r/-	Minimum Grant specifies, in 0.25 µs increments, the minimum burst period PCI-649 needs. PCI-649 does not have any special MIN_GNT requirements. In general, the more channels PCI-649 has active, the worse the bus latency and the shorter the burst cycle.
	15:8	01b	sw:r/-	Interrupt Pin defines which PCI interrupt pin Function 0 uses. 01h means PCI-649 uses pin INTA for HDLC controller interrupts.
	7:0	0Eh	s/w: r/w	Interrupt Line is an eight-bit register used to communicate the interrupt line's routing information. The register is read/write and must be implemented by any device (or device function) that uses an interrupt pin. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific. Default setting: 0EH (1410)

Subsystem Configuration Register (SUBCONF)

Address	bit	rst	r/w	Description
4Fh	0	0b	sw: r/w	Enable write to subsystem ID/subsystem Vendor ID (index 2CH ~ 2FH) 1: Enable 0: Disable (Default)
	1	1b	sw: r/-	Status of signal JP7 at power up reset. Please refer to the bootstrap jumper settings section for more information on jumper number 7. 1: Replace current Subsystem Vendor ID and Product ID (Jumper Open or OUT). 0: Do not overwrite the current Subsystem Vendor ID and Product ID (Jumper Closed or IN).
	2	0b	sw: r/w	Enable write to Class code located at PCI Configuration Register (index 0A-0BH) 1: Enable 0: Disable (Default)
	[7:3]	0b	sw: -/-	Reserved

Notes: *The subsystem ID / subsystem vendor ID registers (index 2Ch ~ 2Fh) are also being shadowed at index 8Ch ~ 8Fh. Read/write to address 2Ch ~ 2Fh will have the same effect as read/write to address 8Ch ~ 8Fh. Whenever there is a change at address 2Ch ~ 2Fh, the content at address 8Ch ~ 8Fh will be updated accordingly and vice versa.*

6.2 Task File Registers

Name	Host Address	Function
HDATA*	1F0h (170)	Data Register (R/W)
HDWPC	1F1h (171)	Write Pre-Comp (Write Only)
HDERR	1F1h (171)	Error Register (Read Only)
HDSCT	1F2h (172)	Sector Count (R/W)
HDSSN	1F3h (173)	Starting Sector Number (R/W)
HDCLL	1F4h (174)	Cylinder Low (R/W)
HDCLH	1F5h (175)	Cylinder High (R/W)
HDSDH	1F6h (176)	SDH (R/W)
HDCMD	1F7h (177)	Command (Write Only)
HDSTT	1F7h (177)	Status (Read Only)
HDFDR	3F6h (376)	Fixed Disk Control Auxiliary Register (Write Only)
HDASR	3F6h (376)	Alternate Status Auxiliary Register (Read Only)

Notes: *Assuming the Base Address is IF0*
**HDATA can be accessed as a 16 - or - 32 bit wide register for all commands.*

6.3 CMD Proprietary IDE/ATA Timing Control Registers for Overall Control

Configuration Register (CFR)

address	Bit	Rst	r/w	description
50h	0	0b		Reserved
	1	0b		Reserved
	2	0b	sw: r/w	Primary channel interrupt status. Write 1 will clear this bit. 1: Interrupt pending 0: No Interrupt pending
	3	0b		Reserved
	4	0b		Reserved
	5	0b		Reserved
	6	1b	sw: r/-	Status of JP1 (please refer to bootstrap jumper section for details) 1: Native mode capable (Default, i.e: Jumper Opened - OUT). 0: Not native mode capable
	7	0b		Reserved

IDE/ATA 8-bits Task File Timing Control Register (CMDTIM)

(The timing control register applies to the 8-bits task file registers on both primary and secondary channels.)

address	Bit	rst	r/w	description
52h	[3:0]	0h	s/w: r/w	IOR/IOW recovery count
	[7:4]	0h	s/w: r/w	IOR/IOW active count

6.4 CMD Proprietary IDE/ATA Timing Control Register for Primary Channel

Control Register for Primary Channel (CNTRL)

address	bit	rst	r/w	Description
51h	0	0b		Reserved
	1	0b		Reserved
	2	1b	sw: r/w	Primary IDE/ATA channel control register. This status is determined by jumper JP3 of the bootstrap jumper setting section. 1: Enable (Jumper Opened : Default) 0: Disable (Jumper Closed)
	3	1b	sw: r/w	Secondary IDE/ATA channel control register. This status is determined by jumper JP4 of the bootstrap jumper setting section. 1: Enable (Jumper closed : Default) 0: Disable (Jumper Opened)
	4	0b		Reserved
	5	1b		Reserved
	6	1b	sw: r/w	Master IDE/ATA drive on primary channel's read ahead control register. (See ARTTIM23) 1: Disable (Default) 0: Enable
	7	1b	sw: r/w	Slave IDE/ATA drive on primary channel's read ahead control register. (See ARTTIM23) 1: Disable (Default) 0: Enable

Status Register for Primary Channel

For information about this register, please refer to Configuration Register, bit2 of index 50h for more details.

PIO IDE/ATA Address Setup Timing Register for Primary Channel's Master Drive (ARTTIM0)

address	bit	rst	r/w	description
53h	[5:0]	000000b	sw: -/-	Reserved
	[7:6]	10b	sw: r/w	Address setup time count 00: 4 clocks 01: 2 clocks 10: 3 clocks (Default) 11: 5 clocks

Notes: *Whichever has the higher count between ARTTIM0 and ARTTIM1 will be selected for the primary channel.*

PIO/MDMA IDE/ATA Data DIOR/DIOW or DMACK Timing Register for Primary Channel's Master Drive (DRWTIM0)

address	bit	rst	r/w	description
54h	[3:0]	0h	s/w: r/w	Recovery Count
	[7:4]	0h	s/w: r/w	Active Count

PIO IDE/ATA Address Setup Timing Register for Primary channel's slave Drive (ARTTIM1)

address	bit	rst	r/w	description
55h	[5:0]	000000b	sw: -/-	Reserved
	[7:6]	11h	sw: r/w	Address setup time count 00: 4 clocks 01: 2 clocks 10: 3 clocks (Default) 11: 5 clocks

Notes: *Whichever has the higher count between ARTTIM0 and ARTTIM1 will be selected for the primary channel. For best performance, it is recommended that both master and slave drives be programmed after each reset.*

PIO/MDMA Data DIOR/DIOW or DMACK Timing Register for Primary Channel's Slave Drive (DRWTIM1)

address	bit	rst	r/w	description
56h	[3:0]	0h	sw: r/w	Recovery Count
	[7:4]	0h	sw: r/w	Active Count

Active Count Conversion Table

Active Count	Read/Write Active Time
0000	16 Clocks
0001	1 Clock
0010	2 Clocks
0011	3 Clocks
0100	4 Clocks
0101	5 Clocks
0110	6 Clocks
0111	7 Clocks
1000	8 Clocks
1001	9 Clocks
1010	10 Clocks
1011	11 Clocks
1100	12 Clocks
1101	13 Clocks
1110	14 Clocks
1111	15 Clocks

Recovery Count Conversion Table

Recovery Count	Read/Write Recovery Time
0000	16 Clocks
0001	2 Clocks
0010	3 Clocks
0011	4 Clocks
0100	5 Clocks
0101	6 Clocks
0110	7 Clocks
0111	8 Clocks
1000	9 Clocks
1001	10 Clocks
1010	11 Clocks
1011	12 Clocks
1100	13 Clocks
1101	14 Clocks
1110	15 Clocks
1111	1 Clock

Notes: *For more information about Ultra DMA IDE/ATA timing control register, please refer to chapter 9 section 7 for additional detail information concerning the PCI Bus Master Control Registers.*

6.5 CMD Proprietary IDE/ATA Timing Control Register for Secondary Channel

Control / Status Register for Secondary Channel (ARTTIM23)

address	bit	rst	r/w	Description
57h	[1: 0]	00b	sw: -/-	Reserved
	2	1b	sw: r/w	Read Ahead capability for Secondary Channel's master IDE/ATA drive. (See CNTRL) 1: Disable (Default) 0: Enable
	3	1b	sw: r/w	Read Ahead capability for Secondary Channel's slave IDE/ATA drive. (See CNTRL) 1: Disable (Default) 0: Enable
	4	0b	sw: r/w	Interrupt status for secondary IDE/ATA Channel. Write 1 will clear this bit. 1: Interrupt Pending 0: No interrupt Pending
	5	0b		Reserved
	[7 : 6]	10b	sw: r/w	Secondary IDE/ATA channel Address Setup Count Register. 00: 4 clocks 01: 2 clocks 10: 3 clocks (Default) 11: 5 clocks

Notes: *Primary disk channel's interrupt status is defined in the Configuration Register, bit2 of index 50H.*

Address Setup Timing Register for Secondary IDE/ATA Channel

For information about these registers, please refer to bit6 and bit7 of the control register for secondary channel for more details. The chip uses these two bits to control both master and slave drive address setup timing, unlike the primary channel where there are two bits for each of master and slave drive.

Data R/W or DACK Timing Register for Secondary Channel's Master Drive (DRWTIM2)

address	bit	rst	r/w	description
58h	[3:0]	0h	s/w: r/w	Recovery Count
	[7:4]	0h	s/w: r/w	Active Count

Read Ahead Count Register (BRST)

address	bit	rst	r/w	description
59h	[7:0]	40h	r/w	This value equals the read-ahead count in quad words. Ex.: 40h x 8 = 200h (512) bytes

Data R/W or DACK Timing Register for Secondary Channel's Slave Drive (DRWTIM3)

address	bit	rst	r/w	description
5Bh	[3:0]	0h	s/w: r/w	Recovery Count
	[7:4]	0h	s/w: r/w	Active Count

Active Count Conversion Table

Active Count	Read/Write Active Time
0000	16 Clocks
0001	1 Clock
0010	2 Clocks
0011	3 Clocks
0100	4 Clocks
0101	5 Clocks
0110	6 Clocks
0111	7 Clocks
1000	8 Clocks
1001	9 Clocks
1010	10 Clocks
1011	11 Clocks
1100	12 Clocks
1101	13 Clocks
1110	14 Clocks
1111	15 Clocks

Recovery Count Conversion Table

Recovery Count	Read/Write Recovery Time
0000	16 Clocks
0001	2 Clocks
0010	3 Clocks
0011	4 Clocks
0100	5 Clocks
0101	6 Clocks
0110	7 Clocks
0111	8 Clocks
1000	9 Clocks
1001	10 Clocks
1010	11 Clocks
1011	12 Clocks
1100	13 Clocks
1101	14 Clocks
1110	15 Clocks
1111	1 Clock

Notes: *For more information about Ultra DMA IDE/ATA timing control register, please refer to chapter 9 section 7 for additional detail information concerning the PCI Bus Master Control Registers.*

6.6 CMD Proprietary Shadow Registers

Shadow Registers for Subsystem ID and Subsystem Vendor ID (08Ch ~ 08Fh)

address	bits	rst	r/w	description
8CH	[7::0]	00h	sw:r/w	Subsystem Vendor ID (LSB)
8DH	[15::8]	00h	sw:r/w	Subsystem Vendor ID (MSB)
8EH	[7::0]	00h	sw:r/w	Subsystem ID (LSB)
8FH	[15::8]	00h	sw:r/w	Subsystem ID (MSB)

6.7 PCI Power Management Registers

Capability ID (CAP_ID)

address	bit	rst	r/w	description
60h	[7:0]	01h	sw: r/-	Capability ID. Each defined capability must have a SIG assigned ID code. These codes are assigned and handled much like the Class Codes. For more details about this and other defined capabilities code, please refer to appendix H of the PCI Local Bus version 2.2. **01**: identifies the linked list item as being the PCI Power Management Registers; however, the value of **01** would be meaningless if the bit 20 of the Command/Status register is not set.

Next Item Pointer (N-I_PTR)

address	bit	rst	r/w	description
61h	[7:0]	00h	sw: r/-	Next Item Pointer - This field provides an offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list. If there are no additional items in the Capabilities List, this register is set to 00H. 00: indicates that there are no additional items in the Capabilities list.

Power Management Capabilities Register (PMC)

address	bit	rst	r/w	description
62h	[2:0]	010b	sw: r/-	Version - a value of 010b indicates that this function complies with revision 1.1 of the PCI Power Management Interface Specification. 010b: indicates that the function is conforms to revision 1.1 of the PCI Power Management interface specification.
	3	0b	sw: r/-	PME Clock - 1: indicates that the function relies on the presence of the PCI Clock for PME# operation 0: indicates that no PCI Clock is required for the function to generate PME#.
	4	0b	sw: r/-	Reserved
	5	1b	sw: r/-	DSI - The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.

Notes: *Bit 5 is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this.*

1: indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
0: indicates that the function is not requires a device specific initialization sequence following transition to the D0 uninitialized state.

address	bit	rst	r/w	description
62h (cont'd)	[8:6]	000b	sw: r/-	Aux_Current - This 3-bit field reports the 3.3Vaux auxiliary current requirements for the PCI function. If the Data Register has been implemented by this function: • Reads of this field must return a value of "000b". • The Data Register takes precedence over this field for 3.3 Vaux current requirement reporting. If PME# generation from D3cold is not supported by the function (PMC(15) = 0), this field must return a value of "000b" when read. For functions that support PME# from D3cold and do not implement the Data Register, the following bit assignments apply: **Bit** — **3.3 Vaux** 8 7 6 — Max. Current Required 1 1 1 — 375 mA 1 1 0 — 320 mA 1 0 1 — 270 mA 1 0 0 — 220 mA 0 1 1 — 160 mA 0 1 0 — 100 mA 0 0 1 — 55 mA 0 0 0 — 0 (Self Powered) (Default)
	9	1b	sw: r/-	D1_Support 1: D1 Power Management State will be supported.
	10	1b	sw: r/-	D2_Support 1: D2 Power Management State will be supported
	[15:11]	00000b	sw: r/-	PME_Support - This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) XXXX1b - PME# can be asserted from D0 bit(12) XXX1Xb - PME# can be asserted from D1 bit(13) XX1XXb - PME# can be asserted from D2 bit(14) X1XXXb - PME# can be asserted from D3hot bit(15) 1XXXXb - PME# can be asserted from D3cold 00000: This indicates that PME# signal is used in not supported any power states.

PCI Functions Power Management State (PMCSP)

address	bit	rst	r/w	description
64h	[1:0]	00b	sw: r/w	Power State - This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b: D0 (Default) 01b: D1 10b: D2 11b: D3
	[7:2]	000000b	sw: r/-	Reserved
	8	0b	sw: r/-	PME_EN 1: Enable the function to assert PME# 0: Disable PME assertion. (Default) ***Notes:*** *This bit defaults to "0" if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.* Functions that do not support PME# generation from any D-state (i.e., PMC(15:11)= "00000b"), may hardwire this bit to be read-only always returning a "0" when read by system software.
	[12:9]	0000b	sw: r/w	Data_Select - This 4-bit field is used to select which data is to be reported through the Data Register and Data_Scale fields. 0 - D0 Power Consumed 1 - D1 Power Consumed 2 - D2 Power Consumed -- data_scale interpretation is 0 or unknown 3 - D3 Power Consumed -- 1 = 0.1x 4 - D0 Power Dissipated -- 2 = 0.01x 5 - D1 Power Dissipated -- 3 = 0.001x 6 - D2 Power Dissipated 7 - D3 Power Dissipated 8 - Common Logic Power Consumption (multi-function PCI devices, Function 0 only) ***Notes:*** *This field is a required component of the Data Register (offset 7) and must be implemented if the Data register is implemented. If the Data Register is not implemented, this field may be hardwired to be read only always returning "0000b" when the PMCSR is read.* *To take advantage of PME function, see Appendix C.*
	[14:13]	11b	sw: r/-	Data_Scale - This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data Register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field. ***Notes:*** *This field is a required component of the Data Register (offset 7) and must be implemented if the Data register is implemented. If the Data Register is not implemented, this field may be hardwired to be read only always returning "0000b" when the PMCSR is read.* 11B: This two bit data_scale field indicates that this function uses 001 as the scale factor to report power.

address	bit	rst	r/w	Description
64h (cont'd)	15	0b	sw: r/w	PME_Status - This bit is set when the function would normally assert the PME# signal independent of the state of the PME_EN bit. ***Notes:*** *Writing a "1" to this bit will clear it and cause the function to stop asserting a PME# (if enabled). Writing a "0" has no effect. This bit defaults to "0" if the function does not support PME# generation from D3cold.* If the function supports PME# from $D3_{cold}$, then this bit is sticky* and must be explicitly cleared by the operating system each time the operating system is initially loaded. * Sticky bit implies the status is indeterminate at time of initial operating system boot if function supports PME# from $D3_{cold}$.

Data Register (DR)

address	bit	rst	r/w	description
67h	[7:0]	F0h	sw: r/-	This read-only Data Register is used to report the state dependent data requested by the Data Select field. The value of this register will always report F0H regardless of what Data_Select field has been programmed. **Consumed:** F0h: D0 Power Consumed, Data_Select field = 0H. (Default) F0h: D1 Power Consumed, Data_Select field = 1H. F0h: D2 Power Consumed, Data_Select field = 2H. F0h: D3 Power Consumed, Data_Select field = 3H. **Dissipated:** F0h: D0 Power dissipated, Data_Select field = 4H. (Default) F0h: D1 Power dissipated, Data_Select field = 5H. F0h: D2 Power dissipated, Data_Select field = 6H. F0h: D3 Power dissipated, Data_Select field = 7H. ***Notes:*** *Please refer to the PCI Power Management interface Specification (Revision 1.1) for detail descriptions.*

6.8 Overall PCI Master Control Registers for both channels

Interrupt Enable and Status Register for both channels & Master Read Select Control Register for both channels (MRDMODE)

address	bit	rst	r/w	description
71h	[1:0]	00b	sw: -/w	Mode of operation 00: Memory Read (Default) 01: Memory Read Multiple 1x: Memory Read Line
	2	0b	sw: r/w	Primary IDE/ATA Channel Interrupt. Write one to clear this bit. 1: Interrupt Pending 0: No interrupt pending
	3	0b	sw: r/w	Secondary IDE/ATA Channel Interrupt. Write one to clear this bit. 1: Interrupt Pending 0: No interrupt pending
	4	0b	sw: r/w	Primary IDE/ATA Channel Interrupt Enable 1: Block Primary IDE/ATA Channel's interrupts. ***Notes:*** *this does not affect the function of bit 2* 0: Propagate Primary IDE/ATA Channel interrupts to ISA_IRQ14 or PCI_INTA# pin (Default).
	5	0b	sw: r/w	Secondary IDE/ATA Channel Interrupt Enable 1: Block Secondary IDE/ATA Channel Interrupts ***Notes:*** *this does not affect the function of bit 3* 0: Propagate Secondary IDE/ATA Channel interrupts to ISA_IRQ15 or PCI_INTA# pin (Default).
	6	0b	sw: r/w	Primary IDE/ATA reset signal status 1: Keep reset signal asserted 0: Keep reset signal de-asserted
	7	0b	sw: r/w	Secondary IDE/ATA bus status 1: Keep reset signal asserted 0: Keep reset signal de-asserted

Notes: *The address for MRDONE can be derived in two ways:*
a). PCI Configuration Space 71H (direct addressing) or
b). Base Address #4 + 01H (indirect addressing)

Bus Master IDE/ATA Control Status Register (BMIDECSR)

address	bit	rst	r/w	description
79h	0	0b	sw: r/-	Primary Channel's 80 pins cable detection bit
	1	0b	sw: r/-	Secondary Channel's 80 pins cable detection bit
	[3:2]	00b	sw: -/-	Reserved
	[5:4]	00b	sw: r/w	FIFO Threshold Control bits for READ (from IDE to PCI) 00b: not empty (Default) 01b: ¼ Full 10b: ½ Full 11b: ¾ Full
	[7:6]	00b	sw: r/w	FIFO Threshold Control bits for WRITE (from PCI to IDE) 00b: not full 01b: ¼ Empty 10b: ½ Empty (Default) 11b: ¾ Empty

6.9 PCI Bus Master Control Register for Primary Channel

Bus Master IDE/ATA Command Register for Primary Channel (BMIDECR0)

address	bit	rst	r/w	Description
70h	0	0b	sw: r/w	DMA Go bit. (Start or Stop Bus Master) 1: Set DMA Go (Enable bus master operation) 0: Clear DMA Go (Disable bus master operation)
	[2:1]	00b	sw: -/-	Reserved
	3	0b	sw: r/w	Read or Write Control 1: PCI bus master writes are performed 0: PCI bus master reads are performed
	[7:4]	0b	sw: -/-	Reserved

Notes: *The address for BMIDECR0 can be derived in two ways:*
a). PCI Configuration Space 70h (direct addressing) or
b). Base Address #4 + 00h (indirect addressing)

Bus Master IDE/ATA Status Register for Primary Channel (BMIDESR0)

address	bit	rst	r/w	description
72h	0	0b	sw: r/-	Bus Master IDE/ATA Active 1: DMA Engine still active. 0: DMA Engine not active.
	1	0b	sw: r/w	Errors 1: Error (Write one to clear error). 0: No Errors.
	2	0b	sw: r/w	DMA Interrupt 1: Interrupt generated on IDE/ATA bus for DMA transfer (software writes one to clear this bit). 0: No Interrupt occurs on IDE/ATA bus for DMA transfer.
	3	0b		Reserved (See bit 0 of index 79h for more information)
	4	0b		Reserved
	5	0b	sw: r/w	Primary master IDE/ATA drive is DMA capable 1: DMA Capable 0: Not DMA Capable
	6	0b	sw: r/w	Primary slave IDE/ATA drive is DMA capable 1: DMA Capable 0: Not DMA Capable
	7	0b	sw: r/-	Simplex only

Notes: *The address for BMIDESR0 can be derived in two ways:*
a). PCI Configuration Space 72h (direct addressing) or
b). Base Address #4 + 02h (indirect addressing)

Ultra DMA IDE/ATA Timing Control Register for Primary Channel (UDIDETCR0)

address	bit	rst	r/w	description
73h	0	0b	sw: r/w	Primary IDE/ATA Channel Master Drive DMA Mode 1: Ultra DMA 0: Multiword DMA (Default)
	1	0b	sw: r/w	Primary IDE/ATA Channel Slave Drive DMA Mode 1: Ultra DMA 0: Multiword DMA (Default)
	2	0b	sw: r/w	Primary IDE/ATA Channel Master Drive Clock Cycle Resolution 1: (for Ultra DMA mode 3,4,5) 0: (for Ultra DMA mode 0,1,2)
	3	0b	sw: r/w	Primary IDE/ATA Channel Slave Drive Clock Cycle Resolution 1: (for Ultra DMA mode 3,4,5) 0: (for Ultra DMA mode 0,1,2)
	[5:4]	11b	sw: r/w	Primary IDE/ATA Channel Master Drive Ultra DMA Cycle Time When bit [2] is set to 0: 00: Reserved 01: Ultra DMA mode 2 10: Ultra DMA mode 1 11: Ultra DMA mode 0 (Default) When bit [2] is set to 1: 00: Ultra DMA mode 5 01: Ultra DMA mode 4 10: Ultra DMA mode 3 11: Reserved
	[7:6]	11b	sw: r/w	Primary IDE/ATA Channel Slave Drive Ultra DMA Cycle Time When bit [3] is set to 0: 00: Reserved 01: Ultra DMA mode 2 10: Ultra DMA mode 1 11: Ultra DMA mode 0 (Default) When bit [3] is set to 1: 00: Ultra DMA mode 5 01: Ultra DMA mode 4 10: Ultra DMA mode 3 11: Reserved

Notes: *The address for UDIDETCR0 can be derived in two ways:*
a). PCI Configuration Space 73h (direct addressing) or
b). Base Address #4 + 03h (indirect addressing)

Descriptor Table Pointer Register for Primary Channel (DTPR0)

address	bit	rst	r/w	description
74h	[1:0]	00b		Reserved
	[31:2]		sw: r/w	Base address of Descriptor Table (0FCH)

Notes: *The address for DTPR0 can be derived in two ways:*
a). PCI Configuration Space 74h (direct addressing) or
b). Base Address #4 + 04h (indirect addressing)9.10 PCI Bus Master Control Register for Secondary Channel

6.10 Bus Master IDE/ATA Control Register for Secondary Channel

Bus Master IDE/ATA Status Register for Secondary Channel (BMIDECR1)

address	bit	rst	r/w	description
78h	0	0b	sw: r/w	DMA Go Bit (Start or Stop Bus Master) 1: Set DMA Go (Enable bus master operation) 0: Clear DMA Go Bit (Disable bus master operation)
	[2:1]	00b		Reserved
	3	0b	sw: r/w	Read or Write Control 1: PCI bus master writes are performed 0: PCI bus master reads are performed
	[7:4]	0b		Reserved

Notes: *The address for BMIDECR1 can be derived in two ways:*
a). PCI Configuration Space 78h (direct addressing) or
b). Base Address #4 + 08h (indirect addressing)

Bus Master IDE/ATA Status Register for Secondary Channel (BMIDESR1)

address	bit	rst	r/w	description
7A	0	0b	sw: r/w	Bus master IDE/ATA active 1: DMA engine still active 0: DMA engine not active
	1	0b	sw: r/w	Errors 1: Error (Write one to clear this bit) 0: No Error
	2	0b	sw: r/w	DMA Interrupt 1: Interrupt generated on IDE/ATA bus for DMA transfer (software write ones to clear bit) 0: No interrupt occurs on IDE/ATA bus for DMA transfer.
	3	0b		Reserved (See bit 1 of index 79h for more information)
	4	0b		Reserved
	5	0b	sw: r/w	Secondary Master IDE/ATA drive is DMA capable 1: DMA Capable 0: Not DMA Capable
	6	0b	sw: r/w	Secondary Slave IDE/ATA drive is DMA capable 1: DMA Capable 0: Not DMA Capable
	7	0b	sw: r/-	Simplex Only

Notes: *The address for BMIDESR1 can be derived in two ways:*
a). PCI Configuration Space 7Ah (direct addressing) or
b). Base Address #4 + 0Ah (indirect addressing)

Ultra DMA IDE/ATA Timing Control Register for Secondary Channel (UDIDETCR1)

address	bit	rst	r/w	description
7Bh	0	0b	sw: r/w	Secondary IDE/ATA Channel Master Drive DMA Mode 1: Ultra DMA 0: Multiword DMA (Default)
	1	0b	sw: r/w	Secondary IDE/ATA Channel Slave Drive DMA Mode 1: Ultra DMA 0: Multiword DMA (Default)
	2	0b	sw: r/w	Secondary IDE/ATA Channel Master Drive Clock Cycle Resolution 1: (for Ultra DMA Mode 3, 4, 5) 0: (for Ultra DMA Mode 0, 1, 2)
	3	0b	sw: r/w	Secondary IDE/ATA Channel Slave Drive Clock Cycle Resolution 1: (for Ultra DMA Mode 3, 4, 5) 0: (for Ultra DMA Mode 0, 1, 2)
	[5:4]	11b	sw: r/w	Secondary IDE/ATA Channel Master Drive Ultra DMA Cycle Time When bit [2] is set to 0: 00: Reserved 01: Ultra DMA mode 2 10: Ultra DMA mode 1 11: Ultra DMA mode 0 (Default) When bit [2] is set to 1: 00: Ultra DMA mode 5 01: Ultra DMA mode 4 10: Ultra DMA mode 3 11: Reserved
	[7:6]	11b	sw: r/w	Secondary IDE/ATA Channel Slave Drive Ultra DMA Cycle Time When bit [3] is set to 0: 00: Reserved 01: Ultra DMA mode 2 10: Ultra DMA mode 1 11: Ultra DMA mode 0 (Default) When bit [3] is set to 1: 00: Ultra DMA mode 5 01: Ultra DMA mode 4 10: Ultra DMA mode 3 11: Reserved

Notes: *The address for UDIDETCR1 can be derived in two ways:*
a). PCI Configuration Space 7Bh (direct addressing) or
b). Base Address #4 + 0Bh (indirect addressing)

Descriptor Table Pointer Register for Secondary Channel (DTPR1)

address	bit	rst	r/w	description
7Ch	[1:0]	00b		Reserved
	[31:2]		sw: r/w	Base Address of Descriptor Table

Notes: *The address for DTPR1 can be derived in two ways:*
a). PCI Configuration Space 7Ch (direct addressing) or
b). Base Address #4 + 0Ch (indirect addressing)

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7. Electrical Specifications

7.1 DC Specifications

Maximum Ratings

Symbol	Parameter	Limits	Units
V_{DD}	DC supply voltage	-0.3 to +4.0	Volts
V_{in}	DC Input Voltage	-0.3 to +6.0	Volts
T_{stg}	Storage Temperature	-40 to +125	Deg. C
I_{in}	DC Input Current	±10	µA

Operating Conditions (V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply voltage	3.0	3.6	Volts
I_{DD}	Typical Operating Supply Current	0	44	mA
V_{in}	Input Voltage	Vss	V_{DD}	Volts
T_{opr}	Operating Temperature	0	+70	°C
P_{DISS}	Power Dissipation		145 (typ)	mW

7.2 DC Characteristics (For V_{DD}= 3.3V, 0 to 70°C)

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Voltage Low	-0.3	0.8	Volts	Note 2
V_{IH}	Input Voltage High	2.0	5.5	Volts	Note 2
V_{OL}	Output Voltage Low		0.40	Volts	Note 3
V_{OH}	Output Voltage High I_{OH} = -2mA	2.4		Volts	Note 1
I_{LO}	Output Leakage Current	-10	10	µA	
I_{LI}	Input High Current $V_{in} = V_{DD}$	-10	10	µA	
I_{IL}	Input Low Current $V_{in} = V_{SS}$	-10	10	µA	
C_{IN}	Input or I/O Capacitance		10	pF	

NOTES: (1) All PCI signals are PCI-compliant driver pins. Refer to PCI specifications. (2) C_X_INTRQ, C_X_DMARQ, C_X_DD[0..15], C_X_IORDY, C_X_CBLID#, PCI_RST#, JP [0..4], and Jp8 are TTL Schmitt trigger pins. (3) IOL=8mA: C1_CS1#, C1_CS0#, C0_CS1#, C0_CS0#, ISA_IRQ14, ISA_IRQ15, Cx_RESET#, Cx_DA[0..2], C0_DIOR#, C0_DIOW#, C1_DIOR#, C1_DIOW#, Cx_DD[0..15], C0_DMACK# and C1_DMACK#. (For Notes 2 & 3, replace the variable 'x' with either channel 0 or channel 1 whenever appropriate.)

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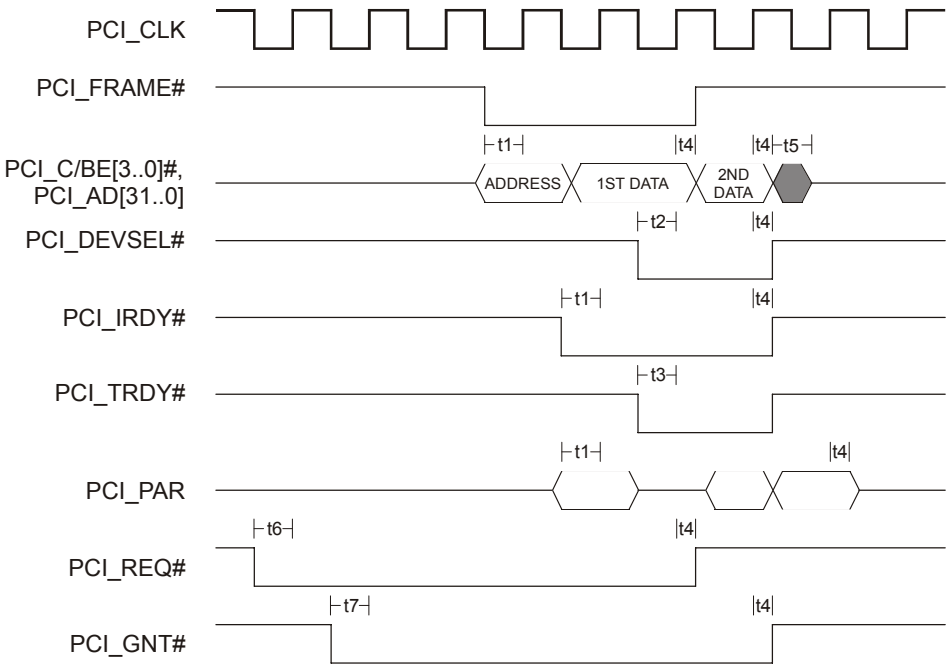
8. PCI DMA Master Read Timing (33MHz PCI_CLK)

DMA Read Signal Diagram



Symbol	Parameter	Timing
t1	PCI_FRAME#, PCI_IRDY#, PCI_C/BE[3..0]#, PCI_AD[31..0], PCI_PAR setup time	7 ns
t2	PCI_DEVSEL# setup time	4-11 ns
t3	PCI_TRDY# setup time	3-10 ns
t4	PCI_AD[31..0], PCI_FRAME#, PCI_IRDY#, PCI_C/BE[3..0]#, PCI_DEVSEL#, PCI_TRDY#, PCI_PAR, PCI_REQ#, PCI_GNT# hold time from rising edge of PCI_CLK.	4-11 ns
t5	Active to float delay from PCI_CLK	3-10 ns
t6	PCI_REQ# setup time	4-11 ns
t7	PCI_GNT# setup time	8-28 ns

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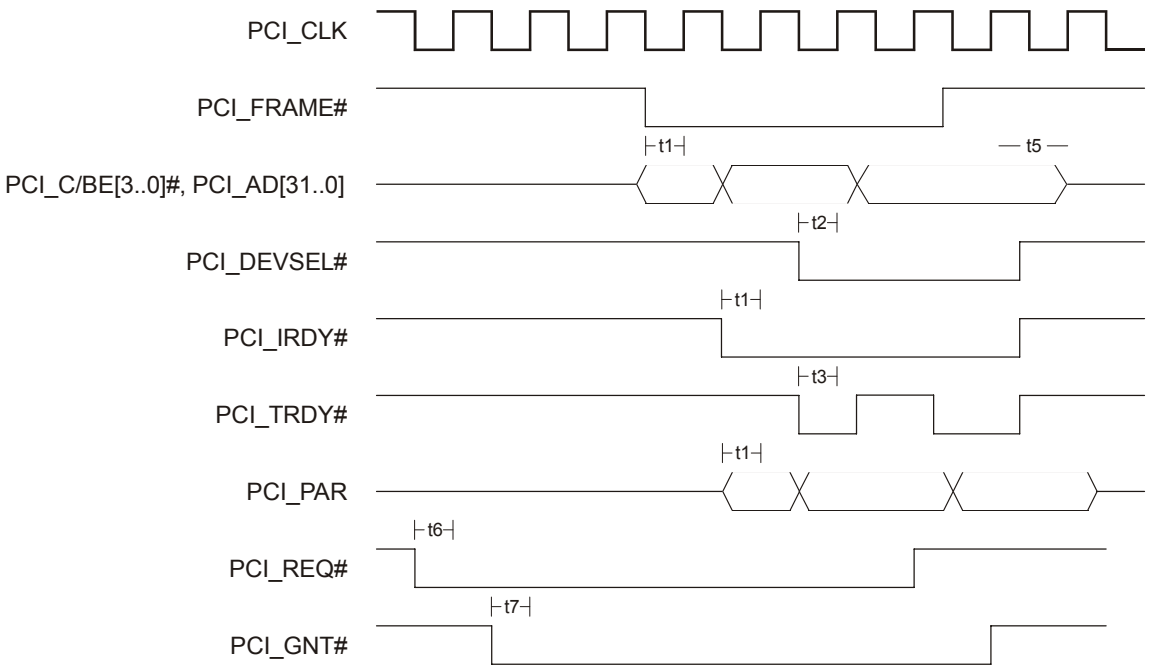
9. PCI DMA Master Write Timing (33MHz PCI_CLK)

DMA Write Signal Diagram



Symbol	Parameter	Timing
t1	PCI_FRAME#, PCI_IRDY#, PCI_C/BE[3..0]#, PCI_AD[31..0], PCI_PAR setup time	7 ns
t2	PCI_DEVSEL# setup time	4-11 ns
t3	PCI_TRDY# setup time	3-10 ns
t4	PCI_AD[31..0], PCI_FRAME#, PCI_IRDY#, PCI_C/BE[3..0]#, PCI_DEVSEL#, PCI_TRDY#, PCI_PAR, PCI_REQ#, PCI_GNT# hold time from rising edge of PCI_CLK.	4-11 ns
t5	Active to float delay from PCI_CLK	3-10 ns
t6	PCI_REQ# setup time	4-11 ns
t7	PCI_GNT# setup time	8-28 ns

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10. Appendix A

10.1 Timing Settings Guide

This appendix is included to assist device driver developers in programming proper timing settings for the PCI-649 chip.

10.2 Setting the Drive Mode

To determine what data transfer mode an ATA or ATAPI drive supports, you have to issue either an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command to the drive. Words 53, 63 or 88 of identify device information will specify the fastest mode it supports. Refer to the ATA/ATAPI-5 specification for a description of that information.

To set the drive to the desired data transfer mode, issue a SET FEATURE command to the drive. Refer to the ATA/ATAPI-5 specification for a description of that command.

Timing Table

The following table describes the minimum timing parameters required for different PIO, MDMA and UDMA mode settings. All times are expressed in nanoseconds (ns).

Mode	Cycle Time	Address setup for DIOR/DIOW (ARTTIM register)	8-bit DIOR/DIOW active time (CMDTIM-active)	8-bit DIOR/DOIOW recovery time (CMDTIM-recovery)	16-bit DIOR/DIOW active time (DRWTIM-active)	16-bit DIOR/DOIOW recovery time (DRWTIM-recovery)
PIO 0	600	70	290	--	165	--
PIO 1	383	50	290	--	125	--
PIO 2	240	30	290	--	100	--
PIO 3	180	30	80	70	80	70
PIO 4	120	25	70	25	70	25
MDMA 0	480	*	*	*	215	265
MDMA 1	150	*	*	*	80	--
MDMA 2	120	*	*	*	70	--
UDMA 0	112	*	*	*	n/a	n/a
UDMA 1	73	*	*	*	n/a	n/a
UDMA 2	54	*	*	*	n/a	n/a
UDMA 3	39	*	*	*	n/a	n/a
UDMA 4	25	*	*	*	n/a	n/a
UDMA 5	17	*	*	*	n/a	n/a

NOTE: *In this timing table, the sum of active time and recovery time may be greater or smaller than cycle time. The important point is that wherever applicable, cycle time, active time, and recovery time for any mode setting has to be equal or greater than the appropriate entry in the above table.*

Since all access to task file registers are by PIO, you can calculate the values for the entries marked with "*" based on the default PIO mode of the drive obtained from identify device information, even though the drive is programmed to do DMA data transfer. The entries marked with "--" mean there is no specified value. These values can be calculated by subtracting active time from cycle time.

Once the drive mode is determined, program the PCI-649 timing registers and other related registers as necessary. Ensure that the drive is set to the proper mode before programming the PCI-649 timing registers.

10.3 Register Set-up for PIO/MDMA Timing

Four registers need to be programmed in order to setup the PCI-649 chip to operate in PIO, MDMA or UDMA modes. These registers are: CMDTIM, ARTTIMx, DRWTIMx and UDIDETCRx.

IDE/ATA Task File Timing Control Register (CMDTIM)

The following is a description of how the timing registers should be programmed. This is based on a PCI bus speed of 33MHz and a clock cycle of 30 nsec. Moreover, the process of setting up these registers will affect or change the task file register's access timing for the primary and secondary channels. Lastly, the offset for the CMDTIM register is 0x52h.

The IDE/ATA task file registers must be accessed by PIO regardless of what data transfer type the drive is programmed to accept. There are some older drives that may not report correct data when the CMDTIM register is programmed to operate at the fastest PIO mode. In such instances, it is safe to program the register based on the drive's default PIO mode.

If the default PIO mode of the drive is 2, this register should be programmed to 0xAFh. The upper 4 bits of this register represent an active time of 10 clocks (300 nsec) which is the minimum time greater than 290 nsec. The lower 4 bits represent a recovery time of 1 clock. There is no 0 clock of recovery time defined and the minimum is 1.

If the default PIO mode of the drive is 3, this register should be programmed to 0x32h. The upper 4 bits of this register represent an active time of 3 clocks (90 nsec) which is the minimum time greater than 80 nsec. The lower 4 bits represent a recovery time of 3 clocks (90 nsec) which is the minimum time greater than or equal to 90 nsec (cycle time - active time; or 180 nsec - 90 nsec = 90 nsec.)

The time specified by this register constitutes a negligible portion to the whole data transfer time. Even if this register is programmed to the slowest PIO mode timing, there should be no performance penalty.

Drive x Address Setup Register (ARTTIMx) for PIO modes

There are three designated registers for this purpose. The registers, ARTTIMx, are located at the following offsets: 0x53h, 0x55h, 0x57h. The variable 'x' in ARTTIMx represents the drive number. If the variable 'x' equals 0 or 1, it represents master or slave drive of primary channel respectively. If it is 23, it represents master and slave drive of secondary channel. This register reflects the address set up time for IDE/ATA Task File access. Like the CMDTIM register, this register has to follow PIO timing requirements, no matter what data transfer type the drive is programmed to.

If the default PIO mode of the device is 1, this register should be set to 0x40h (2 clocks). The 60nsec address set up time is greater than the minimum requirement of 50nsec for PIO mode 1. Drive 2 and drive 3 in the secondary channel share the same address setup count. Bit 6-7 of ARTTIM23 register should be programmed to the slower default PIO timing of the two drives.

The time specified by this register constitutes a negligible portion to the whole data transfer time. The performance difference is insignificant, even if this register is programmed to a longer time.

Drive x DIOR/DIOW or DACK Timing Register (DRWTIMx) for PIO/MDMA Modes

There are four designate registers for this purpose. The registers, DRWTIMx, are located at the following offsets: 0x54h, 0x56h, 0x58h and 0x5Bh. The variable 'x' represents the drive number. If the variable 'x' equals to 0 or 1, it represents master or slave drive of primary channel respectively. If it is 2 or 3, it represents master/slave drive of secondary channel. If the drive is set to Multiword DMA mode 2, this register should be programmed to 0x3Fh. The upper 4 bits of this register represent an active time of 3 clocks (90nsec) which is the minimum time greater than 70nsec. The lower 4 bits represent a recovery time of 1 clock (30nsec) which is the minimum time greater than or equal to 30nsec (recovery time = cycle time - active time; or 120nsec - 90nsec = 30nsec.)

If the drive is set to PIO mode 4, this register should be programmed to 0x3Fh. The upper 4 bits of this register represent an active time of 3 clocks (90nsec) which is the minimum time greater than 70nsec. The lower 4 bits represent a recovery time of 1 clock (30nsec) which is the minimum time greater than or equal to PIO mode 4 recovery time (25nsec). The sum of active and recovery time equals cycle time.

Channel x in Ultra DMA IDE/ATA Timing Control Registers (UDIDETCRx)

Bit 0 and bit 1 of this register need to be 0 in order for the channels to be in MDMA mode.

10.4 Register Set-Up for UDMA Timing

In order to set the PCI-649 chip to operate in Ultra DMA mode, the following two registers need to be programmed, CMDTIM and UDIDETCRx registers. Also, all the task file registers will be programmed through default PIO mode timing specified in section 6.3, the IDE/ATA Task File Timing Control Register (CMDTIM).

IDE/ATA Task File Timing Control Register (CMDTIM)

Please refer to the previous section of the IDE/ATA Task File Timing Control Register for more information.

Channel x Ultra DMA IDE/ATA Timing Control Registers (UDIDETCRx)

These two registers need to be programmed in order to set the channel into UDMA operating modes. The two registers are UDIDETCR0 for primary channel and UIDETCR1 for secondary channel.

This register is used only when the drive is set to run in Ultra DMA mode. If this register is used for a certain drive, the corresponding DRWTIM register for that drive will be invalid. Set either bit 0 and/or bit 1 of this register depending on which drive(s) you want to interface with in Ultra DMA timing. Set either bit 2 or bit 3 depending on the Ultra DMA mode.

If the master drive is set to UDMA mode 2, bits 4-5 should be programmed to 01b and bit 2 should be set to 0. The host will strobe data out every 60 nsec, which is the minimum time greater than the 55nsec cycle time for UDMA mode 2.

If the master drive transfers data using UDMA mode 5, bits 4-5 should be programmed to 00b and bit 2 should be set to 1. The host will strobe data out every 20 nsec, which is the minimum for UDMA mode 5.

The following table shows how to program the UDIDETCRx registers for master drive to the primary channel to operate in either UDMA33, UDMA66 or UDMA100 modes.

bit (7:6)	bit (5:4)	bit 3	bit 2	bit 1	bit 0	UDMA Mode		HSTROBE sustained cycle time (nsec)		Minimum DSTROBE cycle time (nsec)	
1 1	1 1	0	0	1	1	M: S:	Mode 0 Mode 0	M: S:	120 120	M: S:	112 112
1 0	1 1	1	0	1	1	M: S:	Mode 0 Mode 3	M: S:	120 45	M: S:	112 39
1 0	0 1	0	1	1	1	M: S:	Mode 4 Mode 1	M: S:	30 90	M: S:	25 73
0 1	1 0	1	1	1	1	M: S:	Mode 3 Mode 4	M: S:	45 30	M: S:	39 25
0 1	0 0	0	1	1	1	M: S:	Mode 5 Mode 2	M: S:	20 60	M: S:	17 54

NOTES: *1). M denotes master drive, and S denotes slave drive*
2). HSTROBE sustained cycle time is the HSTROBE output from the PCI-649 chip during an IDE/ATA WRITE operation
3). Minimum DSTROBE cycle time is the minimum DSTROBE input from the device that the PCI-649 chip can accept and work with during an IDE/ATA READ operation.
4). Unless otherwise indicated, all data content is shown in Hexadecimal. b indicates data content is in binary format.

10.5 Recommended PIO Mode and Task File Register Settings (Applicable for ICS-000649-C01 and ICS-000649-C02)

The IDE Specification enumerates the command recovery time for each PIO mode. This recovery time is the time between any read or write cycle on the IDE bus. It is the responsibility of the driver to ensure that the recovery time is met. If, however, the recovery time is not met, the 649 will terminate the read or write cycle with the STOP signal (on the PCI bus), which will cause the offending cycle to be retried. When the cycle is retried, if the recovery time is still not met, the cycle will again terminate with the STOP signal and another retry will occur. This will continue until the recovery time is met, at which point the cycle will complete normally. If, however, the cycle to be retried is a "delayed write" cycle, the STOP signal is not asserted, which causes the PCI bus to hang. A delayed write cycle is a PCI write cycle in which IRDY is not asserted one clock after FRAME, but some number of clocks later (causing "wait states" on the PCI bus).

To avoid the potential PCI bus hang, care must be taken in the driver to ensure that the command recovery time is met. If, however, the system design can guarantee that delayed write cycles will never occur, then retries will work properly without a PCI bus hang, even though the driver violates the specified command recovery time.

The recommended PIO mode timing register settings are as follows:

PCI-649 Registers/PIO mode	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4
52h [3:0]Task File Register Recovery	2	2	2	2	F
52h [7:4]Tash File Register Active	0	A	A	3	3
53h [7:6]1Channel Master Address Setup	2	1	1	1	1
54h [3:0]1Channel Master Recovery	2	2	2	2	F
54h [7:4]1Channel Master Active	0	A	5	3	3
55h [7:6]1Channel Slave Address Setup	2	1	1	1	1
56h [3:0]1Channel Slave Recovery	2	2	2	2	F
56h [7:4]1Channel Slave Active	0	A	5	3	3
57h [7:6]2Channel Master/Slave Address Setup	2	1	1	1	1
58h [3:0]2Channel Master Recovery	2	2	2	2	F
58h [7:4]2Channel Master Active	0	A	5	3	3
5Bh [3:0]2Channel Slave Recovery	2	2	2	2	F
5Bh [7:4]2Channel Slave Active	0	A	5	3	3

11. Appendix B: Miscellaneous Design Notes

11.1 Configuration Setup

Depending on your motherboard chip set, either Configuration Mechanism #1 or Configuration Mechanism #2 is applicable. Configuration Mechanism #2 is described below. For Configuration #1 methodology, refer to the PCI Spec 2.2.

Notes: *1) Although PCI BIOS (INT 1Ah) is a portable alternative to mechanism #1 and #2, it is not recommended because MS-DOS's EMM386.SYS causes the system to hang when function FIND PCI DEVICE is accessed.*

2) The PCI-649 supports byte, word, and dword reads/writes of configuration space.

11.2 Configuration Mechanism #2

1) Enter PCI Configuration Mode by writing 10h to port CF8h.

2) Scan the PCI device IDs from 0h to Fh for the presence of a PCI-649 controller. (There should be 1095h in port Cx00h and 0648h in port Cx02h, where x=device index.) For other devices and configurations, refer to Section 1.2 to determine the proper Device ID to be used.

3) To read or write internal registers, read or write to port Cxyyh, where x = device ID from (2) and yy = configuration register's index.

4) Exit PCI Configuration Mode by writing 00 to port CF8h.

11.3 PIO Mode Interrupt Processing

When JP1 (Number 1 of the jumper setting section) is pulled low during reset, both IDE/ATA ports are in PCI IDE/ATA Legacy Mode. When this JP1 has no pull-down during reset, each IDE/ATA port may independently be set to PCI IDE/ATA Legacy Mode or Native Mode via the Programming Interface Byte (configuration register PROGIF, Index 9h).

When an IDE/ATA port is in PCI IDE/ATA Legacy Mode, the PCI-649 is compatible with standard ISA IDE/ATA. The IDE/ATA task file registers are mapped to the standard ISA port addresses, and IDE/ATA drive interrupts occur at IRQ14 (primary) or IRQ15 (secondary).

When an IDE/ATA port is in PCI IDE/ATA Native Mode, the IDE/ATA task file registers may be mapped to non-standard port addresses, and IDE/ATA drive interrupts occur at PCI INTA#. Therefore, if both IDE/ATA ports are in PCI IDE/ATA Native Mode, drive interrupts from both IDE/ATA ports are multiplexed into PCI INTA#. In this case, the interrupt status bits must be polled to determine which IDE/ATA port generated the interrupt, or whether the interrupt was generated by another PCI device sharing INTA# on the bus.

1) The host reads CFR (index 50h). If bit 2 is set, then the interrupt occurred on the primary IDE/ATA port.

2) The host reads ARTTIM23 (index 57h). If bit 4 is set, then the interrupt occurred on the secondary IDE/ATA port.

3) If 1) and 2) are both false, then the interrupt was generated by another PCI device sharing INTA# with the PCI-649.

NOTE: *The interrupt status of each channel can also be determined by the value of either bit 2 or bit 3 in the MRDMODE register. This register is one of the PCI Master Control registers and may be accessed through the I/O space provided that the value of Base Address #4 is valid. This is a safer, more efficient method of accessing the interrupt status in a multitasking environment.*

11.4 DMA Programming

Refer to Revision 1.0 of Intel's "Programming Interface for Bus Master IDE/ATA Controller" for information about bus master DMA programming.

11.5 Read Ahead Operation

The chip will snoop the IDE/ATA command register. If a read or read multiple command is written to it, then the chip will load the readahead count according to the current BRST register (index 59h) setting.

12. Appendix C: Deviations from the Specification

Deviations from the Specification

Part Number	Item	Deviation Description
ICS-000649-C01/C02/CA1	1	In PIO mode 0, minimum cycle time (t0) is 600ns. However, the host controller needs to be programmed to 570ns instead of 600ns for proper operation (please refer to section 10.5). User impact: No hard drive or other peripheral device has been found that fails due to this deviation. As long as the device can respond within 570ns in PIO mode 0, it will operate properly. Workaround: No workaround required.
ICS-000649-C01/C02/CA1	2	In Ultra mode 5, TLI (Limited Interlock time) is to be between 0 and 75ns according to ATA/ATAPI-6 specification. If the device terminates an Ultra DMA data IN burst, TLI (from DMARQ to STOP) can be as high as 83ns. User impact: No data loss will occur since all the data has been transferred and the device is waiting for DMACK and CRC from the host controller. Workaround: No workaround required.
ICS-000649-C01/C02/CA1	3	When the PCI configuration Command register is loaded with a 0000h, only PCI configuration read and write commands are allowed. However, when loaded to this value, the host controller still responds to I/O read and write commands. User impact: None Workaround: No workaround required.
ICS-000649-C01/C02/CA1	4	Host controller does not set the Signaled Target Abort bit of the Status register when it generates a Target Abort. User impact: None Workaround: No workaround required.

Part Number	Item	Deviation Description
ICS-000649-C00	1	There is a design deviation in the PCI-649 (ICS-000649-C00 only) that may cause a system malfunction under certain conditions. For every I/O register access of the PCI-649, if the PCI host asserts the FRAME# longer than two PCI clock cycles, the PCI-649 will decode the wrong address. Specifically, the PCI-649 will latch and decode the AD bus again at the third clock, at which time the AD bus no longer holds a valid address. This will cause the I/O register access to fail, which may prevent the internal DMA GO bit from being set, and hang the following DMA transfer. This deviation has been corrected in the subsequent versions of the PCI-649.
ICS-000649-C00	2	In Ultra mode 5, TLI (Limited Interlock time) is to be between 0 and 75ns according to ATA/ATAPI-6 specification. If the device terminates an Ultra DMA data IN burst, TLI (from DMARQ to STOP) can be as high as 83ns. User impact: No data loss will occur since all the data has been transferred and the device is waiting for DMACK and CRC from the host controller. Workaround: No workaround required.
ICS-000649-C00	3	When the PCI configuration Command register is loaded with a 0000h, only PCI configuration read and write commands are allowed. However, when loaded to this value, the host controller still responds to I/O read and write commands. User impact: None Workaround: No workaround required.
ICS-000649-C00	4	Host controller does not set the Signaled Target Abort bit of the Status register when it generates a Target Abort. User impact: None Workaround: No workaround required.