ULi

M5282

Parallel-ATA Host Controller

Datasheet

NOTICE

TRADEMARK ACKNOWLEDGMENTS

Revision History

Date	Revision	Description	Notes
9/3/2004	0.91	Initial release.	

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Table of Contents

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1. Introduction

1.1 Overview

The M5282 provides personal computer systems with PCI device solution of the highest integration: It includes two controllers: one is a full Parallel-ATA Host controller for supporting two channels, and the other is a Flash ROM controller.

The M5282 provides PCI interface up to 33 MHz and is PCI specification 2.2 compliant. In addition, the M5282 supports CLKRUN# function for mobile applications, which stops PCICLK when there is no activity on the PCI bus. M5282 also supports 32-bit bus mastering CardBus interface that operates up to 33 MHz.

1.2 Features

Parallel-ATA Interface
- Supports Ultra DMA Mode Transfers up to Mode 6 Timing (133 Mbytes/sec).
- Supports 48-bit LBA (Large Disk), hard driver larger than 137 GB.
- Supports PIO Modes up to Mode 4 Timings, and Multiword DMA Mode 0,1,2 with Independent Timing of up to 2 drives.
- Supports Tri-state IDE Signals.

PCI Bus Interface
- Compliant with PCI Specification revision 2.2.
- Supports up to 33 MHz PCI interface clock.
- Supports PCI mobile CLKRUNJ function.
- High performance PCI bus master.

Flash ROM Interface
- Supports up to 64K Flash ROM.
- Supports both Read/Write cycle.

CardBus Interface
- PC card 32-bit CardBus interface.

Other
- Supports Daisy Chain structure up to 3 chips in one PCI slot/device.

0.18 um CMOS process

1.8 V core, 3.3 V I/O, 5V tolerant input

128-pin LQFP Package

1.3   System Configuration

Figure below shows the system block diagram of ULi solution with the M5282. Through the high integration of the M5282, board designers can build a cost-effective motherboard with the rich features of SATA and PATA functions.
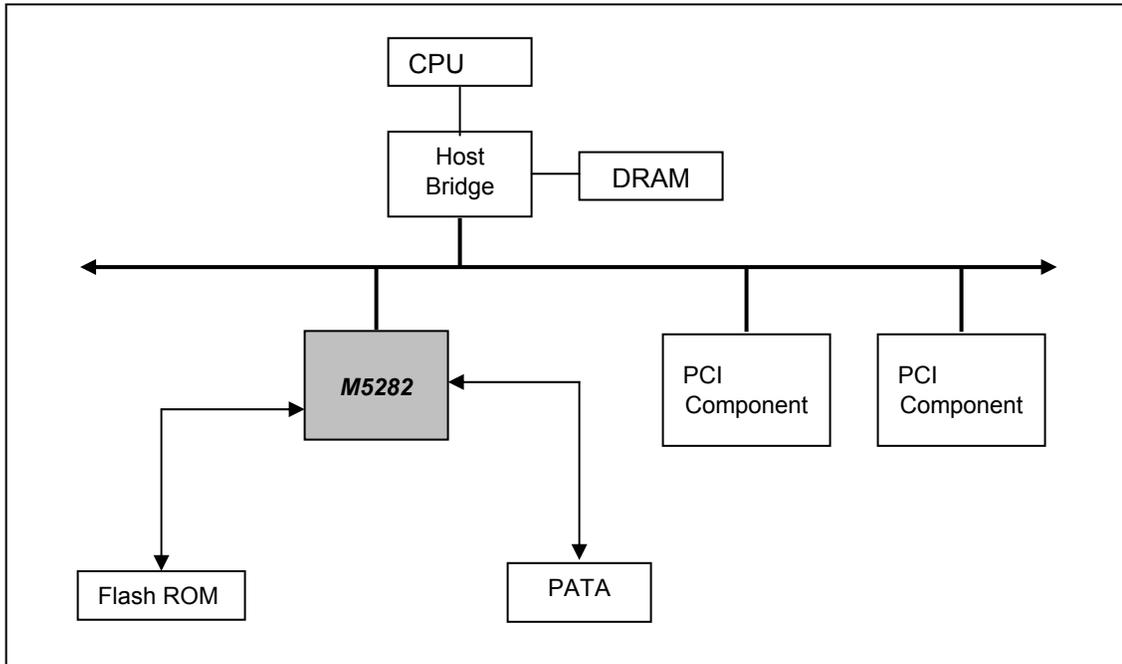
2. Pin Description

2.1 Signal Description

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. Throughout this manual, a '#' will be used at the end of a signal name to indicate that the active, or asserted state occurs when the signal is at a low voltage level.

The following notations are used to describe the signal and type.

I	Input pin
O	Output pin
I/O	Bi-directional pin
OD	Open-Drain Output pin

2.1.1 PCI Interface

Pin Name	Pin No.	Type	Power Region	Description
PCIRST#	143	I	PCI	**PCI Bus Reset**.
PCICLK	145	I	PCI	**PCI Clock** for internal PCI Bus interface. The central resource can stop this clock after the CLKRUN# querying protocol.
AD[31-0]	148, 149, 150, 152, 153, 154, 155, 156, 160, 1, 2, 3, 4, 6, 7, 8, 21, 22, 23, 24, 25, 27, 28, 29, 31, 32, 34, 35, 36, 37, 38, 39	I/O	PCI	**Address and Data** are multiplexed on the PCI bus. During the first clock of a PCI transaction, AD[31-0] contains a physical address. During subsequent clocks, AD[31-0] contains data.
CBE#[3-0]	157, 9, 20, 30	I/O	PCI	**Bus Command and Byte Enable**. During the address phase, CBE#[3-0] define the Bus Command. During the data phase, CBE#[3-0] define the Byte Enables.
FRAME#	10	I/O	PCI	**Cycle Frame** is driven by the current initiator to indicate the beginning and duration of an access.
TRDY#	13	I/O	PCI	**Target Ready** indicates the target's ability to complete the current data phase of the transaction.
IRDY#	11	I/O	PCI	**Initiator Ready** indicates the initiator's ability to complete the current data phase of the transaction.
STOP#	15	I/O	PCI	**Stop** indicates that the M5281 as a target is requesting the master to stop the current transaction.
DEVSEL#	14	I/O	PCI	**Device Select**. This signal indicates that the target device has decoded the address as its own cycle. This signal is an output when the M5281 as a PCI slave has decoded the address as its own cycle.
SERR#/ CLKRUN#	17	OD	PCI	(Select by SW option) **System Error** may be pulsed active by any agent that detects a system error condition. **Clock Run**. This signal is used for Mobile PCI system clock control. The M5281 drives it to request the central resource to start or maintain the interface clock by the assertion of the CLKRUN# signal.

Pin Name	Pin No.	Type	Power Region	Description
PERR#	16	I/O	PCI	**Parity Error**. This signal is the PCI data parity error signal, and may be driven by any device that receives the data and detects a parity error.
PAR	18	I/O	PCI	**Parity signal**. PAR is an Even parity and is calculated on AD[31-0] and CBE#[3-0]. When the M5281 is a PCI master, it drives PAR one PCI clock after the address phase for read/write transactions and one PCI clock after the data phase for write transactions. When the M5281 is a target, it drives PAR one PCI clock after the data phase for PCI master read transactions.
GNT#	146	I	PCI	**Grant**. When this signal is asserted, the M5281 has been granted permission to own the PCI bus.
IDSEL	159	I	PCI	**Initialization Device Select**. It is used as a chip select during configuration read and write transactions.
REQ#	147	O	PCI	**Request** is driven by the M5281 when it requests ownership of the PCI bus.
INTA#	142	OD	PCI	**PCI Interrupt A**.

2.1.2 Parallel ATA, Flash ROM and Serial ROM Interface

Pin Name	Pin No.	Type	Power Region	Description
PROMCS#/EECS	134	O	PATA	**Flash ROM Chip Select**. This signal is connected to Flash ROM chip enable pin. EEPROM Chip Select. This signal is connected to EEPROM chip enable pin.
PROMD[4]	133	I/O	PATA	**Flash ROM Data**. This signal is connected to Flash ROM DATA[4].
PROMD[3]	135	I/O	PATA	**Flash ROM Data**. This signal is connected to Flash ROM DATA[3].
PROMD[2]/EECK	136	I/O	PATA	**Flash ROM Data**. This signal is connected to Flash ROM DATA[2].EEPROM Clock. This signal is clock signal to EEPROM.
PROMD[1]/EEDI	137	I/O	PATA	**Flash ROM Data**. This signal is connected to Flash ROM DATA[1].EEPROM Data Input. This signal is connected to data output pin of EEPROM.
PROMD[0]/EEDO	138	I/O	PATA	**Flash ROM Data**. This signal is connected to Flash ROM DATA[0].EEPROM Data Output. This signal is connected to data input pin of EEPROM.
PIDEA[2:0]	69, 72, 71	O	PATA	**Primary Channel IDE ATA Address Bus**. These are the Address pins connected to Primary Channel.
PIDECS1#	70	O	PATA	**Primary Channel 0 IDE Chip Select 1**. This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3#	68	O	PATA	**Primary Channel 1 IDE Chip Select 3**. This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDED[15:0]	79, 82, 84, 86, 88, 91, 93, 95, 96, 94, 92, 90, 87, 85, 83, 80	I/O	PATA	**Primary IDE ATA Data Bus**. These are the Data pins connected to Primary Channel.
PIDEDAK#	74,	O	PATA	**Primary IDE DACK# for IDE Master**. This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33/66/100/133 mode.
PIDEDRQ	78,	I	PATA	**Primary IDE DMA Request for IDE Master**. This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer. It

Pin Name	Pin No.	Type	Power Region	Description
				will be active high in DMA or Ultra-33/66/100/133 mode and always be inactive low in PIO mode.
PIDEIOR#	76,	O	PATA	**Primary IDE IOR# Command**. This is the IOR# command output pin to notify the Primary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycle, this pin is used by IDE Controller to notify IDE device as DMA Ready (DDMARDY#). In write cycles, IDE Controller will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.
PIDEIOW#	77	O	PATA	**Primary IDE IOW# Command**. This is the IOW# command output pin to notify the Primary IDE device that the available Write Data is already asserted by IDE Controller in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin is driven by IDE Controller to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.
PIDEIRQ	73	I	PATA	**Primary IDE IRQ Input1**.This is a steer-able Interrupt input from Device.
PIDERDY	75	I	PATA	**Primary IDE Ready**. This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE controller to strobe the input data. In write cycle, this pin is used by IDE device to notify IDE Controller as DMA Ready (DDMARDY#).
SIDEA[2]/ PROMD[7] SIDEA[1]/ PROMD[5] SIDEA[0]/ PROMD[6]	102, 105, 104	O	PATA	**Secondary IDE ATA Address Bus**. These are the Address pins connected to Secondary Channel. **Flash ROM Data**. This signal is connected to Flash ROM DATA[7]/DATA[5]/DATA[6].
SIDECS1#/ PROMRE#	103	O	PATA	**Secondary Channel 0 IDE Chip Select 1**. This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command. **Flash ROM Read Enable**. This signal is connected to Flash ROM RE#.
SIDECS3#/ PROMWE#	101	O	PATA	**Secondary Channel 1 IDE Chip Select 3**. This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command. **Flash ROM Write Enable**. This signal is connected to Flash ROM WE#.
SIDED[15:0]/ PROMA[15:0]	113, 116, 118, 121, 123, 126, 128, 130, 131, 129, 127, 124, 122, 119, 117, 114	I/O	PATA	**Secondary IDE ATA Data Bus**. These are the Data pins connected to Secondary Channel. **Flash ROM Address**. This signal is connected to Flash ROM address
SIDEDAK#	107	O	PATA	**Secondary IDE DACK# for IDE Master**. This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33/66/100/133 mode.
SIDEDRQ	112	I	PATA	**Secondary IDE DMA Request for IDE Master**. This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer. It will be active high in DMA or Ultra-33/66/100/133 mode and always be inactive low in PIO mode.
SIDEIOR#	110	O	PATA	**Secondary IDE IOR# Command**. This is the IOR# command output

Pin Name	Pin No.	Type	Power Region	Description
				pin to notify the Secondary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycle, this pin is used by IDE Controller to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Controller will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.
SIDEIOW#	111	O	PATA	**Secondary IDE IOW# Command**. This is the IOW# command output pin to notify the Secondary IDE device that the available Write Data is already asserted by IDE Controller in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin is driven by IDE Controller to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.
SIDEIRQ	106	I	PATA	**Secondary IDE IRQ Input2**. This is a steer-able Interrupt input from device.
SIDERDY	108	I	PATA	**Secondary IDE Ready**. This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE Controller to strobe the input data. In write cycles, this pin is used by IDE device to notify IDE Controller as DMA Ready (DDMARDY#).

2.1.3   Reserved Interface

Pin Name	Pin No.	Type	Power Region	Description
Reserved	47,46	O		Reserved
Reserved	42,43	I		Reserved; pull to low
Reserved	64,63	O		Reserved
Reserved	59,60	I		Reserved; pull to low
Reserved	57	I		AC ground connected with a 10uF external Capacitor.
Reserved	56	I		15K ohm external reference resistor to adjust to Impendence.

2.1.4   DFT Test Pins

Pin Name	Pin No.	Type	Power Region	Description
DFTSE	140	I	PCI	**DFT Scan Enable.** This signal is used as the DFT Scan Enable for ATPG pattern input when DFTTM is tied to high. It should be pulled low for normal operation.
DFTTM	141	I	PCI	**DFT Test Mode.** This signal is used as the DFT Test Mode Enable for ATPG pattern input. It should be pulled low for normal operation.

2.1.5   Other Pins

Pin Name	Pin No.	Type	Power Region	Description
CLKI	98	I	PATA	25 MHz Crystal Pad Input
CLKO	99	O	PATA	25 MHz Crystal Pad Output

2.1.6   Power and Ground

Pin Name	Pin No.	Type	Power Region	Description
VDDO_PCI	5, 33, 151, 139		PCI	3.3 V main power for I/O pad power.
GNDO_PCI	12, 40, 158, 144			Ground for I/O pad.
VDDO_PATA	81, 109		PATA	
GNDO_PATA	89, 115, 125			
VDDCORE	19, 97, 120		CORE	1.8v main power for core
GNDCORE	26, 100, 132			
AVDD0	54			3.3v PHY Analog Power
AVDD1	53			1.8v PHY PLL Power
AVSS1	55			
AVDD2	52			1.8v PHY Analog Power
AVSS2	51			
AVDD3_0, AVDD3_1	49,67			1.8v PHY Transmission Power
AVSS3_0, AVSS3_1	50,66			
AVDD4_0, AVDD4_1	41,61			1.8v PHY Receiver Power
AVSS4	44, 58			
AVDD5_0, AVDD5_1	48,62			3.3v PHY Analog Power
AVSS5_0, AVSS5_1	45,65			

2.2 Hardware Setting

Pin Name	Pin No.	External Pull-R Setting	Function Description
SHCS1#	101	L	128 pin package,
		H	Reserved.
SHCS0#	103	L	Card Bus Disable
		H	Card Bus Enable
SHIOW#	111	L	M5228 Present; M5228 is shown as a PCI device.
		H	M5228 Hidden; M5228 can not be seen as a PCI device.
SHDMACK#	107	L	PATA Disable.
		H	PATA Enable.
{PROMCS#, SHIOR#}	{138,110}	LL	Normal operation (as Card Bus Disable) / PCI driving 4 mA (as Card Bus Enable)
		LH	Daisy Chain position number 1 (as Card Bus Disable) / PCI driving 8 mA (as Card Bus Enable)
		HL	Daisy Chain position number 2 (as Card Bus Disable) / PCI driving 12 mA (as Card Bus Enable)
		HH	Daisy Chain position number 3 (as Card Bus Disable) / PCI driving 16 mA (as Card Bus Enable)

2.3 Integrated PCI Devices Data Reference Table

M5282 is implemented as a PCI multi-function device. Each function and its corresponding function number is as follows:

Function	Function No.	Notes
Serial–ATA	0 (3, 5)	When the Daisy Chain architecture is disabled or the device is at Daisy Chain # 1, the function number. is 0. The function number is 3 when the device is at Daisy Chain # 2. The function number is 5 when the device is at Daisy Chain # 3.
Parallel–ATA	1 (4,6)	When the Daisy Chain architecture is disabled or the device is at Daisy Chain # 1, the function number. is 1. The function number is 4 when the device is at Daisy Chain # 2. The function number is 6 when the device is at Daisy Chain # 3.
Flash ROM	2	In default mode, the Flash ROM controller will be hidden at M5282.

3. Function Description

3.1 PCI

The PCI Interface of M5282 is a 33 MHz, 32-bit Address/Data, Rev 2.2 Compliant solution with the following features:

• Parity protection on all PCI bus signals.
• Fully supports PCI Configuration Space Enable (CSE) protocol.
• Fully compliant with PCI Rev. 2.2.

3.1.1 Target

(TBD)

3.1.2 Master

(TBD)

3.2 Parallel ATA

• 2 PATA channel for up to 4 devices.
• Up to Ultra-DMA mode 6 (ATA-133).
• Up to Multiword DMA mode2.
• Up to PIO mode 4.
• Each channel bus master concurrently. (Each channel could run DMA concurrently.)
• Hot-swap by tri-state IDE signals.

3.3 Flash ROM

• Supports up-to 64K Byte Flash ROM Read/Write.
• AS the HW setting disables the Flash ROM interface, the Flash ROM PCI configuration space 00h -3fh is disabled. But, the other space (after 40h) is still enabled,

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4. Registers

4.1 M5281 PCI Configuration Register

The following table summarizes the registers:

Byte Index	Definition	Attribute (R/W)	Default Value
01h-00h	Vender ID	RO	10B9h
03h-02h	Device ID	RO	5281h
05h-04h	Command	R/W	0000h
07h-06h	Status	RO, R/W Clear	02A0h
08h	Revision ID	RO	A0h
0Bh-09h	Class Code	R/W	018085h
0Ch	Reserved	RO	00h
0Dh	Latency Timer	R/W	00h
0Eh	Header Type	RO	80h
0Fh	Reserved	RO	00h
13h-10h	Base Address Register 1	R/W	000001F1h
17h-14h	Base Address Register 2	R/W	000003F5h
1Bh-18h	Base Address Register 3	R/W	00000171h
1Fh-1Ch	Base Address Register 4	R/W	00000375h
23h-20h	Base Address Register 5	R/W	0000F001h
24h-27h	Reserved	RO	00000000h
2Bh-28h	CardBus Information Structure Pointer	RO	00000000h
2Dh-2Ch	Subsystem Vendor ID	R/W Lock	10B9h
2Fh-2Eh	Subsystem Device ID	R/W Lock	5281h
33h-30h	ROM Base Address (works when M5282's PCI interface is disabled)	RO	00050000h
34h	Capabilities Pointer	R/W Lock	00h
3Bh-35h	Reserved	RO	0s
3Ch	Interrupt Line	R/W	00h
3Dh	Interrupt Pin	RO	01h
3Fh-3Eh	Reserved	RO	0000h
40h	Reserved	RO	00h
41h	Reserved	RO	00h
42h	System Control Register 1	R/W	00h
43h	System Control Register 2	R/W	00h
44h	System Control Register 3	R/W	01h
45h	System Control Register 4	R/W	00h
46h	Reserved	RO	00h
47h	Reserved	RO	00h
48h	Reserved	RO	00h
49h	System Control Register 5, Reserved for ULi only	R/W	00h
4Ah	Reserved	RO	00h
4Bh	Reserved	RO	00h
4Ch	Reserved	R/W	68h
4Dh	Reserved	R/W	00h
4Eh	Reserved	R/W	68h
4Fh	Reserved	R/W	00h
50h	Capability ID	R/W Lock	01h
51h	Next Item Pointer	R/W Lock	00h
53h-52h	Power Management Capabilities	R/W Lock	0002h
55h-54h	Power Management Control/Status Register	R/W Lock	0000h

Byte Index	Definition	Attribute (R/W)	Default Value
56h	PMCSR Bridge Support Extensions	RO	00h
57h	Data Register	R/W Lock	00h
9Fh-5Ch	Reserved	R/W	00h
A7-A0h	Reserved	RO	00h
B9-B0h	Reserved	RW	00h
FFh-BCh	Reserved	R/W	00h

Device: **Reserved Device**
Register Index: **01h-00h**
Register Name: **Vendor ID Register (VID)**
Default Value: 10B9h
Attribute: Read Only

Bit	Description
15-0	This is a 16-bit value assigned to ULi. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Device: **Reserved Device**
Register Index: **03h-02h**
Register Name: **Device ID Register (DID)**
Default Value: 5281h
Attribute: Read Only

Bit	Description
15-0	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device. Write to this register has no effect.

Device: **Reserved Device**
Register Index: **05h-04h**
Register Name: **Command Register (COM)**
Default Value: 0000h
Attribute: Read/Write

Bit	Description
15-11	Reserved. These bits are always 0.
10	Reserved.
9	**Back-to-Back Enable**. M5282 only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8	**Enable the SERRJ driver**. When this bit is set, M5282 will enable SERRJ output driver. This bit is reset to 0 and will be set to 1 when it detects an address parity error. SERRJ is not asserted if this bit is 0.
7	**Wait Cycle Control** - M5282 does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6	**Respond to Parity Errors**. If set to 1, the M5282 block will assert an internal PERRJ when it is the agent receiving data and it detects a data parity error.
5	**Enable VGA Palette Snooping**. This bit is always 0.
4	**Memory Write and Invalidate Command**. M5282 will never issue Memory Write and Invalidate commands. This bit is always 0. Write to this bit has no effect.
3	**Enable Special Cycle**. M5282 will not accept special cycles on PCI. This bit is always 0. Write to this bit has no effect.
2	**Enable PCI Master**. This bit is reset as 0 during Power-On to disable PCI master operations. This bit must be enabled for the normal IDE master operation.
1	**Enable Response to Memory Access**. This bit must be enabled for Flash ROM operation.
0	**Enable Response to I/O Access**. This bit is reset to 0 during Power-On to disable the response to I/O access. This bit must be enabled for normal IDE I/O access.

Device:	**Reserved Device**
Register Index:	**07h-06h**
Register Name:	**Device Status Register (DS)**
Default Value:	0280h
Attribute:	Read Only, Read/Write Clear

Bit	Description
15	**Detected Parity Error**. This bit is set by M5282 to 1 whenever it detects a parity error, even if the Respond to Parity Errors bit (command register, bit 6) is disabled. This bit is cleared (reset to 0) by writing a 1 to it.
14	**SERRJ Status**. This bit is set by M5282 to 1 whenever it detects a PCI address parity error. This bit is cleared (reset to 0) by writing a 1 to it.
13	**Received Master Abort Status**. This bit is set to 1 when M5282, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12	**Received Target Abort Status**. This bit is set to 1 when an M5282 generated PCI cycle (M5282 is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11	**Sent Target Abort Status**. M5282 as a slave never generates a Target abort. This bit is always 0.
10-9	**DEVSELJ Timing**. Read only bits indicating DEVSELJ timing when performing a positive decode. 00: Fast. 01: Medium. 10: Slow. Since DEVSELJ is asserted by M5282 to meet the medium timing, these bits are encoded as 01b.
8	**Data Parity Reported**. Set to 1 if the Respond to Parity Error bit (Command Register bit 6) is set, and M5282 detects internal PERRJ asserted while acting as PCI master (whether internal PERRJ was driven by M5282 or not).
7	**Fast Back-to-Back Capable**. M5282 does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
7-5	**Reserved**. These bits are always 0.
4	**Capabilities**. M5282 supports a pointer for an extended capabilities linked list at SATA_34_D[7:0]. 0: Disable capabilities linked list function (default) 1: Enable capabilities linked list function ** This bit will be Read only when SATA_42_D[0] = '0' (default)
3	**Interrupt Status**. This read-only bit indicates the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's **INTx#** signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2-0	**Reserved**. These bits are always 0.

Device:	**Reserved Device**
Register Index:	**08h**
Register Name:	**Revision ID Register (RID)**
Default Value:	A0h
Attribute:	Read Only

Bit	Description
7-0	This register contains the version number of the M5282. ** This bit can be R/W when SATA_43_D[7] = '1' (default ='0').

Device:	**Reserved Device**
Register Index	**0Bh-09h**
Register Name:	**Class Code Register (CC)**
Default Value	018085h
Attribute:	Read/Write

Bit	Description
23-8	**Class Code**. Value 0180h is the Base Class and Sub-Class Code of M5282 (other storage controller).
7-0	Bits [7:0] identify the Interface of M5282. Meaning of each bit is as follows:
7	**Master or Slave IDE Device**. 0: Slave. 1: Master. The M5282 is a Master IDE Device. This bit is always 1.
6-4	**Reserved**.
3	**Secondary Channel Operation Mode Support**. This bit indicates whether or not the Secondary Channel has a Fix Mode of Operation. 0: Operation mode is fixed and is determined by the value of bit 2. 1: Channel supports both modes and may be set to either mode by writing bit 2. The M5282 supports both modes defined in bit 2. This bit is always 1.
2	**Secondary Channel Operation Mode**. 0: Compatible Mode. 1: Native Mode.
1	**Primary Channel Operation Mode Support** This bit indicates whether or not the Primary Channel has a Fix Mode of Operation. 0: Operation mode is fixed and is determined by the value of bit 0. 1: Channel supports both modes and may be set to either mode by writing bit 0. The M5282 supports both modes defined in bit 0. This bit is always 1.
0	**Primary Channel Operation Mode**. 0: Compatible Mode. 1: Native Mode.

Device:	**Reserved Device**
Register Index:	**0Ch**
Register Name:	**Reserved Register**
Default Value	00h
Attribute:	Read Only

Device:	**Reserved Device**
Register Index:	**0Dh**
Register Name:	**LT - Latency Timer**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7-0	This register identifies the value of latency timer in PCI clocks for PCI bus master cycles.

Device:	**Reserved Device**
Register Index:	**0Eh**
Register Name:	**Header Type Register (HT)**
Default Value	80h
Attribute:	Read Only

Bit	Description
7-0	This register identifies the type of predefined header in the configuration space. Since M5282 is a multi-function device and not a PCI-to-PCI bridge, this byte should be read as 80h.

Device:	**Reserved Device**
Register Index:	**0Fh**
Register Name:	**Reserved Register**
Default Value:	00h
Attribute:	Read Only

Device:	**Reserved Device**
Register Index:	**13h-10h**
Register Name:	**Base Address Register 1 (BA1)**
Default Value:	000001F1h
Attribute:	Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device:	**Reserved Device**
Register Index:	**17h-14h**
Register Name:	**Base Address Register 2 (BA2)**
Default Value:	000003F5h
Attribute:	Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 0. Indicates that the operational registers are mapped into memory space.

Device:	**Reserved Device**
Register Index:	**1Bh-18h**
Register Name:	**Base Address Register 3 (BA3)**
Default Value:	00000171h
Attribute:	Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device: **Reserved Device**
Register Index: **1Fh-1Ch**
Register Name: **Base Address Register 4 (BA4)**
Default Value: 00000375h
Attribute: Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device: **Reserved Device**
Register Index: **23h-20h**
Register Name: **Base Address Register 5 (BA5)**
Default Value: 0000F001h
Attribute: Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device: **Reserved Device**
Register Index: **2Bh-24h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **Reserved Device**
Register Index: **2Dh-2Ch**
Register Name: **Subsystem Vendor ID (SVID)**
Default Value: 5228h
Attribute: Read/Write Lock

Bit	Description
15-0	If M5281 Register index43_D7 = 0, this register is Readable/Writeable, otherwise this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5281 Register index43_D7 = 1.

Device: **Reserved Device**
Register Index: **2Fh-2Eh**
Register Name: **Subsystem Device ID (SDID)**
Default Value: 5228h
Attribute: Read/Write Lock

Bit	Description
15-0	If M5281 Register index43_D7 = 0, this register is Readable/Writeable, otherwise this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5281 Register index43_D7 = 1.

Device: **Reserved Device**
Register Index: **33h-30h**
Register Name: **Reserved Register**
Default Value: 00000000h
Attribute: Read Only

Device: **Reserved Device**
Register Index: **34h**
Register Name: **Capabilities Pointer (CAPPTR)**
Default Value: 00h
Attribute: Read/Write Lock

Bit	Description
7-0	The Capabilities Pointer point to the M5281 configuration space for the location of the first item in the Capabilities linked list. The Capabilities Pointer offset is DWORD aligned. If the Capability bit is enabled (index 06h bit 4), the default value will be 60h.

Device: **Reserved Device**
Register Index: **3Bh-35h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **Reserved Device**
Register Index: **3Ch**
Register Name: **Interrupt Line Register (IL)**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7-0	This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct effect on M5282.

Device: **Reserved Device**
Register Index: **3Dh**
Register Name: **Interrupt Pin Register (IP)**
Default Value: 01h
Attribute: Read Only

Bit	Description
7-0	This register identifies which interrupt pin a device uses. Since M5281 uses INTA#, this value is set to 01h.

Device: **Reserved Device**
Register Index: **3Eh-3Fh**
Register Name: **Reserved Register**
Default Value: 0000h
Attribute: Read Only

Device:	**Reserved Device**
Register Index:	**40h**
Register Name:	**Reserved Register for ULi Software**
Default Value:	00h
Attribute:	Read/Write

Device:	**Reserved Device**
Register Index:	**41h**
Register Name:	**Reserved Register for PHY Control pins**
Default Value:	00h
Attribute:	Read/Write

Device:	**Reserved Device**
Register Index:	**42h**
Register Name:	**System Control Register**
Default Value:	08h
Attribute:	Read/Write

Bit	Description
7	Reserved.
6	**Flash ROM device ID present / absent** 0: Absent (default, use SATA ROM_ADDR to control Flash ROM) 1: Present (show device M5282)
5	**PCI Transmits Mem Read /Mem Read Multiple** 0: Mem Read (default) 1: Mem Read Multiple
4	**Reserved**
3	**Mask address boundary option** 0: Memory Write cycle has 64 byte boundary 1: Memory Write cycle does not have 64 byte boundary (default)
2	**CardBus support.** 0: None (default). 1: Done.
1	**This option is reserved for ULi only in M5281.**
0	**Control of PCI Power Management Register Block of M5281** (index50_D[31:0] – index54_D[31:0]) 0: Read Only (default). 1: Read/Write.

Device: **Reserved Device**
Register Index: **43h**
Register Name: **System Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7	**Revision ID (index 08h) and Subsystem ID (index 2Fh-2Ch) R/W-lock option** (default 0). 0: Read only 1: R/W
6-4	**Reserved**.
3-0	**Index 09h R/W mask**. 0: Read/Write 1: Read Only

Device: **Reserved Device**
Register Index: **44h**
Register Name: **System Control Register**
Default Value: 01h
Attribute: Read/Write

Bit	Description
7-5	**Test pin select** (reserved for ULi only)
4	**M5281 Sub Class Code (Index 0Ah)** 0: depend on the setting of index44h[2]. 1: 01h.
3	**Software Test Mode Enable.** 0: Disable (normal mode). 1: Enable (test mode).
2	**M5281 Sub Class Code (index0Ah)** 0: 80h. 1: 06h
1	**Reserved**
0	**Simplex bit option for IDE bus master** 0: Read/write 1: Read only (default)

Device: **Reserved Device**
Register Index: **45h**
Register Name: **Reserved.**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7-0	Reserved

Device:	**Reserved Device**
Register Index:	**46h**
Register Name:	**Reserved Register for ULi Software**
Default Value:	00h
Attribute:	Read/Write

Device:	**Reserved Device**
Register Index:	**47h**
Register Name:	**Reserved Register for ULi Software**
Default Value:	00h
Attribute:	Read/Write

Device:	**Reserved Device**
Register Index:	**48h**
Register Name:	**Reserved Register for ULi Software**
Default Value:	00h
Attribute:	Read Only

Device:	**Reserved Device**
Register Index:	**49h**
Register Name:	**System Control Register**
Default Value:	00h
Attribute:	Read/Write but reserved for ULi only

Device:	**Reserved Device**
Register Index:	**4Ah**
Register Name:	**Reserved Register for PHY Control pins**
Default Value:	00h
Attribute:	Read/Write

Device:	**Reserved Device**
Register Index:	**4Bh**
Register Name:	**Reserved Register for PHY Control pins**
Default Value:	00h
Attribute:	Read/Write

Device:	**Reserved Device**
Register Index:	**4Ch**
Register Name:	**Reserved.**
Default Value:	68h
Attribute:	Read/Write

Bit	Description
7:0	**Reserved.**

Device: **Reserved Device**
Register Index: **4Dh**
Register Name: **Reserved**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7-0	**Reserved**.

Device: **Reserved Device**
Register Index: **4Eh**
Register Name: **Reserved**
Default Value: 68h
Attribute: Read/Write

Bit	Description
7-0	**Reserved**

Device: **Reserved Device**
Register Index: **4Fh**
Register Name: **Reserved**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7-0	Reserved.

Device: **Reserved Device**
Register Index: **50h**
Register Name: **Capability ID (CAPID)**
Default Value: 01h
Attribute: Read/Write Lock

Bit	Description
7-0	This read-only register value "01" identifies the linked list item as being the PCI power management registers. This register is write-able when index42_D0 = '1'.

Device: **Reserved Device**
Register Index: **51h**
Register Name: **Next Item Pointer (NIP)**
Default Value: 00h
Attribute: Read/Write Lock

Bit	Description
7-0	This read-only register value "00" indicates that there are no additional items in the capabilities list. This register is write-able when index42_D0 = '1'.

Device:	**Reserved Device**
Register Index:	**53h-52h**
Register Name:	**Power Management Capabilities (PMC)**
Default Value:	0002h
Attribute:	Read/Write Lock

Bit	Description
15-11	**PME Support**. This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. The field value "00000" indicates that M5282 is not capable of asserting the PME#. This register is write-able when index42_D0 = '1'
10	**D2 Support**. The read-only bit value "0" indicates that M5282 does not support the D2 power management state. This register is write-able when index42_D0 = '1'
9	**D1 Support**. The read-only bit value "0" indicates that M5282 does not support the D1 power management state. This register is write-able whenindex42_D0 = '1'
8-6	**Reserved** (must be 0s).
5	**DSI**. The value '0' indicates that the special initialization is not required for the M5282. This register is write-able when index42_D0 = '1'.
4	**Reserved** (must be 0).
3	**PME Clock**. The value '0' indicates that no PCI clock is required for PME# operation for the M5282. This register is write-able when index42_D0 = '1'.
2-0	**Version**. A value of 010b indicates that M5282 complies with Revision 1.1 of the PCI Power Management Interface Specification. This register is write-able when index42_D0= '1'.

Device:	**Reserved Device**
Register Index:	**55h-54h**
Register Name:	**Power Management Control/Status Register (PMCSR)**
Default Value:	0000h
Attribute:	Read/Write Lock

Bit	Description
15	**PME Status**. This bit is set when M5282 is to assert the PME# signal independent of the state of the PME Enable bit.
14-13	**Data Scale**. This 2-bit read only field indicates the scaling factor to be used when interpreting the value of the Data register. This register is write-able when index42_D0 = '1'.
12-9	**Data Select**. This 4-bit is used to select which data is to be reported through the Data register and Data Scale field.
8	**PME Enable**. A "1" enables M5282 to assert PME#. When set to "0", PME# assertion is disabled. This bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.
7-2	**Reserved** (must be 0s).
1-0	**Power State**. This 2-bit field is used both to determine the current power state of M5282 and to set the M5282 into a new power state. The definition of the field values is given below. 00b – D0 01b – D1 (Not implemented) 10b – D2 (Not implemented) 11b – D3hot

Device: **Reserved Device**
Register Index: **56h**
Register Name: **PMCSR Bridge Support Extensions (PMCSR_BSE)**
Default Value: 00h
Attribute: Read Only

Device: **Reserved Device**
Register Index: **57h**
Register Name: **Data Register (DATAR)**
Default Value: 00h
Attribute: Read/Write Lock

Bit	Description
7-0	This register is used to report the state dependent data requested by Data Select field. The value of this register is scaled by the value reported by the Data Scale.

Device: **Reserved Device**
Register Index: **9Fh-5Ch**
Register Name: **Reserved**
Default Value: xxh
Attribute: Read/Write

Device: **Reserved Device**
Register Index: **A7h-A0h**
Register Name: **Reserved**
Default Value: 00h
Attribute: Read Only

Device: **Reserved Device**
Register Index: **B9h-B0h**
Register Name: **Reserved**
Default Value: 00h
Attribute: Read/Write

Device: **Reserved Device**
Register Index: **FFh-BCh**
Register Name: **Reserved**
Default Value: 00h
Attribute: Read/Write

4.2   M5228 (Parallel-ATA) PCI Configuration Register

The following table summarizes the registers:

Byte Index	Definition	Attribute (R/W)	Default Value
01h-00h	Vender ID	RO	10B9h
03h-02h	Device ID	RO	5228h
05h-04h	Command	R/W	0000h
07h-06h	Status	RO, R/W Clear	0280h
08h	Revision ID	RO	C5h
0Bh-09h	Class Code	R/W	018085h
0Ch	Reserved	RO	00h
0Dh	Latency Timer	R/W	00h
0Eh	Header Type	RO	80h
0Fh	Reserved	RO	00h
13h-10h	Base Address Register 1	R/W	000001E9h
17h-14h	Base Address Register 2	R/W	000003EDh
1Bh-18h	Base Address Register 3	R/W	00000169h
1Fh-1Ch	Base Address Register 4	R/W	0000036Dh
23h-20h	Base Address Register 5	R/W	0000E001h
24h-27h	Reserved	RO	00000000h
2Bh-28h	CardBus Information Structure Pointer	RO	000000A0h
2Dh-2Ch	Subsystem Vendor ID	R/W Lock	10B9h
2Fh-2Eh	Subsystem Device ID	R/W Lock	5228h
33h-30h	Reserved	RO	00000000h
34h	Capabilities Pointer	R/W Lock	00h
3Bh-35h	Reserved	RO	0s
3Ch	Interrupt Line	R/W	00h
3Dh	Interrupt Pin	RO	01h
3Fh-3Eh	Reserved	RO	0000h
40h	Channel status	RW	00h
42h-41h	Reserved	RO	00h
43h	Class Code Attribute 1	R/W	7Ah
49h-44h	Reserved	RO	0s
4Bh-4Ah	Control Option 1	R/W	C164h
4Dh-4Ch	Reserved	RO	0000h
4Fh-4Eh	Reserved	RO	1ABAh
50h	Control Option 2	R/W	00h
51h	Reset And Testing	R/W	00h
52h	Reserved	RO	00h
53h	Control Option 3	R/W	01h
54h	FIFO Threshold of Primary Channel	R/W	55h
55h	FIFO Threshold of Secondary Channel	R/W	55h
56h	Ultra DMA Setting for Primary Channel	R/W	44h
57h	Ultra DMA Setting for Secondary Channel	R/W	44h
58h	Primary Channel Address Setup Timing	R/W	00h
59h	Primary Channel Command Block Timing	R/W	00h
5Ah	Primary Channel Drive 0 Data Read/Write Timing	R/W	00h
5Bh	Primary Channel Drive 1 Data Read/Write Timing	R/W	00h
5Ch	Secondary Channel Address Setup Timing	R/W	00h
5Dh	Secondary Channel Command Block Timing	R/W	00h
5Eh	Secondary Channel Drive 0 Data Read/Write Timing	R/W	00h
5Fh	Secondary Channel Drive 1 Data Read/Write Timing	R/W	00h

Byte Index	Definition	Attribute (R/W)	Default Value
60h	Capability ID	R/W Lock	01h
61h	Next Item Pointer	R/W Lock	00h
63h-62h	Power Management Capabilities	R/W Lock	0002h
65h-64h	Power Management Control/Status Register	R/W Lock	0000h
66h	PMCSR Bridge Support Extensions	RO	00h
67h	Data Register	R/W Lock	00h
A7-A0h	CardBus Information Structure Data	RO	00h
FFh-68h	Reserved	RO	0s

Device: **IDE Host Controller**
Register Index: **01h-00h**
Register Name: **Vendor ID Register (VID)**
Default Value: 10B9h
Attribute: Read Only

Bit	Description
15-0	This is a 16-bit value assigned to ULi. This register, combined with 03h-02h, uniquely identifies any PCI device. Write to this register has no effect.

Device: **IDE Host Controller**
Register Index: **03h-02h**
Register Name: **Device ID Register (DID)**
Default Value: 5228h
Attribute: Read Only

Bit	Description
15-0	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device. Write to this register has no effect.

Device: **IDE Host Controller**
Register Index: **05h-04h**
Register Name: **Command Register (COM)**
Default Value: 0000h
Attribute: Read/Write

Bit	Description
15-11	Reserved. These bits are always 0.
10	Reserved.
9	**Back-to-Back Enable**. M5228 only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8	**Enable the SERRJ driver**. When this bit is set, M5228 will enable SERRJ output driver. This bit is reset to 0 and will set to 1 when it detects an address parity error. SERRJ is not asserted if this bit is 0.
7	**Wait Cycle Control**. M5228 does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6	**Respond to Parity Errors**. If set to 1, the M5228 block will assert an internal PERRJ when it is the agent receiving data and it detects a data parity error.
5	**Enable VGA Palette Snooping**. This bit is always 0.
4	**Memory Write and Invalidate Command**. M5228 will never issue Memory Write and Invalidate commands. This bit is always 0. Write to this bit has no effect.
3	**Enable Special Cycle**. M5228 will not accept special cycles on PCI. This bit is always 0. Write to this bit has no effect.
2	**Enable PCI Master**. This bit is reset as 0 during Power-On to disable PCI master operations. This bit must be enabled for the normal IDE master operation.
1	**Enable Response to Memory Access**. M5228 will never respond to Memory access. This bit is always 0. Write to this bit has no effect.
0	**Enable Response to I/O Access**. This bit is reset as 0 during Power-On to disable the response to I/O access. This bit must be enabled for normal IDE I/O access.

Device: **IDE Host Controller**
Register Index: **07h-06h**
Register Name: **Device Status Register (DS)**
Default Value: 0280h
Attribute: Read Only, Read/Write Clear

Bit	Description
15	**Parity Error Detected**. This bit is set by M5228 to 1 whenever it detects a parity error, even if the Respond to Parity Errors bit (command register, bit 6) is disabled. This bit is cleared (reset to 0) by writing a 1 to it.
14	**SERRJ Status**. This bit is set by M5228 to 1 whenever it detects a PCI address parity error. This bit is cleared (reset to 0) by writing a 1 to it.
13	**Master Abort Status Received**. This bit is set to 1 when M5228, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12	**Target Abort Status Received**. This bit is set to 1 when an M5228 generated PCI cycle (M5228 is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11	**Target Abort Status Sent**. M5228 as a slave never generates a Target abort. This bit is always 0.
10-9	**DEVSELJ Timing**. Read only bits indicating DEVSELJ timing when performing a positive decode. 00: Fast. 01: Medium. 10: Slow. Since DEVSELJ is asserted by M5228 to meet the medium timing, these bits are encoded as 01b.
8	**Data Parity Reported**. Set to 1 if the Respond to Parity Error bit (Command Register bit 6) is set, and M5228 detects internal PERRJ asserted while acting as PCI master (whether internal PERRJ was driven by M5228 or not).
7	**Fast Back-to-Back Capable**. M5228 supports fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
7-5	**Reserved**. These bits are always 0.
4	**Capabilities**. M5228 supports a pointer for an extended capabilities linked list at IDE_34_D[7:0]. 0: Disable capabilities linked list function (default) 1: Enable capabilities linked list function ** This bit will be Read only when IDE_4A_D[10] = '0' (default)
3	**This read-only bit reflects the state of the interrupt in the device**. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's **INTx#** signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2-0	**Reserved**. These bits are always 0.

Device: **IDE Host Controller**
Register Index: **08h**
Register Name: **Revision ID Register (RID)**
Default Value: C5h
Attribute: Read Only

Bit	Description
7-0	This register contains the version number of the M5228. ** This bit can be R/W when IDE_43_D[7] = '1' (default = '0').

Device: **IDE Host Controller**
Register Index   **0Bh-09h**
Register Name: **Class Code Register (CC)**
Default Value   01018Ah
Attribute: Read/Write

Bit	Description
23-8	**Base Class and Sub-Class Code of M5228**. Value 0101h means IDE Controller.
7-0	Bits [7:0] identify the Interface of M5228. Definition of each bit is as follows:
7	**Master or Slave IDE Device**. 0: Slave. 1: Master. The M5228 is a Master IDE Device. This bit is always 1.
6	**Enable support of IDE Channel Status report** 0: Disable. Default value for PCI Specification 2.1 and later. 1: Enable. The old SCT test program will define this bit along with bits 4 and 5 be 0h and read-only to comply with PCI Specification 2.1. But based on Microsoft's proposal, bit 4 and bit 5 are used by OS to disable/enable IDE Channel. For the old SCT issue, M5228 Register Index 43h, Index 4Dh bit 7 or Index 50h bit 1 can be used to change the attribute and value for bits [6:4]. **To meet PCI 2.2 specification, this bit will be seen as '0', regardless its real value.**
5	**Enable/Disable IDE Primary Channel**. 0: Disable. 1: Enable. This bit is used to disable or enable IDE Primary Channel no matter what value bit 6 is. This bit must be set to 1 to enable IDE Primary Channel. **To meet PCI 2.2 specification, this bit will be seen as '0', regardless its real value.**
4	**Enable/Disable IDE Secondary Channel**. 0: Disable. 1: Enable. This bit is used to disable or enable IDE Secondary Channel no matter what value bit 6 is. This bit must be set to 1 to enable IDE Secondary Channel. **To meet PCI 2.2 specification, this bit will be seen as '0', regardless its real value.**
3	**Secondary Channel Operation Mode Support**. This bit indicates whether or not the Secondary Channel has a Fix Mode of Operation. 0: Operation mode is fixed and is determined by the value of bit 2. 1: Channel supports both modes and may be set to either mode by writing bit 2. The M5228 supports both modes defined in bit 2. This bit is always 1.
2	**Secondary Channel Operation Mode**. 0: Compatible Mode. 1: Native Mode.
1	**Primary Channel Operation Mode Support** This bit indicates whether or not the Primary Channel has a Fix Mode of Operation. 0: Operation mode is fixed and is determined by the value of bit 0. 1: Channel supports both modes and may be set to either mode by writing bit 0. The M5228 supports both modes defined in bit 0. This bit is always 1.
0	**Primary Channel Operation Mode**. 0: Compatible Mode. 1: Native Mode.

Device: **IDE Host Controller**
Register Index: **0Ch**
Register Name: **Reserved Register**
Default Value   00h
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **0Dh**
Register Name: **LT - Latency Timer**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7-0	This register identifies the value of latency timer in PCI clocks for PCI bus master cycles.

Device: **IDE Host Controller**
Register Index: **0Eh**
Register Name: **Header Type Register (HT)**
Default Value   80h
Attribute: Read Only

Bit	Description
7-0	This register identifies the type of predefined header in the configuration space. Since M5228 is a multi-function device and not a PCI-to-PCI bridge, this byte should be read as 80h.

Device: **IDE Host Controller**
Register Index: **0Fh**
Register Name: **Reserved Register**
Default Value: 00h
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **13h-10h**
Register Name: **Base Address Register 1 (BA1)**
Default Value: 000001E9h
Attribute: Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device: **IDE Host Controller**
Register Index: **17h-14h**
Register Name: **Base Address Register 2 (BA2)**
Default Value: 000003EDh
Attribute: Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 0. Indicates that the operational registers are mapped into memory space.

Device: **IDE Host Controller**
Register Index: **1Bh-18h**
Register Name: **Base Address Register 3 (BA3)**
Default Value: 00000169h
Attribute: Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device: **IDE Host Controller**
Register Index: **1Fh-1Ch**
Register Name: **Base Address Register 4 (BA4)**
Default Value: 0000036Dh
Attribute: Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device: **IDE Host Controller**
Register Index: **23h-20h**
Register Name: **Base Address Register 5 (BA5)**
Default Value: 0000E001h
Attribute: Read/Write

Bit	Description
31-2	Base Address. POST writes the value of the IO base address to this register.
1	Reserved. Always 0.
0	Always 1. Indicates that the operational registers are mapped into I/O space.

Device: **IDE Host Controller**
Register Index: **27h-24h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **2Bh-28h**
Register Name: **Reserved Register**
Default Value: 000000A0h
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **2Dh-2Ch**
Register Name: **Subsystem Vendor ID (SVID)**
Default Value: 5228h
Attribute: Read/Write Lock

Bit	Description
15-0	If M5228 Register IDE_53_D7 = 0, this register is Readable/Writeable, otherwise this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5228 Register IDE_53_D7 = 1.

Device: **IDE Host Controller**
Register Index: **2Fh-2Eh**
Register Name: **Subsystem Device ID (SDID)**
Default Value: 5228h
Attribute: Read/Write Lock

Bit	Description
15-0	If M5228 Register IDE_53_D7 = 0, this register is Readable/Writeable, otherwise, this register is Read-Only. BIOS should program a value to this register and then lock it by setting M5228 Register IDE_53_D7 = 1.

Device: **IDE Host Controller**
Register Index: **33h-30h**
Register Name: **Reserved Register**
Default Value: 00000000h
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **34h**
Register Name: **Capabilities Pointer (CAPPTR)**
Default Value: 00h
Attribute: Read/Write Lock

Bit	Description
7-0	The Capabilities Pointer points to the M5228 configuration space for the location of the first item in the Capabilities linked list. The Capabilities Pointer offset is DWORD aligned. If the Capability bit is enabled (index 06h bit 4), the default value will be 60h.

Device: **IDE Host Controller**
Register Index: **3Bh-35h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device:	**IDE Host Controller**
Register Index:	**3Ch**
Register Name:	**Interrupt Line Register (IL)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7-0	This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct effect on M5228.

Device:	**IDE Host Controller**
Register Index:	**3Dh**
Register Name:	**Interrupt Pin Register (IP)**
Default Value:	01h
Attribute:	Read Only

Bit	Description
7-0	This register identifies which interrupt pin a device uses. Since M5228 uses INTA#, this value is set to 01h.

Device:	**IDE Host Controller**
Register Index:	**3Eh-3Fh**
Register Name:	**Reserved Register**
Default Value:	0000h
Attribute:	Read Only

Device:	**IDE Host Controller**
Register Index:	**40h**
Register Name:	**Channel Status Register**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7	**Secondary Channel enable/disable indicator** 0: Enable (default) 1: Disable
6	**Primary Channel enable/disable indicator** 0: Enable (default) 1: Disable
5	**Reserved**
4	**SubClass Code option** 0: return 80h 1: return 01h
3-0	**Reserved**

Device:	**IDE Host Controller**
Register Index:	**42h-41h**
Register Name:	**Reserved Register**
Default Value:	00h
Attribute:	Read Only

Device: **IDE Host Controller**
Register Index: **43h**
Register Name: **Class Code Attribute Register 1 (CCA1)**
Default Value: 7Ah
Attribute: Read/Write

Bit	Description
7	**Revision ID (index 08h) R/W-lock option** (default 0). 0: Read only 1: R/W
6	**Index 09h bit 6 Attribute**. 0: Read/Write. 1: Read Only. This bit can be used to change the attribute of Index 09h bit 6. When this bit is reset as 0, Index 09h bit 6 can be read/write. If this bit is set to 1, Index 09h bit 6 is read only.
5	**Index 09h bit 5 Attribute**. 0: Read/Write. 1: Read Only. This bit can be used to change the attribute of Index 09h bit 5. When this bit is reset as 0, Index 09h bit 5 can be read/write. If this bit is set to 1, Index 09h bit 5 is read only.
4	**Index 09h bit 4 Attribute**. 0: Read/Write. 1: Read Only. This bit can be used to change the attribute of Index 09h bit 4. When this bit is reset as 0, Index 09h bit 4 can be read/write. If this bit is set to 1, Index 09h bit 4 is read only.
3	**Index 09h bit 3 Attribute**. 0: Read/Write. 1: Read Only. This bit can be used to change the attribute of Index 09h bit 3. When this bit is reset as 0, Index 09h bit 3 can be read/write. If this bit is set to 1, Index 09h bit 3 is read only.
2	**Index 09h bit 2 Attribute**. 0: Read/Write. 1: Read Only. This bit can be used to change the attribute of Index 09h bit 2. When this bit is reset as 0, Index 09h bit 2 can be read/write. If this bit is set to 1, Index 09h bit 2 is read only.
1	**Index 09h bit 1 Attribute**. 0: Read/Write. 1: Read Only. This bit can be used to change the attribute of Index 09h bit 1. When this bit is reset as 0, Index 09h bit 1 can be read/write. If this bit is set to 1, Index 09h bit 1 is read only.
0	**Index 09h bit 0 Attribute**. 0: Read/Write. 1: Read Only. This bit can be used to change the attribute of Index 09h bit 0. When this bit is reset as 0, Index 09h bit 0 can be read/write. If this bit is set to 1, Index 09h bit 0 is read only.

Device: **IDE Host Controller**
Register Index: **48h-44h**
Register Name: **Reserved Registers**
Default Value: 0s
Attribute: Read /Write

Device: **IDE Host Controller**
Register Index: **49h**
Register Name: **Reserved Register**
Default Value: 0s
Attribute: Read Only

Note: This register is for testing only. Do NOT write any value into this register, or the secondary channel will fail.

Register Index: **4Bh-4Ah**
Register Name: **Control Option Register I (CO1)**
Default Value: C164h
Attribute: Read/Write

Bit	Description
15-14	Reserved
13	**Interrupt disable registers enable/disable**. 0: disable index04h[10] = '0' and read only index06h[3] ='0' and read only 1: enable index04h[10] read/write index06[3] = (not INTAJ) of M5228
12	Reserved.
11	**Limit the master burst the PCI cycle to less than 16**. 0: enable (default). 1: disable.
10	**Control of PCI Power Management Register Block of M5228** (IDE_60_D[31:0] – IDE_64_D[31:0]) 0: Read-Only (default). 1: Read/Write.
9	**Read/Write memory within 64-byte boundary**. 0: disable (default) 1: enable
8-7	**Reserved**.
6	**Enable/Disable 48-bit LBA support**. 0: Disable 1: Enable (default)
5	**UDMA READ (above ATA-66) Byte count enable/disable** 0: enable 1: disable (use interrupt to indicate the end of byte count)* (default)
4	**Enable/Disable DMA byte count feature for supporting 48-bit LBA**. 0: Enable (default) 1: Disable
3	**Gated clock feature enable/disable** 0: Disable (default) 1: Enable
2	**Simplex bit option for IDE bus master** 0: Read/write 1: Read only (default)
1	**Channel Bus Master Parking** 0: No parking 1: Parking at the previous one channel which is the bus master.
0	ATA read status command will return value from Shadow register of ATA status register when DMA cycle is running. 0: enable (default) 1: disable

Device: **IDE Host Controller**
Register Index: **4Ch**
Register Name: **Reserved Register**
Default Value: 00h
Attribute: Read only
Notice: Do NOT write any value into this register, or the UDMA termination timing will be changed.

Device: **IDE Host Controller**
Register Index: **4Dh**
Register Name: **Reserved Register**
Default Value: 00h
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **4Fh-4Eh**
Register Name: **Reserved Register**
Default Value: 1ABAh
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **50h**
Register Name: **Control Option Register 2**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7-6	**Reserved**.
5 (0)	**Decoding Methods for the third byte of BA2 and BA4 during Native Mode**. 0: All 4 bytes are master IDE's cycle. 1: Only the 3rd byte is master IDE's cycle. This bit is used to control the internal decoding methods for the third byte of BA2 and BA4 registers during native mode. When this bit is reset to 0, all the four bytes defined by the Base Address Register 2 (M5228 Index 17h-14h) and Base Address Register 4 (M5228 Index 1Fh-1Ch) will be decoded as M5228 cycle and pass on to the ATA bus. If this bit is set to 1, only the third byte will be decoded as M5228 cycle and pass on to the ATA bus.
4	**Reserved**.
3	**Decoding Method for I/O Address 3F6h and 376h**. 0: Decode 3F6h and 376h that only uses address. 1: Use byte enable decoding. This bit is used to control the internal decoding method for I/O ports 3F6h and 376h. When this bit is reset to 0, M5228 will decode only the PCI AD address and ignore the byte enable signals. If this bit is set to 1, M5228 will not ignore the byte enable signals, which means only CBEJ[2] = 0 will decode as IDE 3F6h and 376h cycles.
2	**Reserved**.
1	**Index 09h Bits [6:4] Programming Interface**. 0: Return 000b during read (default). 1: Return the real contents.
0	**Force to enable the IDE IO** (bypass the cfg_04[0] (IO enable)) 0: Disable (default). 1: Enable.

Device: **IDE Host Controller**
Register Index: **51h**
Register Name: **Reset and Testing Register (RAT)**
Default Value: 00h
Attribute: Read/Write
This register is for test purpose only and should not be programmed by BIOS in normal operation.

Bit	Description
7	**Chip Reset**. Writing a '1' to this bit will reset the whole chip as hardware reset. It generates a one-cycle pulse only.
6	**Soft Reset**. Writing a '1' to this bit will reset all blocks except the configuration space. It generates a one-cycle pulse only.
5	**Soft Reset**. Writing a '1' to this bit will reset the ATASTATE (ATA State Machine) and AUTOPOL2 (PIO Mode State Machine). It generates a one-cycle pulse only.
4	**Soft Reset**. Writing a '1' to this bit will reset the ATASTATE (ATA State Machine) and AUTOPOL1 (PIO Mode State Machine). It generates a one-cycle pulse only.
3	**Reserved**.
2(0)	**M5228 Test Mode Enable**. 0: Disable. 1: Enable. Writing a '1' to this bit will enable the M5228 test mode.
1(0)	**Force to reset the secondary channel**. 0: Disable (default). 1: Enable.
0(0)	**Force to reset the primary channel**. 0: Disable (default). 1: Enable.

Device: **IDE Host Controller**
Register Index: **52h**
Register Name: **Reserved Register**
Default Value: 00h
Attribute: Read Only

Device: **IDE Host Controller**
Register Index: **53h**
Register Name: **Control Option Register 3**
Default Value: 01h
Attribute: Read/Write

Bit	Description
7	**Sub System Vendor and Device ID Registers (M5228 Register Index 2Fh-2Ch) Attribute Control**. 0: Read/Write. 1: Read Only. This bit is used to control the attribute of M5228 Register Index 2Fh-2Ch. BIOS can use this bit to lock the content of Subsystem Vendor and Device ID Registers.
6-4	Reserved.
3	Reserved for ULi.
2	Reserved.
1(0)	Reserved.
0(1)	Reserved.

Device: **IDE Host Controller**
Register Index: **54h**
Register Name: **PIO FIFO Control of Primary Channel Drive 0 and Drive 1 (PFCP)**
Default Value: 55h
Default Value: Read/Write

Bit	Description
7-6	**PIO FIFO Enable bit Primary Channel Drive 1**. 00: PIO mode with FIFO off. 01: PIO mode with FIFO on. 10: reserved. 11: reserved.
5-4	**FIFO Threshold Register. Defines when to Start the Transaction of Primary Channel Drive 1**. 00: 32 WORDs. 01: 8 WORDs. 10: 16 WORDs. 11: 24 WORDs.
3-2	**PIO FIFO Enable bit of Primary Channel Drive 0**. 00: PIO mode with FIFO off. 01: PIO mode with FIFO on.
1-0	**FIFO threshold register. Defines when to Start the Transaction of Primary Channel Drive 0**. 00: 32 WORDs. 01: 8 WORDs. 10: 16 WORDs. 11: 24 WORDs.

Device:	**IDE Host Controller**
Register Index:	**55h**
Register Name:	**PIO FIFO Control of Secondary Channel Drive 0 and Drive 1 (PFCS)**
Default Value:	55h
Attribute:	Read/Write

Bit	Description
7-6	**PIO FIFO Enable bit of Secondary Channel Drive 1**. 00: PIO mode with FIFO off. 01: PIO mode with FIFO on. 10: reserved. 11: reserved.
5-4	**FIFO Threshold Register**. Defines When to Start the Transaction of Secondary Channel Drive 1. 00: 32 WORDs. 01: 8 WORDs. 10: 16 WORDs. 11: 24 WORDs.
3-2	**PIO FIFO Enable bit of Secondary Channel Drive 0**. 00: PIO mode and FIFO off. 01: PIO mode.
1-0	**FIFO threshold register**. Defines when to Start the Transaction of Secondary Channel Drive 0. 00: 32 WORDs. 01: 8 WORDs. 10: 16 WORDs. 11: 24 WORDs.

Device: **IDE Host Controller**
Register Index: **56h**
Register Name: **Ultra DMA Timing Setting for Primary Channel Drive 0 and Drive 1 (UDMAP)**
Default Value: 44h
Attribute: Read/Write

Bit	Description
7	**Enable Primary Channel Device 1 for Ultra DMA**. 0: Disable. 1: Enable. This bit is used to enable the Ultra DMA mode for Primary Channel Device 1.
6-4	**Ultra DMA mode for Primary Channel Device 1**. These three bits are used to program the cycle time for Primary Channel Device 1 when Ultra DMA mode is set by bit 7. These three bits have no effect when bit 7 is set to 0. 000: mode 4 (ATA-66) 001: mode 3 010: mode 2 (ATA-33) 011: mode 1 100: mode 0 101: mode 6 (ATA-133) 110: reserved 111: mode 5 (ATA-100)
3	**Enable Primary Channel Device 0 for Ultra DMA**. 0: Disable. 1: Enable. This bit is used to enable the Ultra DMA mode for Primary Channel Device 0.
2-0	**Ultra DMA mode for Primary Channel Device 0**. These three bits are used to program the cycle time for Primary Channel Device 0 when Ultra DMA mode is set by bit 3. These three bits have no effect when bit 3 is reset as 0. 000: mode 4 (ATA-66) 001: mode 3 010: mode 2 (ATA-33) 011: mode 1 100: mode 0 101: mode 6 (ATA-133) 110: reserved 111: mode 5 (ATA-100)

Device:	**IDE Host Controller**
Register Index:	**57h**
Register Name:	**Ultra DMA Timing Setting for Secondary Channel Drive 0 and Drive 1 (UDMAS)**
Default Value:	44h
Attribute:	Read/Write

Bit	Description
7	**Enable Secondary Channel Device 1 for Ultra DMA**. 0: Disable. 1: Enable. This bit is used to enable the Ultra DMA mode for Secondary Channel Device 1.
6-4	**Ultra DMA mode for Secondary Channel Device 1**. These three bits are used to program the cycle time for Secondary Channel Device 1 when Ultra DMA mode is set by bit 7. These three bits have no effect when bit 7 is set as 0. 000: mode 4 (ATA-66) 001: mode 3 010: mode 2 (ATA-33) 011: mode 1 100: mode 0 101: mode 6 (ATA-133) 110: reserved 111: mode 5 (ATA-100)
3	**Enable Secondary Channel Device 0 for Ultra DMA**. 0: Disable. 1: Enable. This bit is used to enable the Ultra DMA mode for Secondary Channel Device 0. When this bit is set to 1, the operation level defined in Index 55h bits [3:2] will be ignored by M5228, and will support Ultra DMA mode for Secondary Channel Device 0.
2-0	**Ultra DMA mode for Secondary Channel Device 0**. These three bits are used to program the cycle time for Secondary Channel Device 0 when Ultra DMA mode is set by bit 3. These three bits have no effect when bit 3 is set as 0. 000: mode 4 (ATA-66) 001: mode 3 010: mode 2 (ATA-33) 011: mode 1 100: mode 0 101: mode 6 (ATA-133) 110: reserved 111: mode 5 (ATA-100)

Device:	**IDE Host Controller**
Register Index:	**58h**
Register Name:	**Primary Channel Address Setup Timing Register (PCAS)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7-3	Reserved.
2-0 (000)	**Address Setup Timing Count for Primary Channel**. These three bits are used to program the address setup time count for Primary Channel. Clock defined by PCI clock cycle time. The setting value will take effect for command and data access. (1 clk = 30 ns) 000: 8 clks. 001: 1 clk. 010: 2 clks. 011: 3 clks. 100: 4 clks. 101: 5 clks. 110: 6 clks. 111: 7 clks.

Device:	**IDE Host Controller**
Register Index:	**59h**
Register Name:	**Primary Channel Command Block Timing Register (PCCB)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7	Reserved.
6-4 (000)	**Command Active Count**. These three bits are used to program the command block active timing count for Primary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only. (1 clk = 30 ns) 000: 8 clks. 001: 1 clk. 010: 2 clks. 011: 3 clks. 100: 4 clks. 101: 5 clks. 110: 6 clks. 111: 7 clks.
3-0(0000)	**Command Recovery Count**. These four bits are used to program the command block recovery timing count for Primary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only. (1 clk = 30 ns) 0000: 16 clks. 0001: 1 clk. 0010: 2 clks. 0011: 3 clks. 0100: 4 clks. 0101: 5 clks. 0110: 6 clks. 0111: 7 clks. 1000: 8 clks. 1001: 9 clks. 1010: 10 clks. 1011: 11 clks. 1100: 12 clks. 1101: 13 clks. 1110: 14 clks. 1111: 15 clks.

Device:	**IDE Host Controller**
Register Index:	**5Ah**
Register Name:	**Primary Channel Drive 0 Data Read/Write Timing Register (PCDT0)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7	Reserved.
6-4 (000)	**Data Read/Write Active Count**. These three bits are used to program the data read/write active timing count for Primary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 0 data access only. (1 clk = 30 ns) 000: 8 clks.　　001: 1 clk.　　010: 2 clks.　　011: 3 clks. 100: 4 clks.　　101: 5 clks.　　110: 6 clks.　　111: 7 clks.
3-0 (0000)	**Data Read/Write Recovery Count**. These four bits are used to program the data read/write recovery timing count for Primary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 0 data access only. (1 clk = 30 ns) 0000: 16 clks.　　0001: 1 clk.　　0010: 2 clks.　　0011: 3 clks. 0100: 4 clks.　　0101: 5 clks.　　0110: 6 clks.　　0111: 7 clks. 1000: 8 clks.　　1001: 9 clks.　　1010: 10 clks.　　1011: 11 clks. 1100: 12 clks.　　1101: 13 clks.　　1110: 14 clks.　　1111: 15 clks.

Device:	**IDE Host Controller**
Register Index:	**5Bh**
Register Name:	**Primary Channel Drive 1 Data Read/Write Timing Register (PCDT1)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7	Reserved.
6-4 (000)	**Data Read/Write Active Count**. These three bits are used to program the data read/write active timing count for Primary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 1 data access only. (1 clk = 30 ns) 000: 8 clks.　　001: 1 clk.　　010: 2 clks.　　011: 3 clks. 100: 4 clks.　　101: 5 clks.　　110: 6 clks.　　111: 7 clks.
3-0 (0000)	**Data Read/Write Recovery Count**. These four bits are used to program the data read/write recovery timing count for Primary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Primary Channel Drive 1 data access only. (1 clk = 30 ns) 0000: 16 clks.　　0001: 1 clk.　　0010: 2 clks.　　0011: 3 clks. 0100: 4 clks.　　0101: 5 clks.　　0110: 6 clks.　　0111: 7 clks. 1000: 8 clks.　　1001: 9 clks.　　1010: 10 clks.　　1011: 11 clks. 1100: 12 clks.　　1101: 13 clks.　　1110: 14 clks.　　1111: 15 clks.

Device:	**IDE Host Controller**
Register Index:	**5Ch**
Register Name:	**Secondary Channel Address Setup Timing Register (SCAS)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7-3	Reserved.
2-0 (000)	**Address Setup Timing Count for Secondary Channel**. These three bits are used to program the address setup time count for Secondary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command and data access. (1 clk = 30 ns) 000: 8 clks.　　001: 1 clk.　　010: 2 clks.　　011: 3 clks. 100: 4 clks.　　101: 5 clks.　　110: 6 clks.　　111: 7 clks.

Device:	**IDE Host Controller**
Register Index:	**5Dh**
Register Name:	**Secondary Channel Command Block Timing Register (SCCB)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7	Reserved.
6-4 (000)	**Command Active Count**. These three bits are used to program the command block active timing count for Secondary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only. (1 clk = 30 ns) 000: 8 clks.　　001: 1 clk.　　010: 2 clks.　　011: 3 clks. 100: 4 clks.　　101: 5 clks.　　110: 6 clks.　　111: 7 clks.
3-0 (0000)	**Command Recovery Count**. These four bits are used to program the command block recovery timing count for Secondary Channel. Clock is defined by PCI clock cycle time. The setting value will take effect for command block access only. (1 clk = 30 ns) 0000: 16 clks.　　0001: 1 clk.　　0010: 2 clks.　　0011: 3 clks. 0100: 4 clks.　　0101: 5 clks.　　0110: 6 clks.　　0111: 7 clks. 1000: 8 clks.　　1001: 9 clks.　　1010: 10 clks.　　1011: 11 clks. 1100: 12 clks.　　1101: 13 clks.　　1110: 14 clks.　　1111: 15 clks.

Device: **IDE Host Controller**
Register Index: **5Eh**
Register Name: **Secondary Channel Drive 0 Data Read/Write Timing Register (SCDT0)**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7	Reserved.
6-4 (000)	**Data Read/Write Active Count**. These three bits are used to program the data read/write active timing count for Secondary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 0 data access only. (1 clk = 30 ns) 000: 8 clks. 001: 1 clk. 010: 2 clks. 011: 3 clks. 100: 4 clks. 101: 5 clks. 110: 6 clks. 111: 7 clks.
3-0 (0000)	**Data Read/Write Recovery Count**. These four bits are used to program the data read/write recovery timing count for Secondary Channel Drive 0. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 0 data access only. (1 clk = 30 ns) 0000: 16 clks. 0001: 1 clk. 0010: 2 clks. 0011: 3 clks. 0100: 4 clks. 0101: 5 clks. 0110: 6 clks. 0111: 7 clks. 1000: 8 clks. 1001: 9 clks. 1010: 10 clks. 1011: 11 clks. 1100: 12 clks. 1101: 13 clks. 1110: 14 clks. 1111: 15 clks.

Device: **IDE Host Controller**
Register Index: **5Fh**
Register Name: **Secondary Channel Drive 1 Data Read/Write Timing Register (SCDT1)**
Default Value: 00h
Attribute: Read/Write

Bit	Description
7	Reserved.
6-4 (000)	**Data Read/Write Active Count**. These three bits are used to program the data read/write active timing count for Secondary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 1 data access only. (1 clk = 30 ns) 000: 8 clks. 001: 1 clk. 010: 2 clks. 011: 3 clks. 100: 4 clks. 101: 5 clks. 110: 6 clks. 111: 7 clks.
3-0 (0000)	**Data Read/Write Recovery Count**. These four bits are used to program the data read/write recovery timing count for Secondary Channel Drive 1. Clock is defined by PCI clock cycle time. The setting value will take effect for Secondary Channel Drive 1 data access only. (1 clk = 30 ns) 0000: 16 clks. 0001: 1 clk. 0010: 2 clks. 0011: 3 clks. 0100: 4 clks. 0101: 5 clks. 0110: 6 clks. 0111: 7 clks. 1000: 8 clks. 1001: 9 clks. 1010: 10 clks. 1011: 11 clks. 1100: 12 clks. 1101: 13 clks. 1110: 14 clks. 1111: 15 clks.

Note: 1 clk = 30 ns

The Power Management Register Block

31	16	15	0	
Power Management Capabilities (PMC)		Next Item Pointer	Capability ID	60h
Data	PMCSR_BSE Bridge Support Extensions	Power Management Control/Status Register (PMCSR)		64h
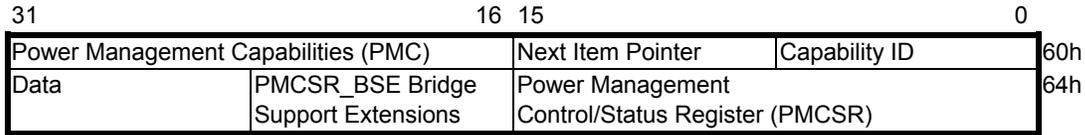
Device: **IDE Host Controller**
Register Index: **60h**
Register Name: **Capability ID (CAPID)**
Default Value: 01h
Attribute: Read/Write Lock

Bit	Description
7-0	This read-only register value "01" identifies the linked list item as being the PCI power management registers. This register is write-able when IDE_4A_D10 = '1'.

Device: **IDE Host Controller**
Register Index: **61h**
Register Name: **Next Item Pointer (NIP)**
Default Value: 00h
Attribute: Read/Write Lock

Bit	Description
7-0	This read-only register value "00" indicates that there are no additional items in the capabilities list. This register is write-able when IDE_4A_D10 = '1'.

Device: **IDE Host Controller**
Register Index: **63h-62h**
Register Name: **Power Management Capabilities (PMC)**
Default Value: 0002h
Attribute: Read/Write Lock

Bit	Description
15-11	**PME Support**. This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. The field value "00000" indicates that M5228 is not capable of asserting the PME#. This register is write-able when IDE_4A_D10 = '1'
10	**D2 Support**. The read-only bit value "0" indicates that M5228 does not support the D2 power management state. This register is write-able when IDE_4A_D10 = '1'
9	**D1 Support**. The read-only bit value "0" indicates that M5228 does not support the D1 power management state. This register is write-able when IDE_4A_D10 = '1'
8-6	Reserved (must be 0s).
5	**DSI**. The value '0' indicates that the special initialization is not required for the M5228. This register is write-able when IDE_4A_D10 = '1'.
4	Reserved (must be 0).
3	**PME Clock**. The value '0' indicates that no PCI clock is required for PME# operation for the M5228. This register is write-able when IDE_4A_D10 = '1'.
2-0	**Version**. A value of 010b indicates that M5228 complies with Revision 1.1 of the PCI Power Management Interface Specification. This register is write-able when IDE_4A_D10= '1'.

Device:	**IDE Host Controller**
Register Index:	**65h-64h**
Register Name:	**Power Management Control/Status Register (PMCSR)**
Default Value:	0000h
Attribute:	Read/Write Lock

Bit	Description
15	**PME Status**. This bit is set when M5228 will assert the PME# signal independent of the state of the PME Enable bit.
14-13	**Data Scale**. This 2-bit read only field indicates the scaling factor is to be used when interpreting the value of the Data register. This register is write-able when IDE_4A_D10 = '1'.
12-9	**Data Select**. This 4-bit is used to select which data is to be reported through the Data register and Data Scale field.
8	**PME Enable**. A "1" enables M5228 to assert PME#. When set to "0", PME# assertion is disabled. This bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.
7-2	Reserved (must be 0s).
1-0	**Power State**. This 2-bit field is used both to determine the current power state of M5228 and to set the M5228 into a new power state. The definition of the field value is given below. 00b – D0 01b – D1 (Not implemented) 10b – D2 (Not implemented) 11b – D3hot

Device:	**IDE Host Controller**
Register Index:	**66h**
Register Name:	**PMCSR Bridge Support Extensions (PMCSR_BSE)**
Default Value:	00h
Attribute:	Read Only

Device:	**IDE Host Controller**
Register Index:	**67h**
Register Name:	**Data Register (DATAR)**
Default Value:	00h
Attribute:	Read/Write Lock

Bit	Description
7-0	Data. This register is used to report the state dependent data requested by Data Select field. The value of this register is scaled by the value reported by the Data Scale.

Device:	**IDE Host Controller**
Register Index:	**FFh-68h**
Register Name:	**Reserved Register**
Default Value:	
Attribute:	Read Only

Note: Some registers are reserved by ULi for testing purpose only.

4.3 M5228 Configuration Space Register Index 09h Bit Definition

5228 Register Index 09h can disable the Primary and Secondary Channel. The following shows the detailed definition of each bit.

Note: 5228 only supports the native mode.

Index 09h - bit7 - bus master IDE
0: No, it is not a bus master IDE.
1: Yes, it is a bus master IDE.

Index 09h - bit6 - Report IDE channel status
0: No, this is the default zero value of PCI 2.2 specification.
1: Yes, bits [5:4] can be queried to determine status of the IDE controller.

Index 09h - bit5 - Primary Channel
0: No, the Primary channel is disabled.
1: Yes, the Primary channel is enabled.

Index 09h - bit4 - Secondary Channel
0: No, the Secondary channel is disabled.
1: Yes, the Secondary channel is enabled.

Index 09h - bit3 - Secondary Channel Support
0: Compatibility only.
1: Both compatibility and native mode.

Index 09h - bit2 - Operation of Secondary channel
0: Compatibility mode.
1: Native mode.

Index 09h - bit1 - Primary Channel Support
0: Compatibility mode only.
1: Both compatibility and native mode.

Index 09h - bit0 - Operation of Primary Channel
0: Compatibility mode.
1: Native mode.

4.3.1.1 PIO Mode IDE I/O Space Definition

Native Mode Only
Primary Channel I/O space can be programmed at Index 10h-14h. The I/O range is 8-byte at Index 10h and 1-byte at Index 14h. Secondary Channel I/O space can be programmed at Index 18h-1Ch. The I/O range is 8-byte at Index 18h and 1-byte at Index 1Ch.

4.4 Bus Master IDE IO Register Description

Bus Master IDE function uses 16 bytes of I/O space. All bus master IDE I/O spaces can be accessed as byte, word, or Dword. The descriptions of the 16 bytes of I/O registers are as follows:

Offset from Base Address	Register	Register Access
00h	Bus Master IDE Command Register Primary	R/W
01h	Device Specific	
02h	Bus Master IDE Status Register Primary	R/W Clear
03h	Device Specific	
04h-07h	Bus Master IDE PRD Table Address Primary	R/W
08h	Bus Master IDE Command Register Secondary	R/W
09h	Device Specific	
0Ah	Bus Master IDE Status Register Secondary	R/W Clear
0Bh	Device Specific	
0Ch-0Fh	Bus Master IDE PRD Table Address Secondary	R/W

Register Name: **Bus Master IDE Command register**
Address Offset: Primary Channel - Base address defined in Index 20h + 00h
Secondary Channel - Base address defined in Index 20h + 08h
Base Address: F001h
Default Value: 00h
Attribute: Read/Write

Bit	Description
7-4	Reserved. Must be 0.
3	**Read or Write Control**. This bit sets the direction of the bus master transfer. 0: PCI bus master read. 1: PCI bus master write. This bit must not be changed when the bus master function is active.
2-1	Reserved. Must be 0.
0	**Start/Stop Bus Master**. Writing a '1' to this bit enables bus master operation of the controller. Bus Master operation begins when this bit has detected a change from zero to one. The controller will transfer data between the IDE device and memory only when this bit is set. Writing a '0' to this bit can halt master operation. All state information is lost when a '0' is written; Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active and the drive has not yet finished its data transfer, the bus master command is said to be aborted and data transferred from the drive maybe discarded before being written to system memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master IDE active bit or the interrupt bit of the Bus master IDE status register for that IDE channel being set, or both.

Register Name: **SATA SCR Mapping Register Address Offset (only for M5281)**
Primary Channel - Base address defined in Index 20h + 01h
Secondary Channel - Base address defined in Index 20h + 09h
Base Address: F001h
Default Value: 00h
Attribute: Read Only

Bit	Description
7-0	SCR. SERR [7:0]

Register Name: **Bus Master IDE Status Register Address Offset**
Primary Channel - Base address defined in Index 20h + 02h
Secondary Channel - Base address defined in Index 20h + 0Ah
Base Address: F001h
Default Value: 00h
Attribute: Read/Write

Bit	Description
7	**Simplex Only**. (RO) This bit indicates whether or not both bus master channels (primary and secondary) can be operated at the same time. 0: Channels operate independently and can be used at a time. 1: Only one channel can be used at a time.
6	**Drive 1 DMA Capable**. (R/W) This bit is set by device dependent codes (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
5	**Drive 0 DMA Capable**. (R/W) This bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
4-3	Reserved. Must be 0.
2	**Interrupt**. This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a '1' is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is one, all data transferred from the drive is visible in system memory.
1	**Error**. This bit is set when the controller encounters an error in transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a '1' is written to it by software.
0	**Bus Master IDE Active**. This bit is set when the Start bit is written to the Command Register. This bit is cleared when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted.

Register Name: **SATA SCR Mapping Register Address Offset (only for M5281)**
Primary Channel - Base address defined in Index 20h + 03h
Secondary Channel - Base address defined in Index 20h + 0Bh
Base Address: F001h
Default Value: 00h
Attribute: Read Only

Bit	Description
7-4	SCR. Sstaus[3:0]
1-0	SCR. SERR [7:0]

Register Name: **Descriptor Table Pointer Register**
Primary Channel - Base address defined in Index 20h + 04h
Secondary Channel - Base address defined in Index 20h + 0Ch
Base Address: F001h
Default Value: 00000000h
Attribute: Read/Write

Bit	Description
31-2	Base address of Descriptor table. Corresponds to A[31:2]
1-0	Reserved.

4.4.1.1 Physical Region Descriptor Table

Before the controller starts a master transfer it is given a pointer to a Physical Region Descriptor Table. This table contains some number of Physical Region Descriptor (PRD) which describes the areas of memory that are involved in the data transfer. The PRD table must be aligned on a 4-byte boundary and the table cannot cross a 64K boundary in memory. The EOT stands for "END of TABLE" and is used to indicate that this transaction has ended.

	byte 3	byte 2	byte 1	byte 0		Memory Region
Dword0	Memory Region Physical Base Address [31:1]				0	
Dword1	EOT	Reserved	Byte Count[15:1]		0	
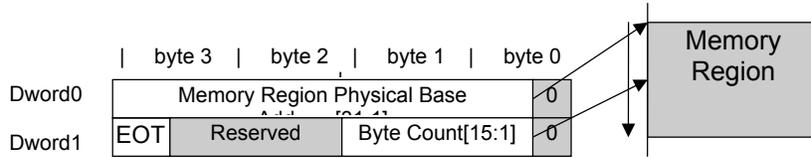
4.5 Flash ROM PCI Configuration Register

The following is the register summary table:

Byte Index	Definition	Attribute (R/W)	Default Value
01h-00h	Vender ID	RO	10B9h
03h-02h	Device ID	RO	5282h
05h-04h	Command	R/W	0000h
07h-06h	Status	RO, R/W Clear	02A0h
08h	Revision ID	RO	00h
0Bh-09h	Class Code	R/W	050100h
0Ch	Reserved	RO	00h
0Dh	Latency Timer	R/W	00h
0Eh	Header Type	RO	80h
0Fh	Reserved	RO	00h
13h-10h	Reserved	RO	00h
17h-14h	Reserved	RO	00h
1Bh-18h	Reserved	RO	00h
1Fh-1Ch	Reserved	RO	00h
23h-20h	Reserved	RO	00h
24h-27h	Reserved	RO	00000000h
2Bh-28h	CardBus Information Structure Pointer	RO	000000A0h
2Dh-2Ch	Subsystem Vendor ID	R/W Lock	10B9h
2Fh-2Eh	Subsystem Device ID	R/W Lock	5282h
33h-30h	ROM Base Address	RO	00050000h
34h	Capabilities Pointer	R/W Lock	50h
3Bh-35h	Reserved	RO	0s
3Ch	Interrupt Line	R/W	00h
3Dh	Interrupt Pin	RO	00h
3Fh-3Eh	Reserved	RO	0000h
40h	System Control Register 1	R/W	00h
41h	System Control Register 2	R/W	03h
42h	System Control Register 3	R/W	00h
43h	System Control Register 4	R/W	00h
44h	IO Pad Control Register 1	R/W	37h
45h	IO Pad Control Register 1	R/W	10h
46h	Process Monitor value	RO	00h
47h	Daisy Chain Mask Byte	R/W	01h
48h	Reserved	RO	00h
49h	Reserved	RO	00h
4Ah	Reserved	RO	00h
4Bh	Reserved	RO	00h
4Ch	Reserved	RO	00h
4Dh	Reserved	RO	00h
4Eh	Reserved	RO	00h
4Fh	Reserved	RO	00h
50h	Capability ID	R/W Lock	02h
51h	Next Item Pointer	R/W Lock	00h
53h-52h	Power Management Capabilities	R/W Lock	0002h
55h-54h	Power Management Control/Status Register	R/W Lock	0000h
56h	PMCSR Bridge Support Extensions	RO	00h
57h	Data Register	R/W Lock	00h
A7-A0h	CardBus Information Structure Data	RO	00h

Device: **Flash ROM Controller**

Register Index:	**01h-00h**
Register Name:	**Vendor ID Register (VID)**
Default Value:	10B9h
Attribute:	Read Only

Bit	Description
15-0	This is a 16-bit value assigned to ULi. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Device:	**Flash ROM Controller**
Register Index:	**03h-02h**
Register Name:	**Device ID Register (DID)**
Default Value:	5282h
Attribute:	Read Only

Bit	Description
15-0	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device. Write to this register has no effect.

Device:	**Flash ROM Controller**
Register Index:	**05h-04h**
Register Name:	**Command Register (COM)**
Default Value:	0000h
Attribute:	Read/Write

Bit	Description
15-11	Reserved. These bits are always 0.
10	Reserved.
9	**Back-to-Back Enable**. FLASH ROM CONTROLLER only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8	**Enable the SERRJ driver**. When this bit is set, FLASH ROM CONTROLLER will enable SERRJ output driver. This bit is reset to 0 and will set to 1 when it detects an address parity error. SERRJ is not asserted if this bit is 0.
7	**Wait Cycle Control** - FLASH ROM CONTROLLER does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6	**Respond to Parity Errors**. If set to 1, the FLASH ROM CONTROLLER block will assert an internal PERRJ when it is the agent receiving data and it detects a data parity error.
5	**Enable VGA Palette Snooping**. This bit is always 0.
4	**Memory Write and Invalidate Command**. FLASH ROM CONTROLLER will never issue Memory Write and Invalidate commands. This bit is always 0. Write to this bit has no effect.
3	**Enable Special Cycle**. FLASH ROM CONTROLLER will not accept special cycles on PCI. This bit is always 0. Write to this bit has no effect.
2	**Enable PCI Master**. This bit is reset as 0 during Power-On to disable PCI master operations.
1	**Enable Response to Memory Access**. This bit is reset as 0 during Power-On to disable the response to Memory access. This bit must be enabled for FLASH ROM operation.
0	**Enable Response to I/O Access**. This bit is reset as 0 during Power-On to disable the response to I/O access.

Device: **Flash ROM Controller**
Register Index: **07h-06h**
Register Name: **Device Status Register (DS)**
Default Value: 0280h
Attribute: Read Only, Read/Write Clear

Bit	Description
15	**Detected Parity Error**. This bit is set by FLASH ROM CONTROLLER to 1 whenever it detects a parity error, even if the Respond to Parity Errors bit (command register, bit 6) is disabled. This bit is cleared (reset to 0) by writing a 1 to it.
14	**SERRJ Status**. This bit is set by FLASH ROM CONTROLLER to 1 whenever it detects a PCI address parity error. This bit is cleared (reset to 0) by writing a 1 to it.
13	**Received Master Abort Status**. This bit is set to 1 when FLASH ROM CONTROLLER, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12	**Received Target Abort Status**. This bit is set to 1 when a FLASH ROM CONTROLLER generated PCI cycle (FLASH ROM CONTROLLER is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11	**Sent Target Abort Status**. FLASH ROM CONTROLLER as a slave never generates a Target abort. This bit is always 0.
10-9	**DEVSELJ Timing**. Read only bits indicating DEVSELJ timing when performing a positive decode. 00: Fast. 01: Medium. 10: Slow. Since DEVSELJ is asserted by FLASH ROM CONTROLLER to meet the medium timing, these bits are encoded as 01b.
8	**Data Parity Reported**. Set to 1 if the Respond to Parity Error bit (Command Register bit 6) is set, and FLASH ROM CONTROLLER detects internal PERRJ asserted while acting as PCI master (whether internal PERRJ was driven by FLASH ROM CONTROLLER or not).
7	**Fast Back-to-Back Capable**. FLASH ROM CONTROLLER supports fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
7-5	Reserved. These bits are always 0.
4	**Capabilities**. FLASH ROM CONTROLLER supports a pointer for an extended capabilities linked list at FLASH_34_D[7:0]. 0: Disable capabilities linked list function (default) 1: Enable capabilities linked list function ** This bit will be Read only when FLASH_42_D[0] = '0' (default)
3	**Interrupt Status**. This read-only bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's **INTx#** signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2-0	Reserved. These bits are always 0.

Device: **Flash ROM Controller**
Register Index: **08h**
Register Name: **Revision ID Register (RID)**
Default Value: 00h
Attribute: Read Only

Bit	Description
7-0	This register contains the version number of the Flash ROM controller.

Device:	**Flash ROM Controller**
Register Index	**0Bh-09h**
Register Name:	**Class Code Register (CC)**
Default Value	050100h
Attribute:	Read/Write

Bit	Description
23-8	Value 0501h identifies the Base Class and Sub-Class Code of Flash ROM controller.
7-0	Reserved

Device:	**Flash ROM Controller**
Register Index:	**0Ch**
Register Name:	**Reserved Register**
Default Value	00h
Attribute:	Read Only

Device:	**Flash ROM Controller**
Register Index:	**0Dh**
Register Name:	**LT - Latency Timer**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7-0	This register identifies the value of latency timer in PCI clocks for PCI bus master cycles.

Device:	**Flash ROM Controller**
Register Index:	**0Eh**
Register Name:	**Header Type Register (HT)**
Default Value	80h
Attribute:	Read Only

Bit	Description
7-0	This register identifies the type of predefined header in the configuration space. Since the Flash ROM controller is a multi-function device and not a PCI-to-PCI bridge, this byte should be read as 80h.

Device:	**Flash ROM Controller**
Register Index:	**0Fh**
Register Name:	**Reserved Register**
Default Value:	00h
Attribute:	Read Only

Device:	**Flash ROM Controller**
Register Index:	**13h-10h**
Register Name:	**Reserved Register**
Default Value:	00s
Attribute:	Read Only

Device: **Flash ROM Controller**
Register Index: **17h-14h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **Flash ROM Controller**
Register Index: **1Bh-18h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **Flash ROM Controller**
Register Index: **1Fh-1Ch**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **Flash ROM Controller**
Register Index: **23h-20h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **Flash ROM Controller**
Register Index: **2Bh-24h**
Register Name: **Reserved Register**
Default Value: 00s
Attribute: Read Only

Device: **Flash ROM Controller**
Register Index: **2Dh-2Ch**
Register Name: **Subsystem Vendor ID (SVID)**
Default Value: 10B9h
Attribute: Read/Write Lock

Device: **Flash ROM Controller**
Register Index: **2Fh-2Eh**
Register Name: **Subsystem Device ID (SDID)**
Default Value: 5282h
Attribute: Read/Write Lock

Device:	**Flash ROM Controller**
Register Index:	**33h-30h**
Register Name:	**Expansion ROM Base Address Register**
Default Value:	00050000h
Attribute:	Read Only

Bit	Description
0	Address decode enable. It is used to control whether the device accepts accesses to its expansion ROM.
10-1	Reserved
31-11	Expansion ROM Base Address.

Device:	**Flash ROM Controller**
Register Index:	**34h**
Register Name:	**Capabilities Pointer (CAPPTR)**
Default Value:	50h
Attribute:	Read/Write Lock

Bit	Description
7-0	The Capabilities Pointer point to the Flash ROM controller configuration space for the location of the first item in the Capabilities linked list. The Capabilities Pointer offset is DWORD aligned. If the Capability bit is enabled (index 06h bit 4), the default value will be 50h.

Device:	**Flash ROM Controller**
Register Index:	**3Bh-35h**
Register Name:	**Reserved Register**
Default Value:	00s
Attribute:	Read Only

Device:	**Flash ROM Controller**
Register Index:	**3Ch**
Register Name:	**Interrupt Line Register (IL)**
Default Value:	00h
Attribute:	Read/Write

Bit	Description
7-0	This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct effect to the Flash ROM controller.

Device:	**Flash ROM Controller**
Register Index:	**3Dh**
Register Name:	**Interrupt Pin Register (IP)**
Default Value:	00h
Attribute:	Read Only

Bit	Description
7-0	This register identifies which interrupt pin a device uses. Since Flash ROM controller does not use INTA#, this value is set to 00h.

Device: **Flash ROM Controller**
Register Index: **3Eh-3Fh**
Register Name: **Reserved Register**
Default Value: 0000h
Attribute: Read Only

Device: **Flash ROM Controller**
Register Index: **40h**
Register Name: **System Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description
4-0	**Serial ROM software control**. Bit 0: Serial ROM re-load Bit 1: Serial ROM chip select Bit 2: Serial ROM clock Bit 3: Serial ROM data out Bit 4: Serial ROM data in
6-5	Reserved.
7	Force to enable the Serial ROM. 0: Arbitrate with Flash ROM interface. 1: Serial ROM interface.

Device: **Flash ROM Controller**
Register Index: **41h**
Register Name: **System Control Register**
Default Value: 03h
Attribute: Read/Write

Bit	Description
0	**Enable/Disable PATA channel 1**. 0: Disable 1: Enable (Default)
1	**Enable/Disable PATA channel 2.** 0: Disable 1: Enable (Default)
2	**CLKRUN# / SERR# selection.** **0: SERR#** **1: CLKRUN#**
3	Reserved.
4	**Test-pin mux select**. 0: Normal (Default) 1: Change to test pin for ROM interface's IO (Reserved for ULi only.)
7-5	Reserved.

Device: **Flash ROM Controller**
Register Index: **42h**
Register Name: **System Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description
0	**R/W-lock PCI Power Management Capabilities List**. 0: RO (Default) 1: R/W
1	Reserved.
2	**CardBus support**. 0: None (Default) 1: Done.
7-3	Reserved.

Device: **Flash ROM Controller**
Register Index: **43h**
Register Name: **System Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description
6-0	Reserved.
7	**R/W-lock Revision ID (index 08h) & Subsystem ID (index 2Fh – 2Ch)** 0: RO 1: R/W

Device: **Flash ROM Controller**
Register Index: **45h – 44h**
Register Name: **IO Pad Control Register**
Default Value: 1037h
Attribute: Read/Write

Bit	Description
3-0	**Driving for PCI IO Pads**

Driving bit control				
Driving_3	Driving_2	Driving_1	Driving_0	Driving capacity
0	0	0	0	2ma
0	0	0	1	4ma
0	0	1	0	6ma
0	0	1	1	8ma
0	1	0	0	10ma
0	1	0	1	12ma
0	1	1	0	14ma
0	1	1	1	16ma
1	1	0	0	18ma
1	1	0	1	20ma
1	1	1	0	22ma
1	1	1	1	24ma

As the HW setting is set to control the PCI IO pads driving capability, the {Ddiving_2, Driving_1} is only affected by the HW setting.

Bit	Description
7-4	**Driving for PATA IO Pads**

Driving bit control				
Driving_3	Driving_2	Driving_1	Driving_0	Driving capacity
0	0	0	0	2ma
0	0	0	1	4ma
0	0	1	0	6ma
0	0	1	1	8ma
0	1	0	0	10ma
0	1	0	1	12ma
0	1	1	0	14ma
0	1	1	1	16ma
1	1	0	0	18ma
1	1	0	1	20ma
1	1	1	0	22ma
1	1	1	1	24ma

Bit	Description
8	**Slew rate control for PCI IO Pad** 0: slow slew rate 1: quick slew rate
9	**Smitter trigger control for PCI IO Pad** 0: Smitter trigger 1: Normal
10	**Power down control for PCI IO Pad** 0: Normal 1: Power down
11	Reserved.
12	**Slew rate control for PATA IO Pad** 0: slow slew rate 1: quick slew rate
13	**Smitter trigger control for PATA IO Pad** 0: Smitter trigger 1: Normal
14	**Power down control for PATA channel 1 IO Pad** 0: Normal 1: Power down
15	**Power down control for PATA channel 2 IO Pad** 0: Normal 1: Power down

Device:	**Flash ROM Controller**
Register Index:	**46h**
Register Name:	**Process Monitor Register**
Default Value:	00h
Attribute:	Read Only

Bit	Description
7-0	Value for Process Monitor.

Device:	**Flash ROM Controller**
Register Index:	**47h**
Register Name:	**Daisy Chain structure Mask Byte Register**
Default Value:	01h
Attribute:	Read/Write

Bit	Description
1-0	**Daisy Chain Structure Position**. Use this to control which 5281 of the Daisy Chain is programmed. 00: Reserved. 01: First one 10: Second one. 11: Third one.
7-2	Reserved

Device:	**Flash ROM Controller**
Register Index:	**50h**
Register Name:	**Capability ID (CAPID)**
Default Value:	01h
Attribute:	Read/Write Lock

Bit	Description
7-0	This read-only register value "01" identifies the linked list item as being the PCI power management registers. This register is write-able when FLASH_42_D0 = '1'.

Device:	**Flash ROM Controller**
Register Index:	**51h**
Register Name:	**Next Item Pointer (NIP)**
Default Value:	00h
Attribute:	Read/Write Lock

Bit	Description
7-0	This read-only register value "00" indicates that there are no additional items in the capabilities list. This register is write-able when FLASH_42_D0 = '1'.

Device: **Flash ROM Controller**
Register Index: **53h-52h**
Register Name: **Power Management Capabilities (PMC)**
Default Value: 0002h
Attribute: Read/Write Lock

Bit	Description
15-11	**PME Support**. This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. The field value "00000" indicates that M5228 is not capable of asserting the PME#. This register is write-able when FLASH_42_D0 = '1'
10	**D2 Support**. The read-only bit value "0" indicates that M5228 does not support the D2 power management state. This register is write-able when FLASH_42_D0 = '1'
9	**D1 Support**. The read-only bit value "0" indicates that M5228 does not support the D1 power management state. This register is write-able when FLASH_42_D0 = '1'
8-6	Reserved (must be 0s).
5	**DSI**. The value '0' indicates that the special initialization is not required for the M5228. This register is write-able when FLASH_42_D0 = '1'.
4	Reserved (must be 0).
3	**PME Clock**. The value '0' indicates that no PCI clock is required for PME# operation for the M5228. This register is write-able when FLASH_42_D0 = '1'.
2-0	**Version**. A value of 010b indicates that M5228 complies with Revision 1.1 of the PCI Power Management Interface Specification. This register is write-able when FLASH_42_D0= '1'.

Device: **Flash ROM Controller**
Register Index: **55h-54h**
Register Name: **Power Management Control/Status Register (PMCSR)**
Default Value: 0000h
Attribute: Read/Write Lock

Bit	Description
15	**PME Status**. This bit is set when M5228 is to assert the PME# signal independent of the state of the PME Enable bit.
14-13	**Data Scale**. This 2-bit read only field indicates the scaling factor to use when interpreting the value of the Data register. This register is write-able when FLASH_42_D0 = '1'.
12-9	**Data Select**. This 4-bit is used to select which data is to be reported through the Data register and Data Scale field.
8	**PME Enable**. A "1" enables M5228 to assert PME#. When "0" PME# assertion is disabled. This bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.
7-2	Reserved (must be 0s).
1-0	**Power State**. This 2-bit field is used both to determine the current power state of M5228 and to set the M5228 into a new power state. The definition of the field values is given below. 00b – D0 01b – D1 (Not implemented) 10b – D2 (Not implemented) 11b – D3hot

Device: **Flash ROM Controller**
Register Index: **56h**
Register Name: **PMCSR Bridge Support Extensions (PMCSR_BSE)**
Default Value: 00h
Attribute: Read Only

Device: **Flash ROM Controller**
Register Index: **57h**
Register Name: **Data Register (DATAR)**
Default Value: 00h
Attribute: Read/Write Lock

| Bit	Description
7-0	Data. This register is used to report the state dependent data requested by Data Select field. The value of this register is scaled by the value reported by the Data Scale.

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5. Packaging Information

160LD LQFP Package Outline
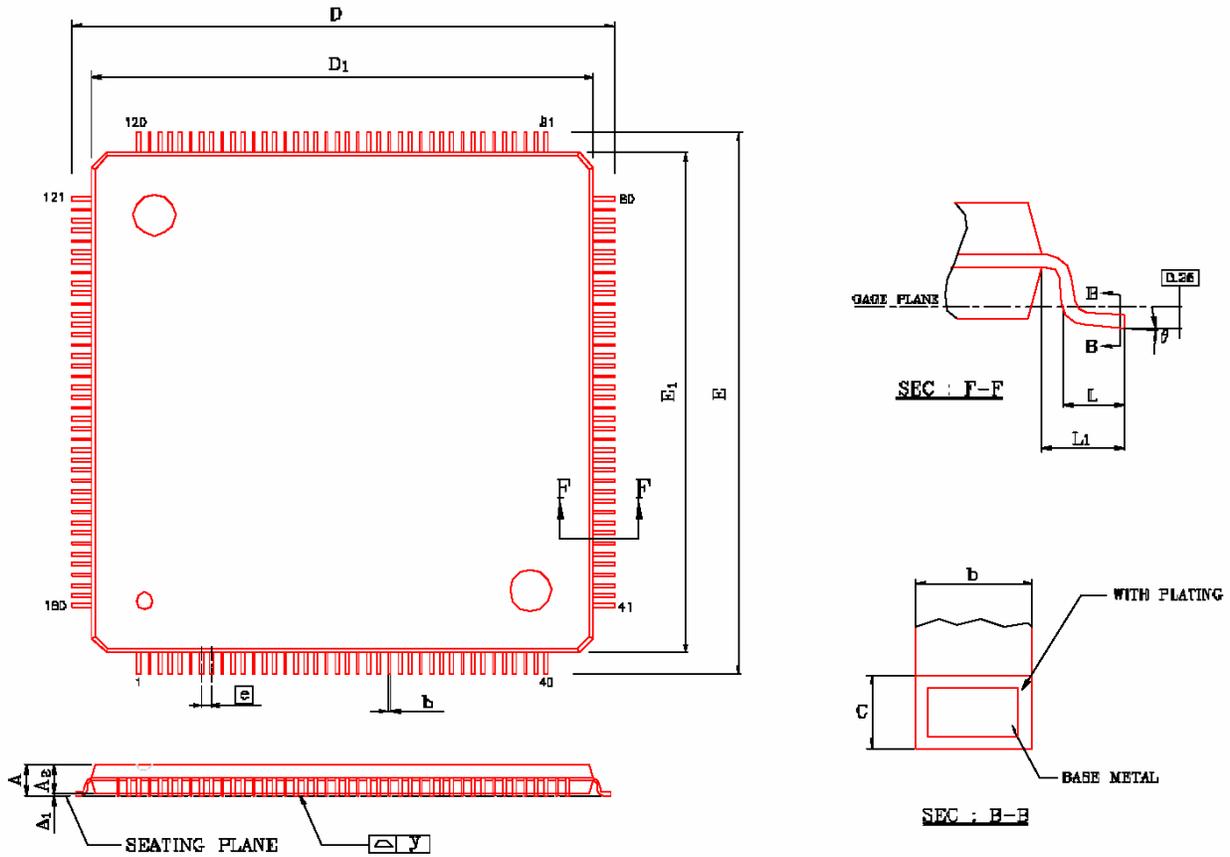
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A₁	0.002	—	—	0.05	—	—
A₂	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.005	—	0.008	0.12	—	0.20
D	1.018	1.024	1.030	25.85	26.00	26.15
D₁	0.941	0.945	0.949	23.90	24.00	24.10
E	1.018	1.024	1.030	25.85	26.00	26.15
E₁	0.941	0.945	0.949	23.90	24.00	24.10
e	0.020 BSC			0.50 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L₁	0.039 REF			1.00 REF		
y	—	—	0.003	—	—	0.08
θ	0°	3.5°	7°	0°	3.5°	7°

NOTE :

⚠ TO BE DETERMINED AT SEATING PLANE ⊏C⊐ .

⚠ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMACH.

⚠ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

⚠ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

⚠ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.

⚠ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

7. CONTROLLING DIMENSION : MILLIMETER.

8. REFERENCE DOCUMENT : JEDEC MS-026 , BHB.

Appendix A. EEPROM Contents

EEPROM Contents

Word No.	Function	Register	PCI Register Offset	Default Value
1-0		Data signature		55AA55Aah (Note *1)
2	Flash ROM	Flash ROM Device ID		5282h
4-3	Flash ROM	Flash ROM Subsystem ID	2Fh-2Ch	528210B9h
8-5	Flash ROM	Flash ROM CIS Information Register	A7h-A0h	00h
10-9	SATA	SATA Subsystem ID	2Fh-2Ch	528110B9h
14-11	SATA	SATA CIS Information Register	A7h-A0h	00h
16-15	PATA	PATA Subsystem ID	2Fh-2Ch	522810B9h
20-17	PATA	PATA CIS Information Register	A7h-A0h	00h

Flash ROM Contents

Byte No.	ROM Offset	Function	Register	PCI Register Offset	Default Value
3-0	FFFCh - FFFFh		Data signature		AA55AA55h (Note *1)
5-4	FFFAh - FFFBh	Flash ROM	Flash ROM Device ID		8252h
9-6	FFF6h - FFF9h	Flash ROM	Flash ROM Subsystem ID	2Fh-2Ch	B9108252h
17-10	FFEEh - FFF5h	Flash ROM	Flash ROM CIS Information Register	A7h-A0h	00h
21-18	FFEAh - FFEDh	SATA	SATA Subsystem ID	2Fh-2Ch	B9108152h
29-22	FFE2h - FFE9h	SATA	SATA CIS Information Register	A7h-A0h	00h
33-30	FFDEh - FFE1h	PATA	PATA Subsystem ID	2Fh-2Ch	B9108252h
41-34	FFD6h - FFDDh	PATA	PATA CIS Information Register	A7h-A0h	00h

Note *1: Data signature value must be as described. The other values are samples only.

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