VT8501
Apollo MVP4

Design Guide

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INTRODUCTION

This document provides design guidelines for motherboard manufacturers on developing single Socket 7 processor and VIA Apollo MVP4 (VT8501) based systems. All the major underlying subsystems, especially Host Interface, Memory and Graphic subsystems, related to the motherboard design are described in detail. General layouts, routing guidelines and power requirements of each subsystem are presented.

1.1 About This Design Guide

A brief description of each chapter is given below:

Chapter 1: Introduction. An overview of Apollo MVP4 reference design features is given in this chapter along with general recommendations on MVP4 system design.

Chapter 2: Motherboard Design Guidelines. General design schemes and recommended layout rules are shown in chapter 2. It begins with the 492-pin BGA ballout assignment. The following section contains placement and routing of a motherboard, PCB stack-up information and power requirements for a desktop system. Detailed placement, layout, and routing guidelines for each bus or subsystem (Host bus, Memory subsystem, Graphic subsystem and PCI bus) are described in section 2.3.

Chapter 3: Timing Diagram Analysis. Timing analyses for cache control cycles and memory read/write cycles are discussed in Chapter 3.

Chapter 4: Electrical Specifications. The electrical specifications for the VT8501 North Bridge are listed in this chapter.

Chapter 5: Signal Connectivity and Design Checklist. This final chapter provides signal connection tables as a brief reference for hardware design engineers who are experienced in PC motherboard design. Also some design checklists can be used for reviewing the Apollo MVP4 system design.

Appendices: Reference Design Schematics. Reference schematics for the Apollo MVP4 system design with Super South Bridge Controller (VT82C686A), TMDS transmitter, TV encoder, TV decoder, and VIA AC'97 Codec are shown in appendices.

1.2 Apollo MVP4 Chipset Overview

The VIA Apollo MVP4 (VT8501) is a PC Socket-7 system logic North Bridge with an integrated 2D/3D graphics accelerator. The core logic portion of the chip is based on the VIA Apollo MVP3 (VT82C598/598MVP) with the addition of a state-of-the-art high performance 2D/3D graphic accelerator designed by Trident Microsystems, Inc. The combination of these two leading edge technologies provides a stable, cost effective and high performance solution for the personal computer market. The features of an Apollo MVP4 system are listed below:

- Socket 7 CPU (66-100MHz)
- L2 Cache and Tag RAM
- SDRAM Memory Interface
- PCI Bus (30-33MHz)
- Analog RGB Monitor with DDC
- Various Flat Panels or Digital Monitor Transmitter (TMDS or LVDS) Interfaces
- Video Capture / Playback Codec

A block diagram of a typical Apollo MVP4 based system with "Super South" South Bridge (VT82C686A) is shown in Figure1-1. The Apollo MVP4 supports a single Socket-7 processor including 64-bit Intel Pentium ™ / Pentium ™ with MMX ™, AMD 6K86 ™ (K6 ™ and K6-2 ™), Cyrix/National 6X86 ™/6X86MX ™, IDT/Centaur C6 and Rise MP6 CPUs at the maximum 100MHz system bus frequency. The VT82C686A Super-IO PCI Integrated Peripheral Controller (PSIPC) is a high integration, high performance, power efficient and high compatibility device that supports Intel and non-Intel based processors plus PCI bus bridge functionality to make a complete Microsoft PC98-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C686A includes the following standard intelligent peripheral controllers:

- Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands
- 4-Port Universal Serial Bus controller that is USB v1.1 and Universal HCI v1.1 compliant
- Keyboard controller with PS2 mouse support
- Real Time Clock with 256 bytes extended CMOS
- Power management functionality compliant with ACPI and legacy APM requirements
- Hardware monitoring subsystem for managing system/motherboard voltage levels, temperatures, and fan speed
- Full System Management Bus (SMBus) interface
- Two 16550-compatible serial I/O ports with infrared communication port option
- Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system.
- Two game ports and one MIDI port
- ECP/EPP-capable parallel port
- Standard floppy disk drive interface
- Distributed DMA capability for support of ISA legacy DMA over the PCI bus. Serial IRQ is also supported for docking and non-docking applications
- Plug and play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel

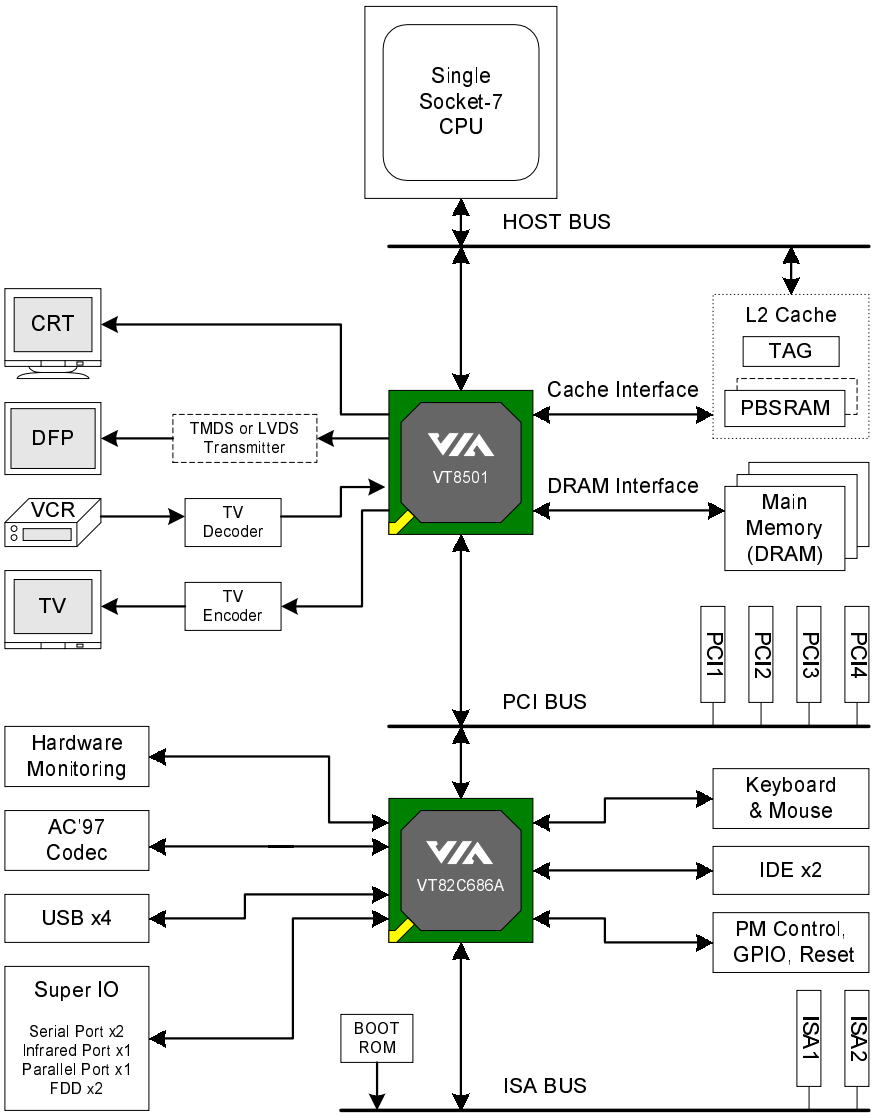


Figure 1-1. Apollo MVP4 System Block Diagram Using the VT82C686A Super South Bridge

1.3 System Design Recommendations

Both the Apollo MVP4 (VT8501) and Super South (VT82C686A) give rise to VIA's most optimized chipset combination for Socket-7 based PC systems. On an ATX form factor, for example, the optimized system specification for such a combination is listed below:

- Single Socket 7 CPU (66-100MHz)
- MVP4 single chip clock synthesizer
- Apollo MVP4 North Bridge (Host/PCI) Controller
- L2 Cache (512KB or 1MB) & Tag RAM (32KB or 64KB)
- Three DIMM Slots (maximum 768MB and 100MHz memory frequency)
- One CRT Interface (supporting of non-interlaced 1280x1024x64K, 1024x768x16M, 800x600x16M, and 640x480x16M)
- One 24-bit Flat Panel Interface (supporting standard TFT and STN panels or driving external TMDS or LVDS transmitters)
- One Video Capture Interface
- One TV Out Interface
- Four PCI Slots (30-33MHz)
- Two ISA Slots
- One 2MB Flash ROM for system and Graphics Controller BIOS
- One AC'97 Link Controller (to cooperate with an AC'97 CODEC chip)
- Four Universal Serial Bus Ports
- PS2 Keyboard/Mouse Support
- Two Enhanced IDE Interfaces supporting both ATA-33 and ATA-66
- One Floppy Drive Interface
- One Infrared Interface
- Various Hardware Monitoring functions (supporting 5 positive voltages, 3 temperatures, and 2 fan-speed monitoring inputs)
- One parallel Port and Two Serial Ports
- One MIDI Port
- One Game Port

For the rest of this document, the specification above will be used as a reference example for component placement and PCB layout.

MOTHERBOARD DESIGN GUIDELINES

This chapter describes general design schemes and recommended layout rules. It begins with the 492-pin BGA ballout assignment. The following section contains the placement and routing of a motherboard, PCB stack-up information and power requirements for a desktop system. Detailed placement, layout, and routing guidelines for each bus or subsystem (Host bus, Memory subsystem, Graphic subsystem and PCI bus) are described in section 2.3.

2.1 BGA Ballout Assignment

Basically, the chipset ballout plays an important role in motherboard designs. It can determine the quality of the Printed Circuit Board (PCB) layout. The reliability of a motherboard depends on the ballout of both the North Bridge and the South Bridge. To achieve a cost effective and compact 4-layer motherboard, the ballouts should be well defined because they have an inseparable relationship with component placement and PCB layout.

Ballouts of both the Apollo MVP4 North Bridge and the "Super South" South Bridge are designed to minimize the number of crossover signals. Figure 2-1 shows the four major signal group quadrants of the Apollo MVP4 Ballout. They are Host, Memory, Graphics and PCI interfaces. Please refer to the VT8501 datasheet for more details on ball assignments.

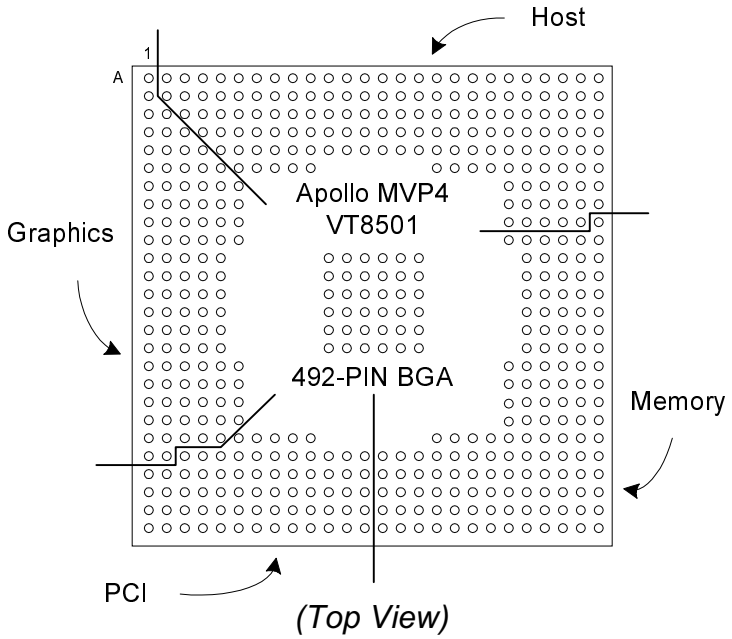


Figure 2-1. Major Signal Group Distributions of the Apollo MVP4 Ballout (Top View)

Similarly to Figure 2-1, the major signal group quadrants of the "Super South" South Bridge are shown in Figure 2-2. They are PCI, ISA, Hardware Monitoring, IDE1, IDE2 (shared with Audio/Game), Super IO (including FDC, COM, LPT, and Infrared interface (not shown)), USB, Keyboard & Mouse, and a group of Power Control, GPIO & Reset. Please refer to the VT82C686A datasheet for more details on these ball assignments.

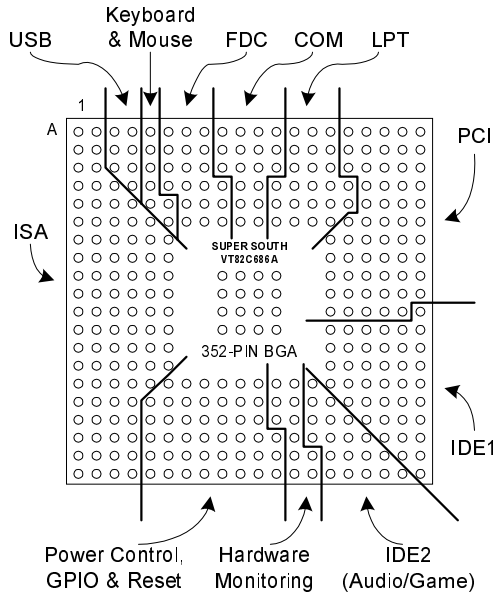


Figure 2-2. Major Signal Group Distributions of "Super South" South Bridge Ballout (Top View)

Package Information:

- The VIA Apollo MVP4 North Bridge (VT8501) is a 492-pin Ball Grid Array (BGA) package. The package size is 35mm x 35mm and the grid matrix is 26x26.
- The VIA "Super South" South Bridge (VT82C686A) is a 352-pin BGA package. The package size is 27mm x 27mm and the grid matrix is 20x20.

2.2 Motherboard Description

This section illustrates proposed component placements for an Apollo MVP4 based motherboard with different system configurations to achieve maximum optimization. The description of the Printed Circuit Board (PCB) for a motherboard is also given.

2.2.1 Motherboard Placement and Routing

For Apollo MVP4 PC motherboard designs, proposed placements and group signal routings of the three most popular form factors (ATX, micro-ATX and Baby AT) are shown in figures 2-3, 2-4 and 2-5. Detailed layout guidelines and signal routings will be addressed later in section 2.3.

Each figure shows a full size of its respective form factor. The empty area at the bottom of each placement diagram can be eliminated to reduce the board size. Table 2-1 shows the full size and the suggested compact size for each form factor implementation.

Table 2-1. Different Board Size Lists

Form Factor Type	Full size	Compact Size	Specification
ATX	12" x 9.6" (30.5cm x 24.5cm)	12" x 7" (30.5cm x 18cm)	4 PCI, 2 ISA, 3 DIMM, 1 PBSRAM
Micro-ATX	9.6" x 9.6" (24.5cm x 24.5cm)	9.6" x 7.9" (24.5cm x 20cm)	3 PCI, 1 ISA, 3 DIMM, 1 PBSRAM
Baby-AT	8.7" x 13" (22cm x 33cm)	8.7" x 9.5" (22cm x 24cm)	3 PCI, 1 ISA, 3 DIMM, 1 PBSRAM

2.2.1.1 ATX Form Factor

A proposed component placement and signal group routing for an Apollo MVP4 ATX form factor system design is illustrated in Figure 2-3. The major components on the board are: single Socket-7 CPU, four PCI slots, two ISA slots and three DIMM slots. This Figure shows an ATX motherboard placement as a reference only. The placement should be re-evaluated if a different combination of PCI and ISA slots and other motherboard peripherals is desired.

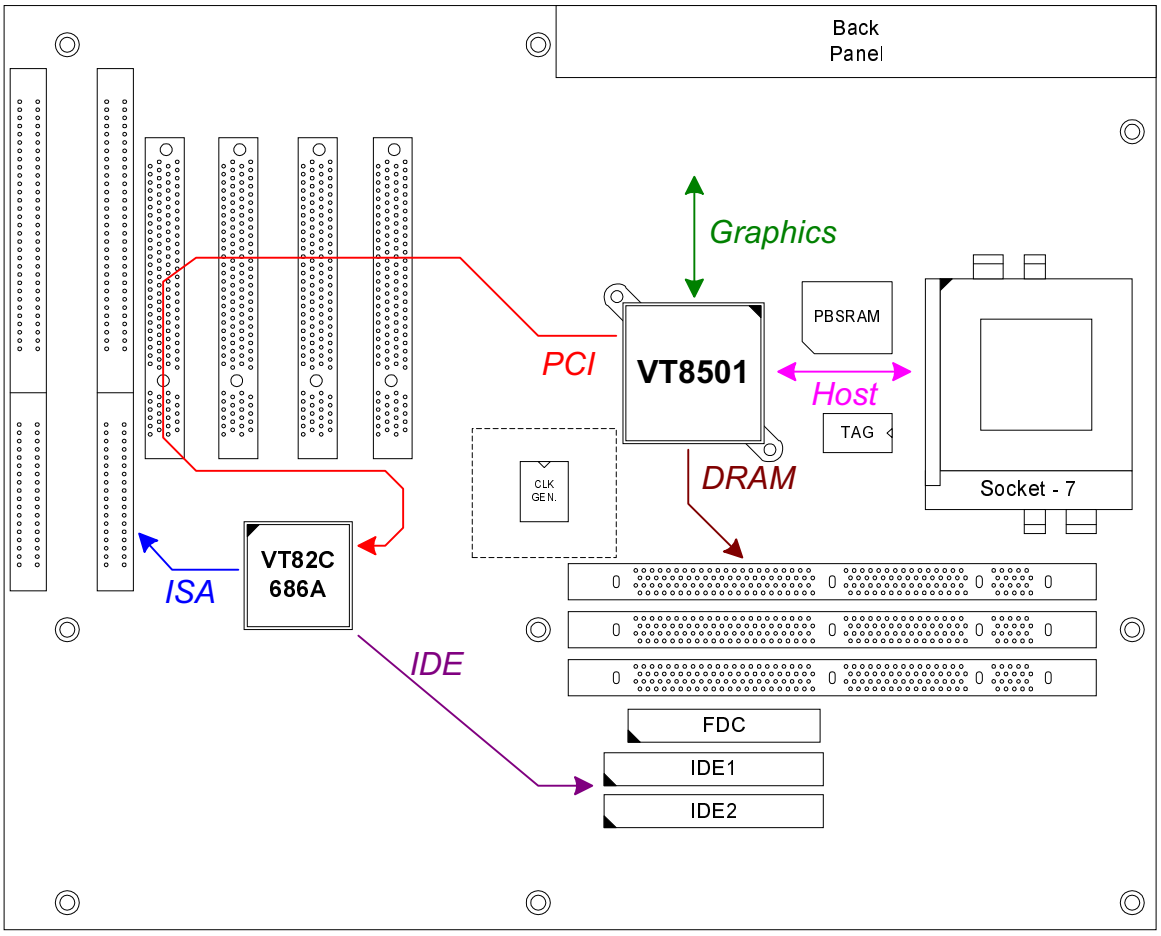


Figure 2-3. ATX Placement and Routing Example

2.2.1.2 Micro ATX Form Factor

A proposed component placement and signal group routing for an Apollo MVP4 micro-ATX system design is illustrated in Figure 2-4. The major components on the board are: single Socket-7 CPU, three PCI slots, one ISA slot and three DIMM slots. This Figure shows a reference only micro-ATX motherboard placement. The placement should be re-evaluated if a different combination of PCI and ISA slots and other motherboard peripherals is desired.

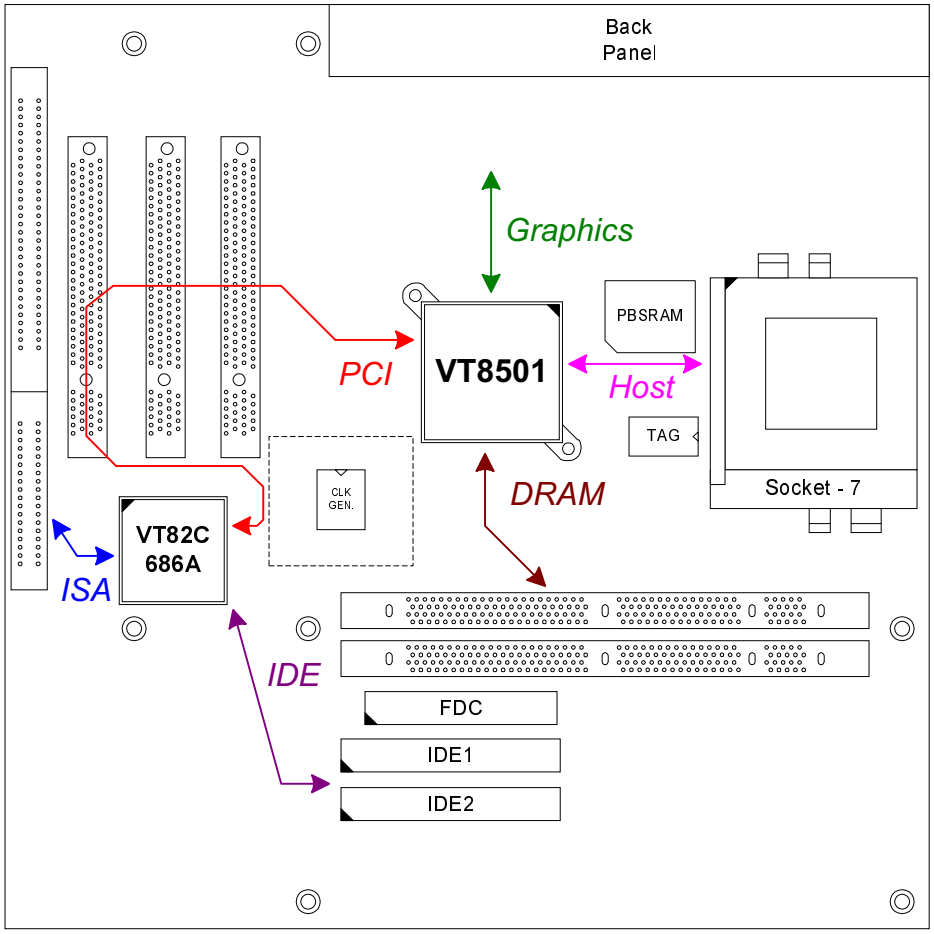


Figure 2-4. Micro-ATX Placement and Routing Example

2.2.1.3 Baby AT Form Factor

Figure 2-5 illustrates a proposed component placement and signal group routing for an Apollo MVP4 Baby-AT form factor system design. The major component combination is the same as that of the Micro-ATX form factor above. A reference example of the Baby-AT motherboard placement is shown in this Figure. The placement displayed should be re-evaluated if a different slot combination is chosen.

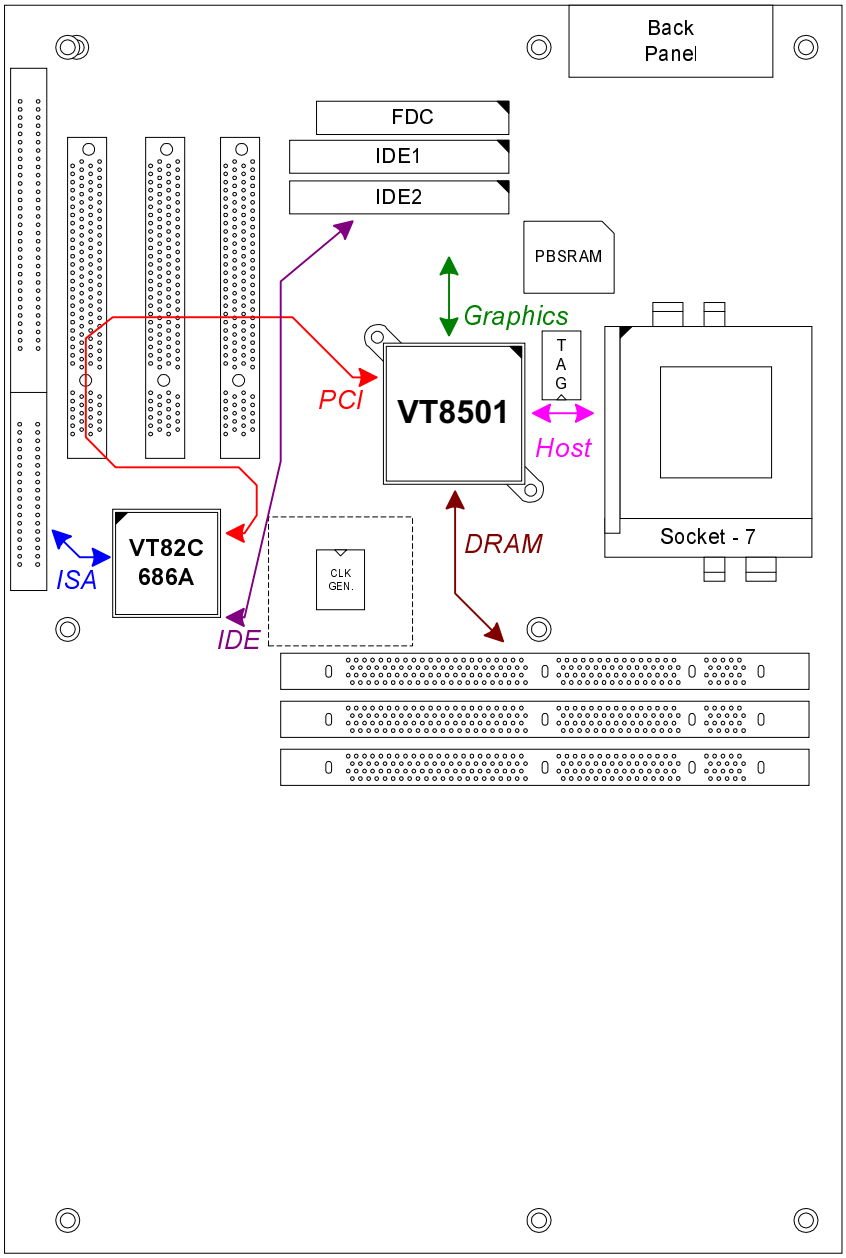


Figure 2-5. Baby-AT Placement and Routing Example

2.2.2 Printed Circuit Board Description

A brief description of the Printed Circuit Board (PCB) for an Apollo MVP4 based system is provided in this section. From a cost-effectiveness point of view, a four-layer board is recommended for the motherboard design. For better quality, a six-layer board is preferred. These two types of boards will be discussed below:

2.2.2.1 Four-Layer Board

A four-layer stack-up with 2 signal layers and 2 power planes is shown in Figure 2-6. The two signal layers are referred to as the component layer and the solder layer. The two power planes are the power layer and the ground layer. The sequence of component layer-ground layer-power layer-solder layer is the most common stack-up arrangement from top to bottom. It is recommended to place a 6-mil substrate between the solder layer and the power plane and between the component layer and the ground plane, with a 40-mil substrate between the power and ground planes. Dielectric constant, E_r, should be 4.5 for all substrate materials.

Routing any signal trace on the power planes, either on the power layer or on the ground layer, is not recommended. If a signal must be routed on the power planes, then it should be routed as short as possible on the power layer, not on the ground layer. The impedance of all signal layers is to be in the range between 55 ohms and 75 ohms. Lower trace impedance providing better signal quality is preferred over higher trace impedance.

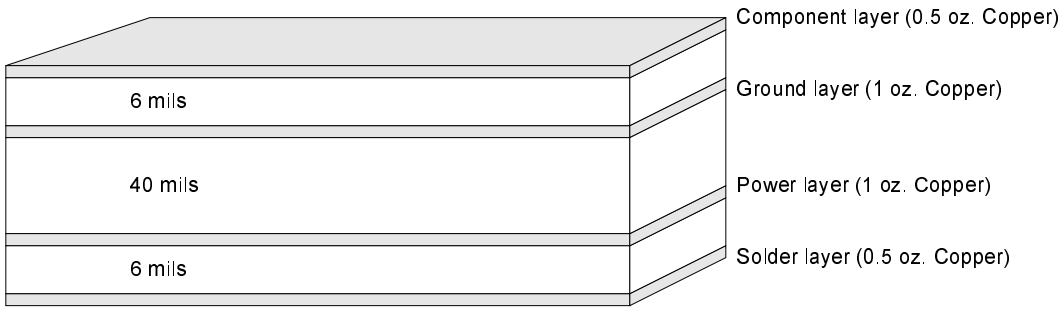


Figure 2-6. Four-Layer Stack-up with 2 Signal Layers and 2 Power Planes

2.2.2.2 Six-Layer Board

Figure 2-7 illustrates an example of a six-layer stack-up with 4 signal layers and 2 power planes. The layer sequence of component-ground-internal1-internal2-power-solder is the most common stack-up arrangement from top to bottom. It is recommended to place a 6-mil substrate between one signal layer and the power plane and also between the two internal layers. An 18-mil substrate must be placed between the power plane and the internal layer. Dielectric constant, E_r, should be 4.5 for all substrate materials.

In order to reduce crosstalk effects between layers, signal traces on the two internal layers should be orthogonal. Routing any signal trace on the power planes, either on the power layer or on the ground layer, is also not recommended on a six-layer board. As an exception, if a signal has been routed on the power layer, then it should be routed as short as possible. In any case, routing on the ground layer is not allowed. The impedance of all signal layers is to be in the range between 55 ohms and 75 ohms. Lower trace impedance providing better signal quality is preferred over higher trace impedance.

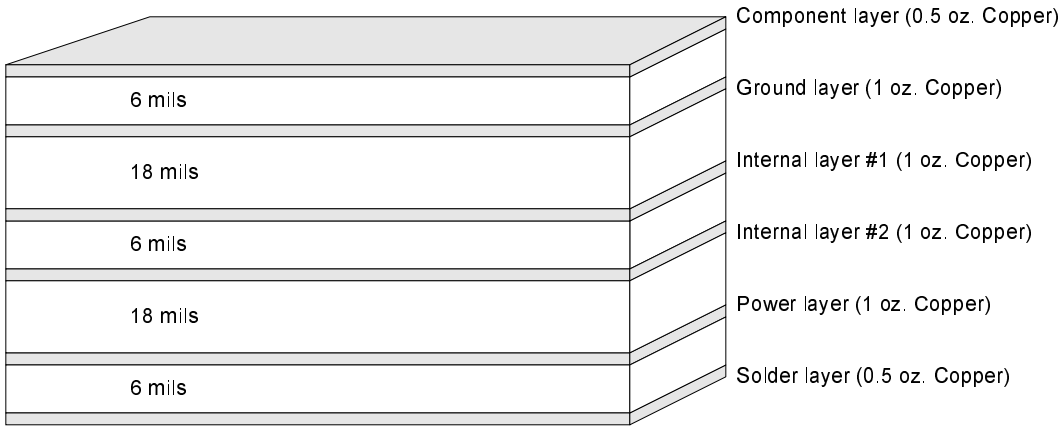


Figure 2-7. Six-Layer Stack-up with 4 Signal Layers and 2 Power Planes

2.2.3 Power Requirements

This section describes issues related to the power supply of a Socket-7 CPU and an Apollo MVP4 chipset. It is well known that appropriate decoupling capacitors are required to provide a stable power source to the CPU, the ASIC and all other components on a motherboard. Moreover, details about capacitor type and placement on a motherboard are also given.

2.2.3.1 Single Socket-7 Processor Capacitive Decoupling

Currently, the voltage range of a Socket-7 processor core voltage (VCC2) is between 2.1V and 3.3V. Local regulation of VCC2 is recommended. That is, a local DC-to-DC converter, placed as close to the CPU as possible, converts a higher voltage to a lower voltage using a linear or switching (preferred) regulator. The closer to the load the capacitor is placed, the more inductance is bypassed. Decoupling capacitors are required to provide a stable power source to a CPU on a motherboard. Usually, low ESR and low ESL capacitors are preferred for decoupling. Basically, there are two types of decoupling capacitors, Bulk Capacitors (greater than 10uF, Electrolytic or Tantalum) for preventing power supply droop and high frequency capacitors (less than 10uF, ceramic) for providing adequate decoupling. It is recommended to keep vias for decoupling capacitors (SMD type) as close to the capacitor pads as possible (see Figure 2-8).

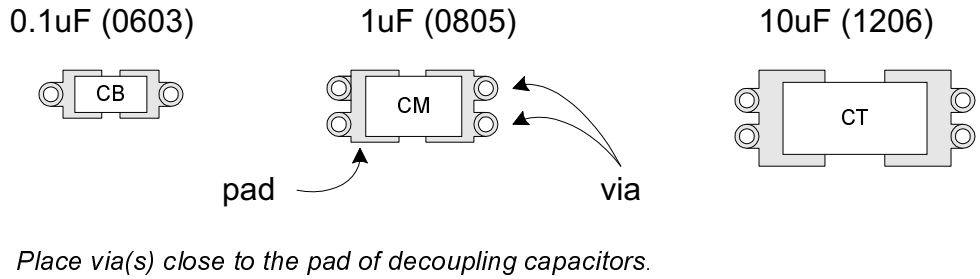


Figure 2-8. Example of Via Location

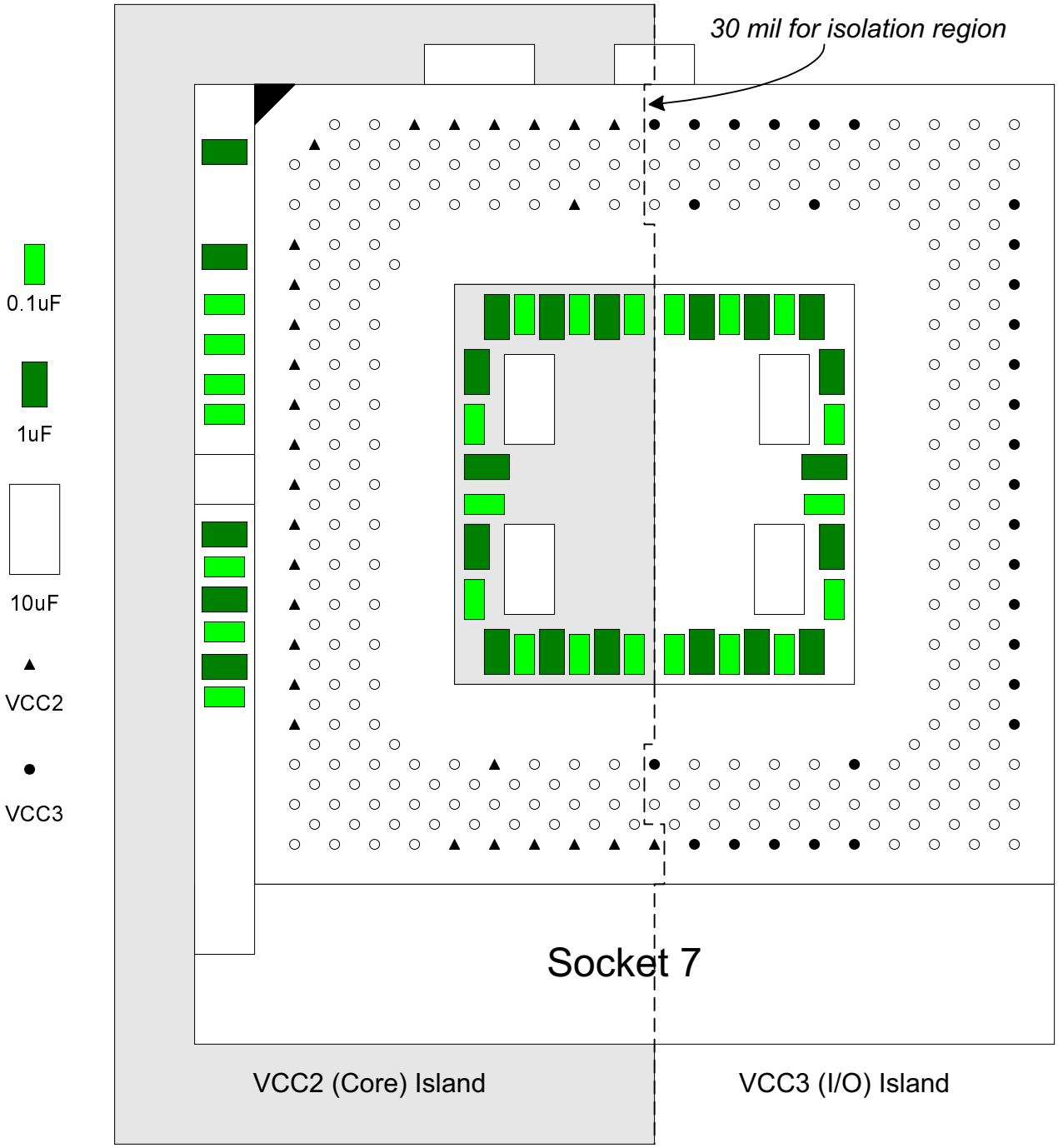


Figure 2-9. Decoupling Capacitor Placement for Single Socket 7 Processor

Figure 2-9 shows a suggested component placement for the decoupling capacitors for a Socket-7 CPU. The isolation region between the VCC2 (Core) island and VCC3 (I/O) island should be at least 30 mil wide. The high frequency decoupling capacitors (0.1uF and 1uF) should be located as close to the power and ground pins of the CPU as possible.

2.2.3.2 Apollo MVP4 Chipset Capacitive Decoupling

Decoupling capacitors for the VT8501 and VT82C686A are shown in Figure 2-10. It is recommended to place decoupling capacitors as close to the chips as possible and evenly distribute these capacitors around them. In most cases, the value of these decoupling capacitors is 1uF, but 0.1uF capacitors are also acceptable. Similarly, this kind of placement can apply on other ASIC chips, slots or sockets.

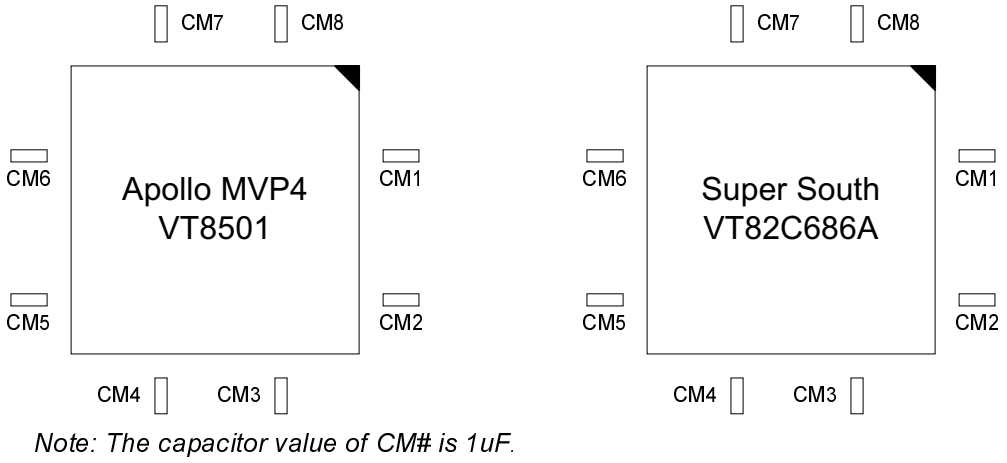


Figure 2-10. Decoupling Capacitor Placements for VT8501 and VT82C686A

2.2.3.3 Power Plane Partitions

The required voltage sources in an Apollo MVP4 system design are: +/-12V, +/-5V, CPU_CORE voltage, 3.3V and 2.5V. The power layer is partitioned into several power islands with four major power sources: **VCC2** (CPU_CORE voltage), **VCC3** (3.3V), **VCCI** (2.5 V North Bridge core voltage), and **VCC** (+5V). The remaining power sources will have their own small power islands or be routed as power traces 20-50 mil wide. Figure 2-11 shows the power plane partitions on a typical ATX form factor.

The island associated with VCC2 covers half the area of the PGA socket for the Socket-7 CPU. The VCC3 island covers an area which contains the other half of the CPU socket, the PBSRAM, the Tag RAM, the North Bridge chip, the South Bridge chip and all DIMM slots. The rest of the power layer belongs to VCC. Different power plane partitions for Micro-ATX and Baby-AT form factors are shown in Figure 2-12 and Figure 2-13 respectively. The distribution of power islands is almost the same between ATX and Micro-ATX, except for the smaller VCC island on the power layer of the Micro-ATX.

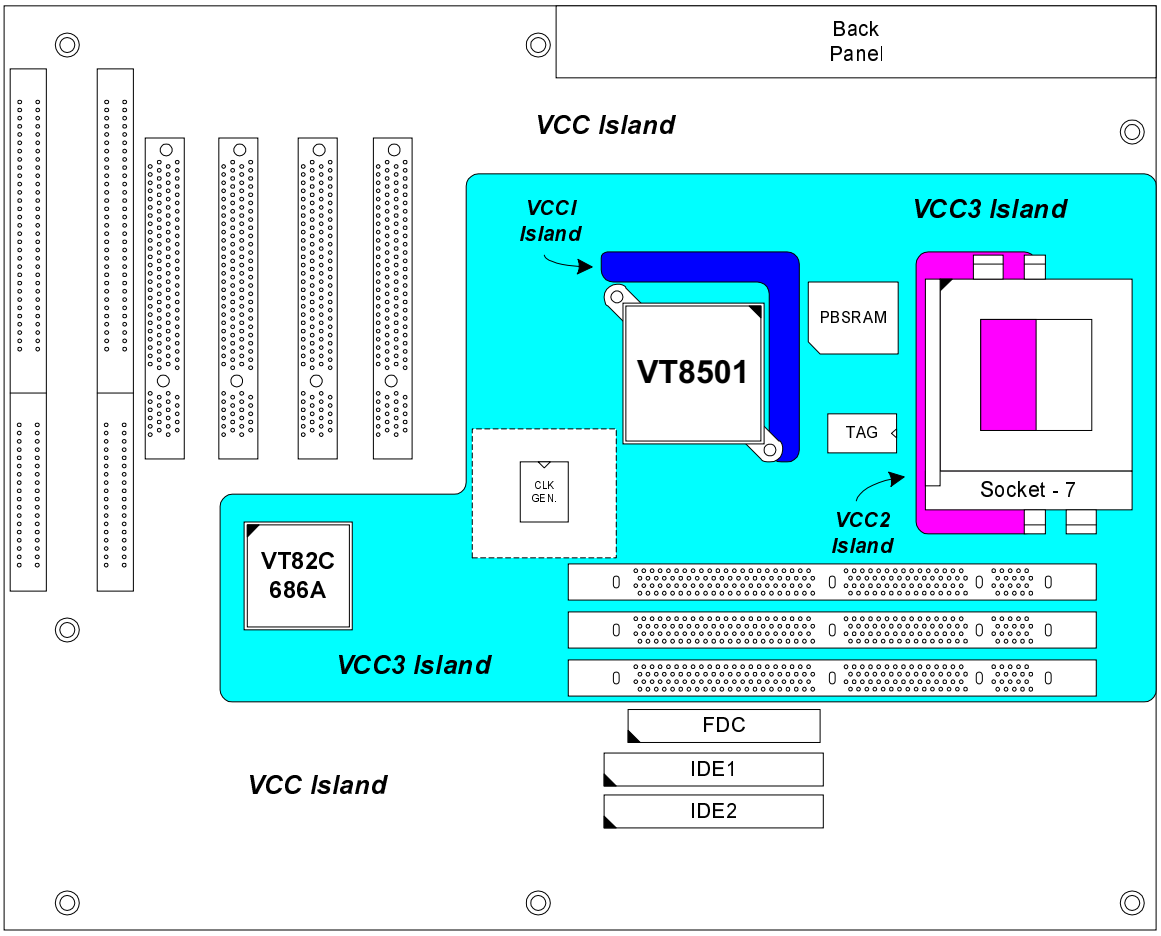


Figure 2-11. Power Plane Partitions for ATX

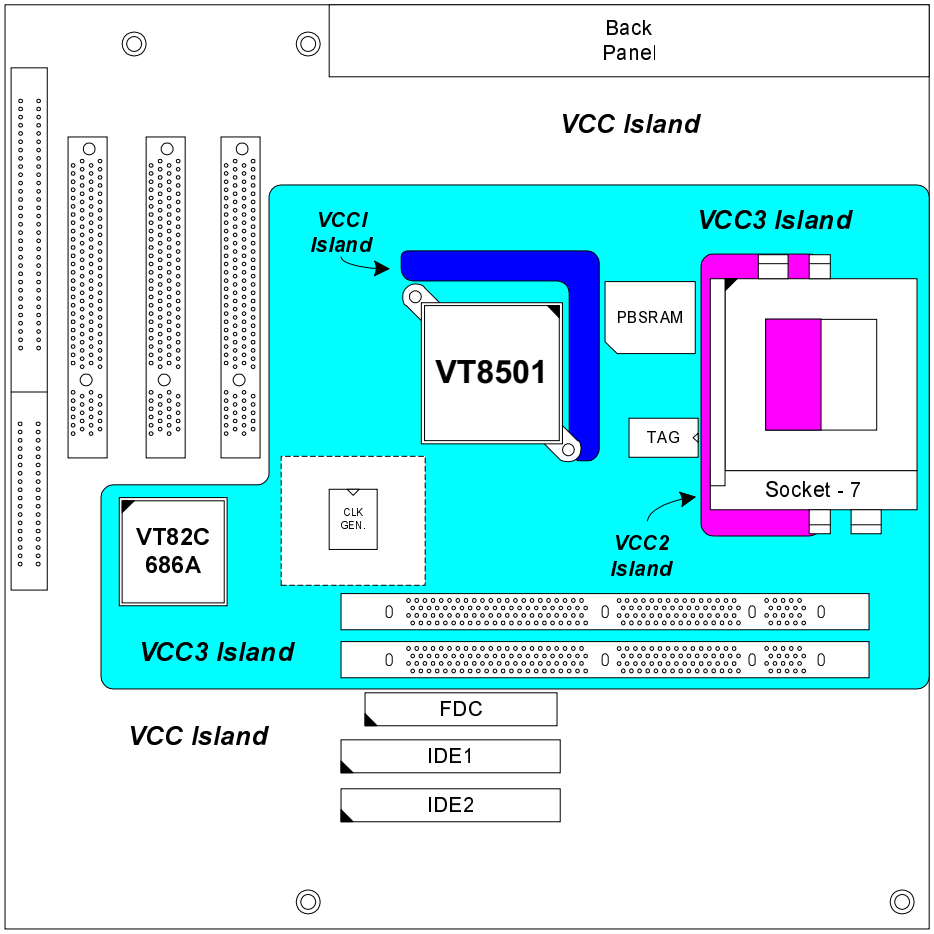


Figure 2-12. Power Plane Partitions for Micro-ATX

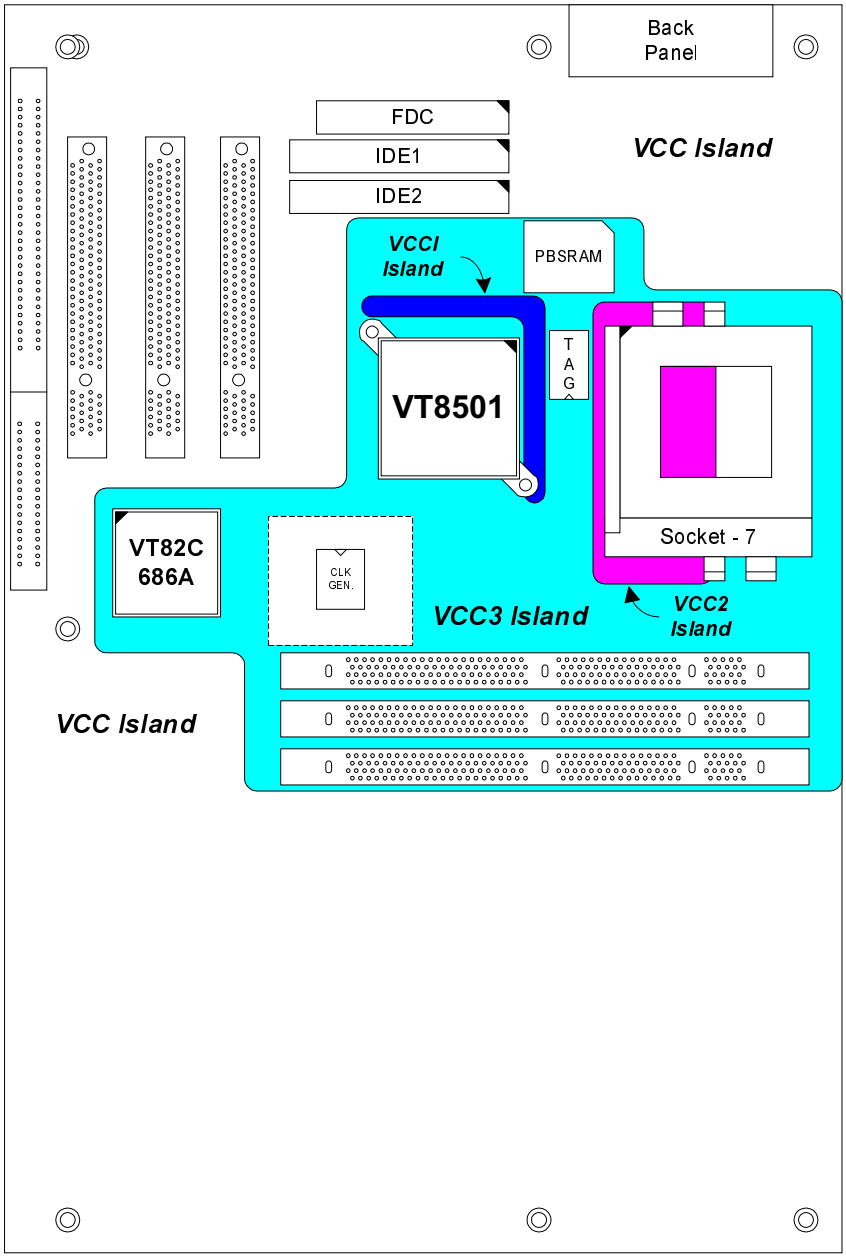


Figure 2-13. Power Plane Partitions for Baby-AT

2.2.3.4 Chipset Power and Ground Recommendations

This section shows the recommended layout of the power plane and the ground plane on each layer for the two BGA chips of the VIA chipset (VT8501 and VT82C686A). Appropriate power and ground distribution for component, ground, power and solder layers can provide a better power and ground circuit to the chip. Power and ground layout examples for both VT8501 and VT82C686A are shown in Figures 2-14 and 2-15 respectively.

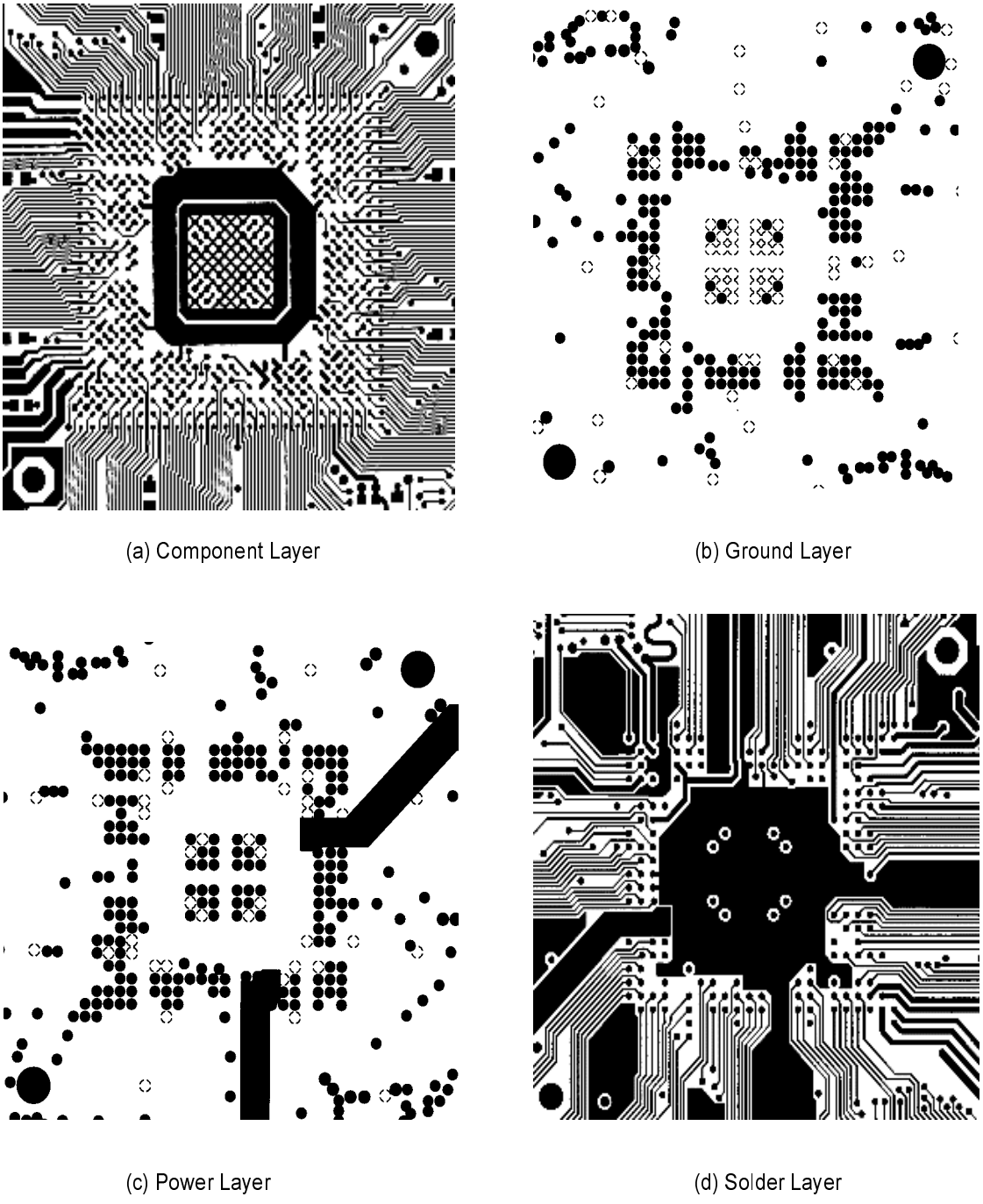


Figure 2-14. VT8501 Power and Ground Layout

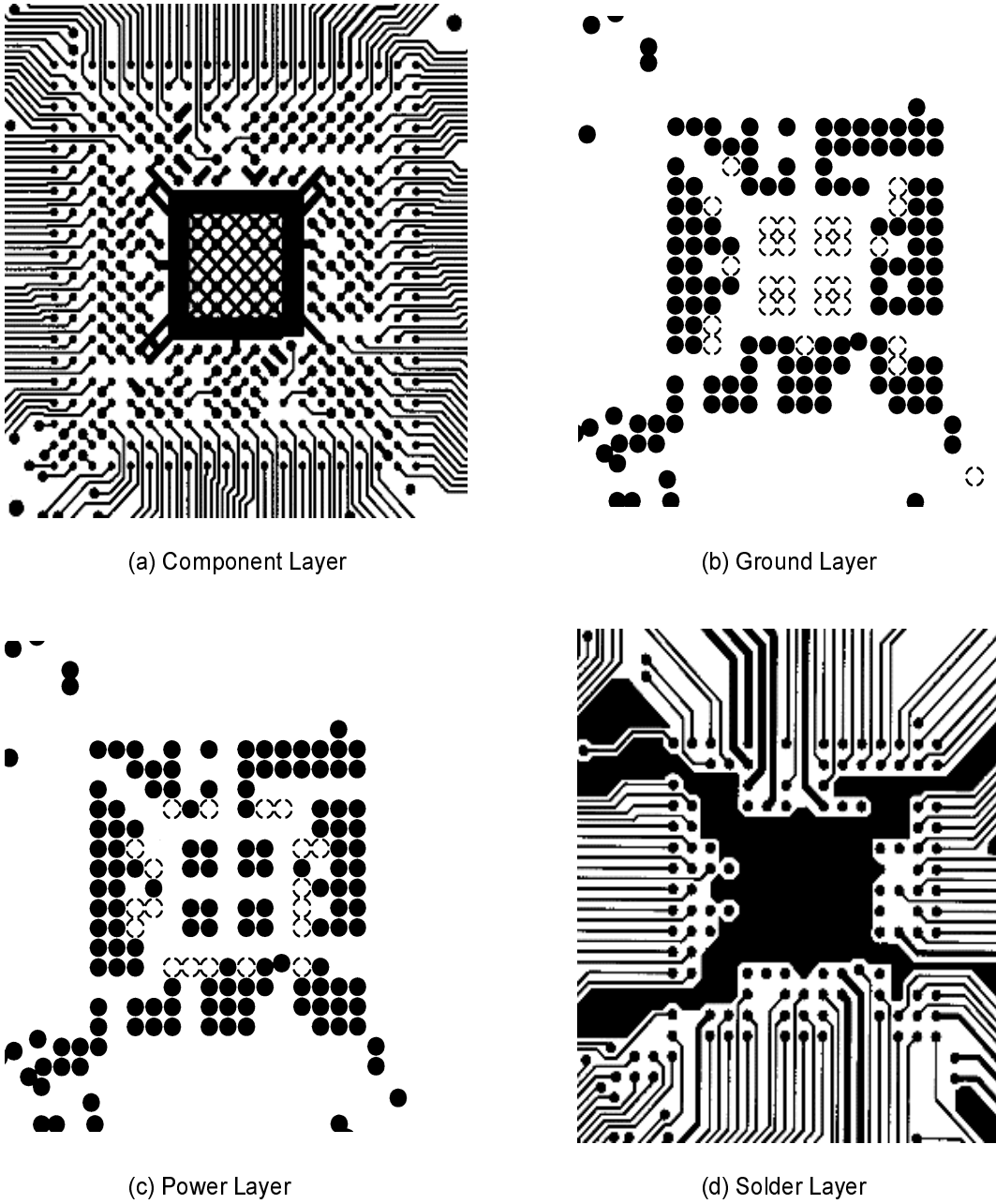


Figure 2-15. VT82C686A Power and Ground Layout

2.2.4 Power Up Configuration

During system reset and power up, the information of the system configuration is latched at the rising edge of the RESET# signal. Internal configuration registers of Apollo MVP4 digital core logic are based on the status of memory address lines MA[13:0]. These memory address signals may be pulled up or pulled down with external resistors to determine the configurations. If the default configuration setting is acceptable, no external pulled down resistors are necessary because all Apollo MVP4 North Bridge MA bus pins have been internally pull down on their I/O buffers. Please refer to Table 2-2 for the power up configuration of MA signals.

Table 2-2. Power-Up Configuration for VT8501

Pin Name	Pin #	Strapping Description	Note
MA[13:12]	AF25, AE25	Ratio Selection of CPU External Frequency to PCI Frequency **00** : Auto detect **01** : 3x (100MHz) **10** : 2x (66MHz) **11** : Illegal selection	
MA11	AE26	SERR Pin Function Selection: **0** = SERR, **1** = Power Good	
MA[10:9]	AD25, AD26	North Bridge Clock Delay: **00** = 0 units, **01** = 1 unit, **10** = 2 units, **11** = 3 units	
MA8, MA2	AC24 , AB26	Graphics (GFX) Power on Strapping **00** : Normal operation GFX memory clock <= N2GMCLK (NB to GFX memory clock output) GFX video clock <= GFX PLL1 output GFX LCD clock <= GFX PLL2 output **01** : Graphic standalone simulation mode GFX memory clock <= pin XTLI GFX video clock <= pin IMIIN GFX LCD clock <= pin IMIIN **1x** : NB + Graphic simulation mode GFX memory clock <= N2GMCLK (NB to GFX memory clock output) GFX video clock <= pin IMIIN GFX LCD clock <= pin IMIIN	Note 1
MA7	AC25	Graphic Test Mode: **0** = Normal Mode, **1** = Graphics Test Mode	
MA6	AC26	LCD On/Off selection: **0** = Disable, **1** = Enable LCD Panel Function	
MA[5:3]	AB23, AB24, AB25	Flat Panel Type Selection **000** : TFT 1024x768-18 **001** : TFT 1280x1024-18+18 **010** : TFT 800x600-18 **011** : TFT 1024x600-18 **100** : DSTN 1024x768-16 **101** : DSTN 1024x600-24 **110** : DSTN 800x600-16 **111** : DSTN 1024x768-24	Note 2
MA[1:0]	AA23, AA24	Graphic Clock Delay: **00** = 0 unit, **01** = 1 unit, **10** = 2 units, **11** = 3 units	

Notes:

1. *Graphics Memory Clock (MCLK): Most of the logic inside the graphics core is referenced to this clock. It controls the VGA, 2D, 3D, DVD, and graphics data path logic.*
   Graphic Video Clock (VCLK): Video clock or pixel clock. Logic after the display FIFO to the CRT display signals is clocked by VCLK. Signals such as HSYNC and VSYNC are generated from VCLK.
   Normal operation (strappings of MA8 and MA2 are "00"): MCLK is provided by the VT8501 north bridge PLL, VCLK is provided by graphics controller PLL1 and LCDCLK is provided by graphics controller PLL2.
   Graphic Standalone simulation mode (strappings of MA8 and MA2 are "01"): MCLK is supplied externally from pin XTLI and VCLK and LCDCLK are supplied externally from pin IMIIN.
   NB + Graphic simulation mode (strappings of MA8 and MA2 are "10 or 11"): MCLK is provided by the VT8501 north bridge PLL and VCLK and LCDCLK are supplied externally from pin IMIIN.
2. *TFT 1024x768-18: panel timing is selected for TFT panels, the panel resolution is 1024 pixels x 768 pixels, and panel data is transferred over the 18-bit panel data bus (transferring a single pixel per clock).*

The logical state of these power-up strapping pins is determined as follows: each pin of the MA[13..0] bus has an internal pull-down. Even though it can be set to logical 0 without any pull-up or pull-down, the existence of an external pull-down will insure that the correct configuration is detected. By setting a 3-pin jumper as shown in Figure 2-16, a state of logical 1 or logical 0 can be selected (the internal pull-down resistors are weak so that they will not affect normal operation of the MA signals).

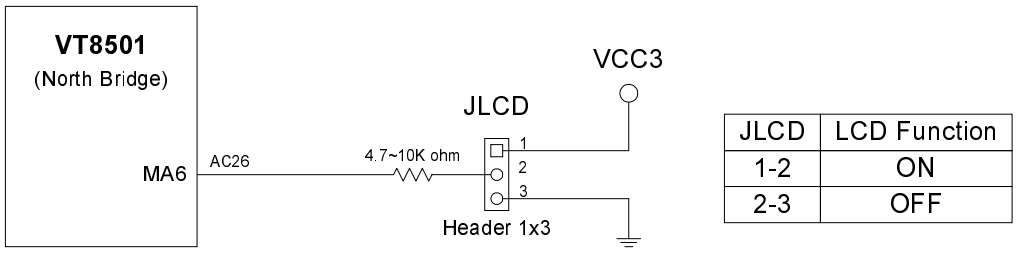


Figure 2-16. A Typical Example of a 3-pin Jumper Strapping Circuit

The power up configuration for the VT82C686A South Bridge is shown in Table 2-3 below. The strapping of SPKR (pin V5 of the VT82C686A) is sampled during reset to determine the usage of the Secondary Disk Data (SDD) pins. When connecting the SPKR signal to a speaker, the strapping circuit of SPKR is slightly different from the regular strapping circuit. Two application circuits for SPKR strapping are shown in Appendix F.

Table 2-3. Power-Up Configuration for VT82C686A

Signal Name	Pin #	Strapping Description	Note
SPKR	V5	Selection for Secondary IDE data bus or Audio/GAME function. 1 = Audio/GAME (Audio/Game uses SDD bus and SA[15:0] can also function as SDD bus). 0 = Secondary IDE data bus (Primary IDE and Secondary IDE have their own data buses).	
ROMCS#	C1	Selection of Socket-7 configuration or Slot-1 configuration. 1 = Slot-1 for Pentium II or Socket-370 (also called “Socket-9”) for Celeron 0 = Socket-7	

2.3 General Layout and Routing Guidelines

This section provides general layout rules and routing guidelines for designing Apollo MVP4 motherboards.

For most signal traces on an Apollo MVP4 motherboard layout, 6-mil trace width and 9-mil spacing are advised. To reduce trace inductance, minimum power trace width is set at 30 mils. As a quick reference, recommended trace width and spacing for different trace types are listed in Table 2-4.

Table 2-4. Recommended Trace Width and Spacing

Trace Type	Trace Width (mils)	Spacing (mils)
Signal	6 or wider	9 or wider
Clock	15 or wider	15 or wider
Power	30 or wider	20 or wider

In high-speed bus design, general rules for minimizing crosstalk are listed below:

- Maximize the distance between traces. Maintain a minimum 9 mils space between traces wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Select a board stack-up that minimizes coupling between adjacent traces.
- The trace impedance of all signals should be lower than 65 ohms.

2.3.1 Apollo MVP4 Clock Layout Recommendations

The requirements of the system clock synthesizer for an Apollo MVP4 based system design are listed in Table 2-5.

Table 2-5. Apollo MVP4 Clock Synthesizer Requirements

Clock Signal Type	Frequency (MHz)	Quantity	Connections
CPU Clock	66/75/83/95/100/124	4	Connect to CPU (1), Apollo MVP4 (1) and L2 Cache (2)
SDRAM Clock	66/100	13	Connect to three SDRAM slots (12) and Apollo MVP4 (1)
SDRAM Clock In	66/100	1	Connect to Apollo MVP4 (1)
PCI Clock	30/33	6	Connect to Apollo MVP4 (1), Super South (1), and PCI slots (4)
USB Clock	48	1	Connect to Super South (1)
Super I/O Clock	24	1	Connect to Super I/O (1) if an external Super I/O is used
Reference Clock	14.31818	2	Connect to Super South (1) and ISA slots (1)

Note: The voltage level for all clock signals is 3.3V.

The 13 (66 / 100MHz) SDRAM clocks are generated from a clock buffer inside the system clock synthesizer. They are controlled by the SDRAM clock output (MCLKO) provided by the Apollo MVP4 North Bridge. The VT8501 (North Bridge) has built-in de-skew Phase Lock Loop (PLL) circuitry for optimal skew control within and between clocking regions. For more details, refer to Figure 2-17.

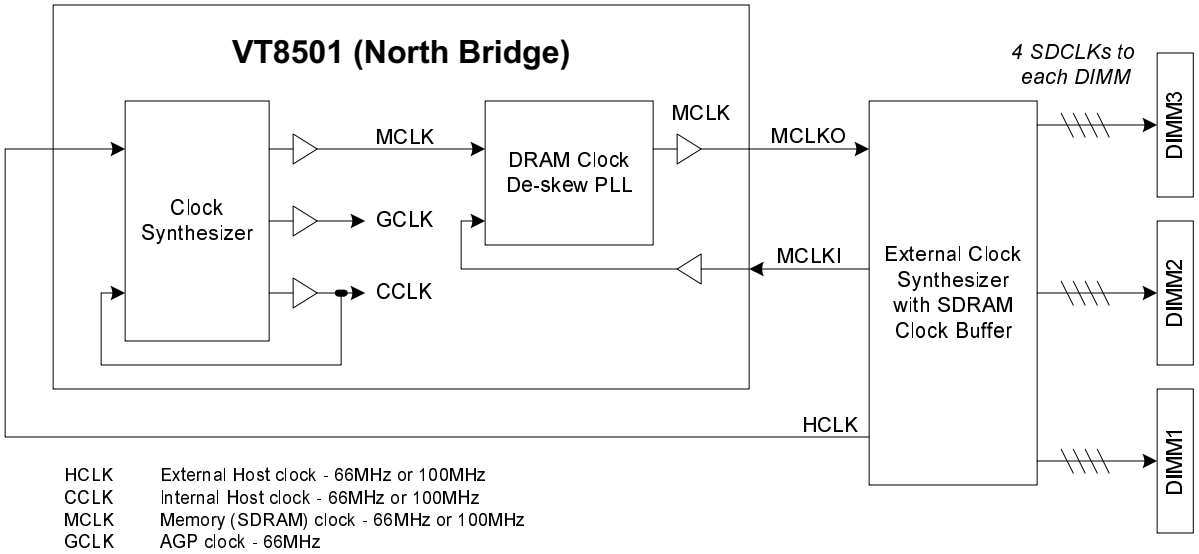


Figure 2-17. Apollo MVP4 Chip Clocking Scheme

2.3.1.1 Clock Routing Considerations

Clock routing guidelines are listed below:

- The recommended range of a clock trace width is between 15 mils and 20 mils.
- The minimum space between one clock trace and adjacent clock traces is 15 mils. The minimum space from one segment of a clock trace to other segments of the same clock trace is two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling (see Figure 2-18).
- Clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane (see Figure 2-19).
- Series terminations (damping resistors) are needed for all clock signals (typically 10 ohms to 33 ohms). When two loads are driven by one clock signal, the series termination layout is shown in Figure 2-20. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20 mils to 50 mils) is preferred.
- No clock traces on the internal layer if a six-layer board is used.

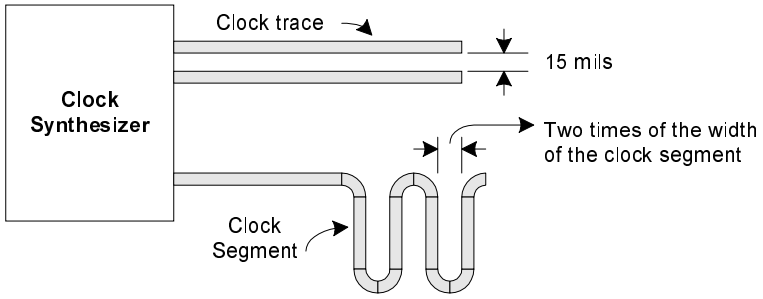


Figure 2-18. Clock Trace Spacing Guidelines

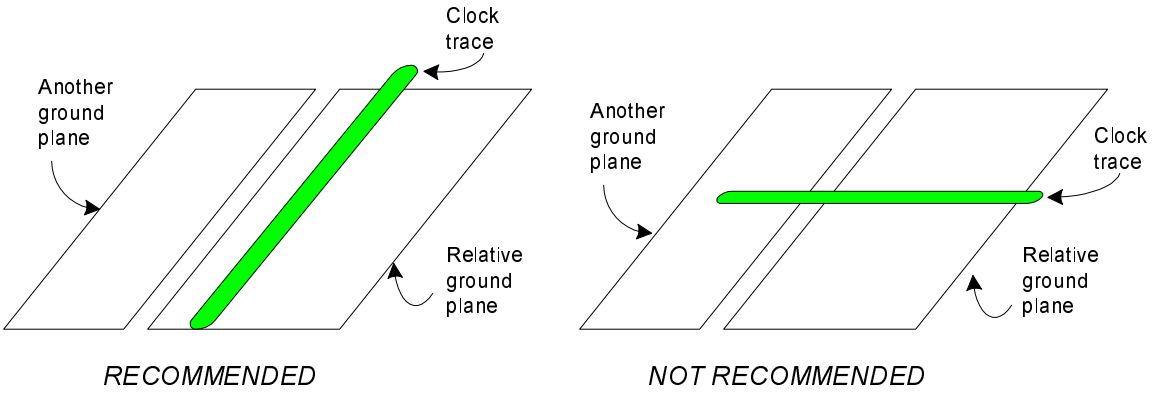


Figure 2-19. Effect of Ground Plane to a Clock Signal

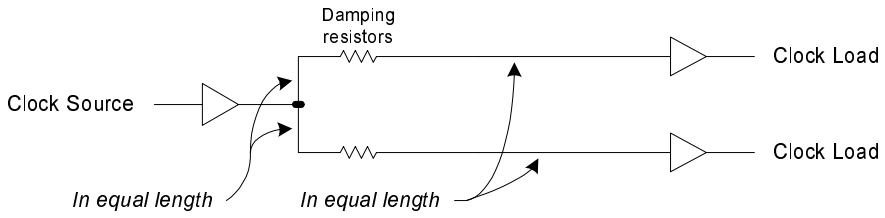


Figure 2-20. Series Termination for Multiple Clock Loads

2.3.1.2 Host CPU Clock and SDRAM Clock Signals

The layout recommendations of the host clocks and SDRAM clocks are shown in Figure 2-21. 22 ohm and 10 ohm series terminations are recommended for all host clocks and all SDRAM clocks respectively. It is also recommended that bypass capacitors be added to all clock signals on the clock synthesizer side. Different values of series terminations and bypass capacitors are needed for a better clock transmission and alignment on the final PCB layout. In other words, it is best to observe the actual clock waveform and experimentally determine the optimal values for series termination and bypass capacitors. For clock alignment considerations, trace lengths of all clocks should match the longest one.

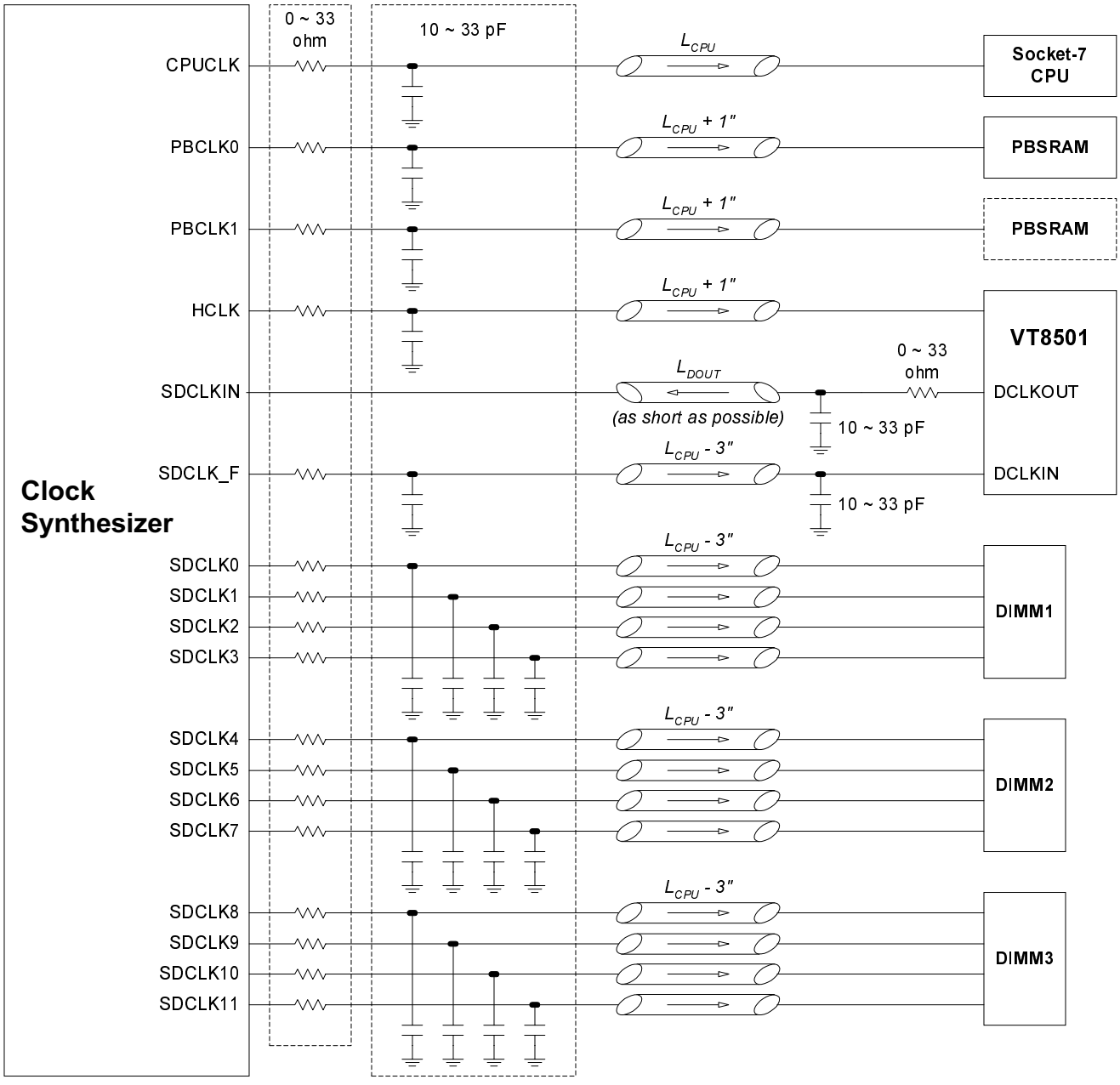


Figure 2-21. Host Clock and SDRAM Clock Layout Recommendations

2.3.1.3 PCI Clock Signals

Layout recommendations for the PCI clocks are shown in Figure 2-22. 22 ohm series terminations are recommended for all PCI clocks. A typical 22 pF bypass capacitor is also required for each PCI clock. Depending on how the system is designed, the value of the bypass capacitors for the PCI clocks may vary. For clock alignment considerations, trace lengths of all PCI clocks should match the longest one.

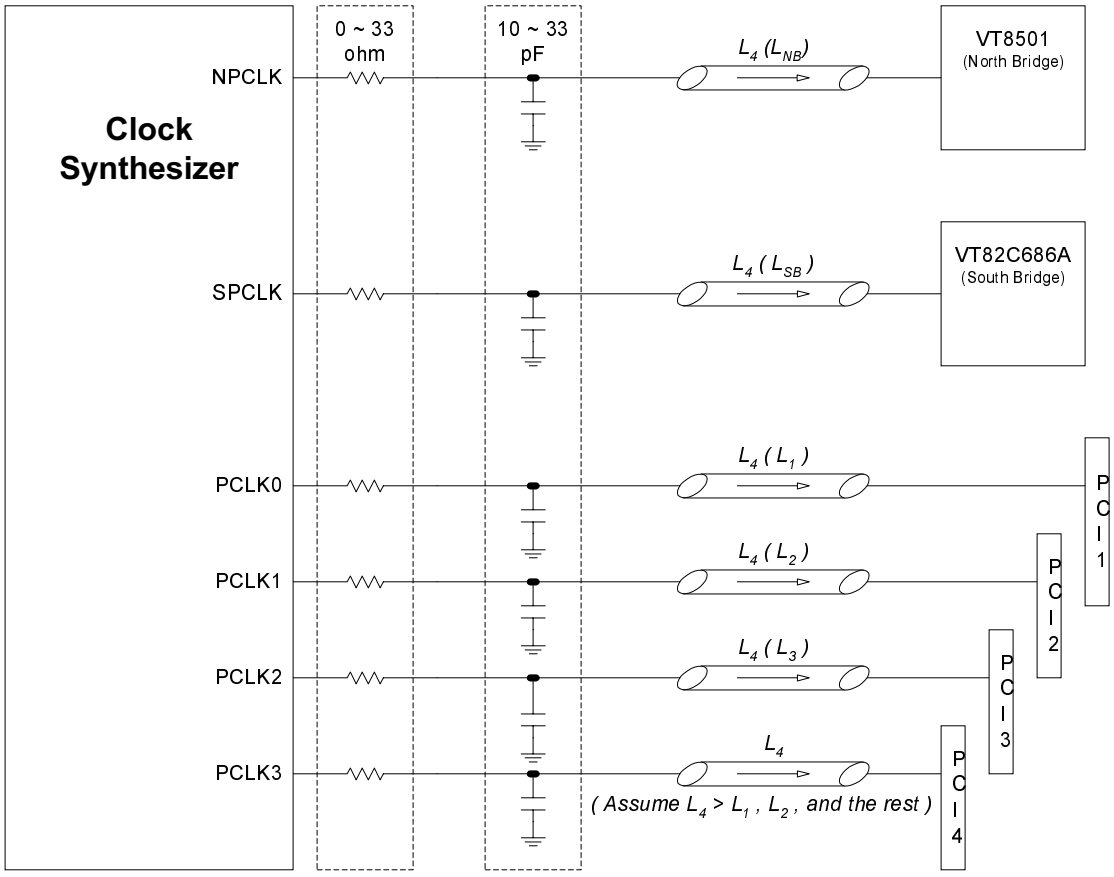


Figure 2-22. PCI Clock Layout Recommendations

2.3.1.4 Miscellaneous Clock Signals

22 ohm series terminations are recommended for clock signals such as the USB clock (48 MHz), Super I/O clock (typically 24 MHz) and reference clock (14.31818 MHZ) which are generated from the system clock synthesizer.

22 ohm series terminations are also needed for clock signals such as the LCD shift clock (SHFCLK, 32.5 or 65 MHz), Video Capture clock (VIDCLK, typically 27MHz), and TV clock (TVCLK, 27~44MHZ), generated from the VT8501 North Bridge. The highest frequency the VT8501 can provide for SHFCLK is 108 MHz.

The trace width for the clocks above should be at least 15 mils. To reduce crosstalk impact, trace spacing between these clocks and other signals should be maintained at a minimum of 15 mils.

2.3.1.5 Clock Trace Length Calculation

CPU Clock Trace Length Calculation

Before routing any other signals on the board, pre-route every CPU clock trace from the system clock synthesizer to the CPU (CPUCLK), North Bridge (HCLK), and PBSRAM(s) (PBCLK0 or PBCLK1) as short as possible. All high frequency clock alignment will be on the basis of the longest one (usually CPUCLK). A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → CPU	L_{CPU}	**L_{CPU}**	-	4"~9"
Clock chip → VT8501 (NB)	L_{NB}	**L_{CPU} + 1"**	0.5"	3"~9"
Clock chip → PBSRAM	L_{PB}	**L_{CPU} + 1"**	0.5"	3"~9"

SDRAM Clock Trace Length Calculation

Pre-route SDRAM clock traces (SDCLK0~SDCLK11) from the system clock synthesizer to the DIMM slots as short as possible. The length of all SDRAM clocks will be based on the longest one (L_{SD}). The length of MCLKI (L_{DIN}) should be the same as that of the SDCLKs. The MCLKO clock trace should be as short as possible. A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → SDCLK[11:0]	L_{SD} (assume < L_{CPU})	**L_{CPU} - 3"**	0.5"	3"~5"
MCLKI (Clock chip → NB)	L_{DIN}	**L_{CPU} - 3"**	0.5"	3"~5"
MCLKO (NB → Clock chip)	L_{DOUT}	**L_{DOUT}**	-	2"~5"

PCI Clock Trace Length Calculation

Pre-route PCI clock traces from the system clock synthesizer to the VT8501 (NPCLK) and VT82C686A (SPCLK) as short as possible. Then pre-route PCI clock traces PCLK0~PCLK3 from the system clock synthesizer to all PCI slots as short as possible. The length of these clocks will be based on the longest one. A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → VT8501 (NB)	L_{NB}	**L_4 + 2.5"**	0.5"	5"~14.5"
Clock chip → VT82C686A (SB)	L_{SB}	**L_4 + 2.5"**	0.5"	5"~14.5"
Clock chip → PCI1	L_1	**L_4**	0.5"	5"~12"
Clock chip → PCI2	L_2	**L_4**	0.5"	5"~12"
Clock chip → PCI3	L_3	**L_4**	0.5"	5"~12"
Clock chip → PCI4	L_4 (> the others)	**L_4**	-	5"~12"

Notes:

1. *Shortest length means the minimum routable trace length between both clock ends.*
2. *Desired length means the real length of the clock traces on PCB layout.*
3. *Allowable difference means the maximum difference between clock traces of the same type.*
4. *Allowable range means the acceptable clock length range for the specific clock.*
5. *The location of the system clock chip can affect the length of all clock traces. To optimize the clock alignment, place the clock chip at an appropriate location.*
6. *In addition, the trace impedance of all clock traces should be lower than 55 ohms.*

2.3.2 Routing Styles and Topology

High-speed bus signals are sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. In order to maintain better signal quality, transmission stubs should be kept under 1.5 inches. Therefore, daisy chain style routing is strongly recommended for these signals. Figure 2-23 below shows an example of a daisy chain routing.

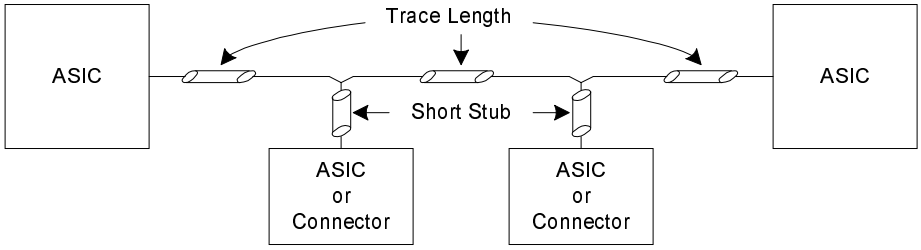


Figure 2-23. Daisy Chain Routing Example

Topology is the physical connectivity of a net or a group of nets. Basically, there are two types of topologies for a motherboard layout: point-to-point and multi-drop. An example of these topologies is shown in Figure 2-24.

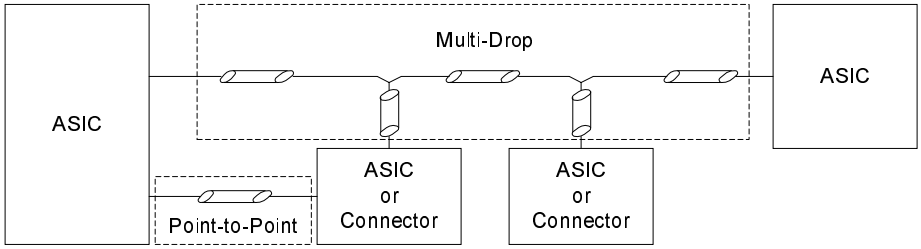


Figure 2-24. Point-to-Point and Multi-Drop Topology Examples

If daisy chain routing is not allowed in some circumstances, different routings may be considered. An alternative topology is shown in Figure 2-25. The branch point in this case is somewhere between both ends. It may be near the source or near the loads. Being close to the load side is best. The separated traces should be equal length.

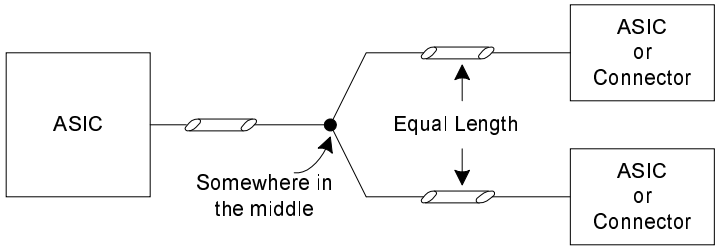


Figure 2-25. Alternate Multi-Drop Topology Example

2.3.3 Host Interface Layout and Routing Guidelines

The host address bus and host data bus are typical multi-drop buses. Except for the byte enable signals, most host control signals are point-to-point connections between CPU and North Bridge. For multi-drop connections, daisy chain routing style is strongly preferred from a transmission line effect point of view. Recommended layout guidelines and routing examples for each bus and control signal with one PBSRAM chip are given in the following sections (see Section 2.3.4 for the two-PBSRAM-chip case).

2.3.3.1 Host Address Bus

The recommended routing for the host address bus is to place the CPU and the Apollo MVP4 North Bridge at both ends of the daisy chain. This daisy chain topology includes CPU, Tag RAM, L2 Cache Pipelined Burst Synchronous RAM (PBSRAM) and VT8501 (North Bridge) as shown in Figure 2-26 below.

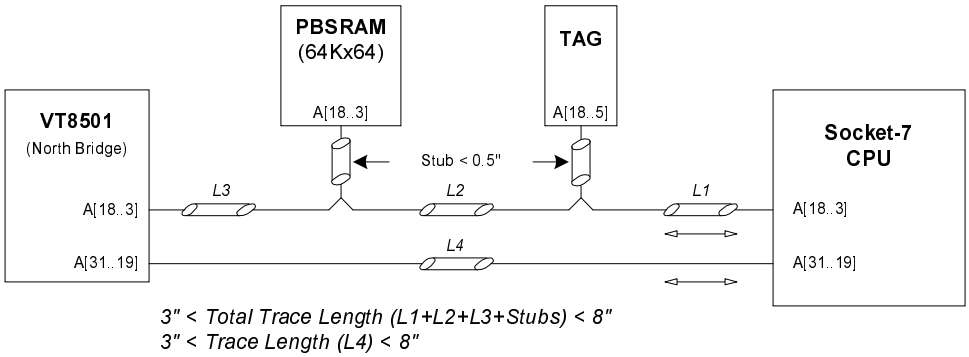


Figure 2-26. Host Address Bus Topology Example

2.3.3.2 Host Data Bus

The recommended routing for the host data bus is to place the CPU and the Apollo MVP4 North Bridge at both ends of the daisy chain. This daisy chain topology includes CPU, L2 Cache PBSRAM, and VT8501 as shown in Figure 2-27 below.

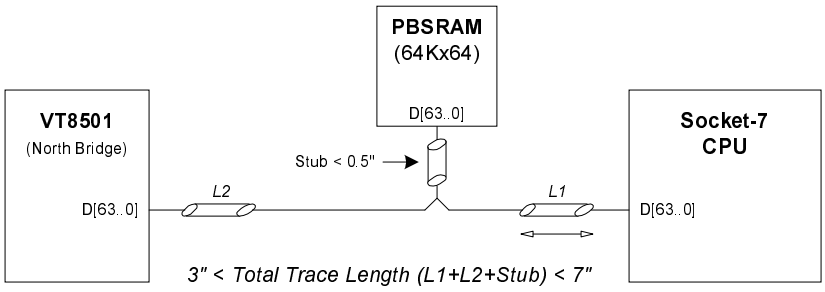


Figure 2-27. Recommended Example of Host Data Bus Topology

2.3.3.3 Host Control Signals

The only multi-drop group of host control signals is BE[7..0]. All remaining host control signals from the VT8501 North Bridge, PBSRAM, or South Bridge may be routed point-to-point. A brief description of each control signal is listed in Table 2-6.

Table 2-6. Host Control Signals

North Bridge -- L2 PBSRAM -- CPU		
Signal Name	**I/O**	**Description**
BE[7..0]	IO	Byte Enable
North Bridge -- CPU		
Signal Name	**I/O**	**Description**
ADS#	IO	Address Strobe
AHOLD	O	Address Hold
BOFF#	O	Back Off
BRDY#	IO	Bus Ready
CACHE#	I	Cacheable Indicator
D/C#	IO	Data / Control Indicator
EADS#	O	External Address Strobe
KEN#	O	Cache Enable / Invalidate
HITM#	I	Hit Modified
HLOCK#	I	Host Lock
M/IO#	IO	Memory / IO In Indicator
NA#	O	Next Address Indicator
SMIACT#	I	System Management Interrupt Active
W/R#	IO	Write / Read Command Indicator
L2 PBSRAM -- CPU		
Signal Name	**I/O**	**Description**
ADSC#	I	Address Strobe Copy
North Bridge -- Tag RAM		
Signal Name	**I/O**	**Description**
TA[7..0]	IO	Tag Address
TWE#	O	Tag Write Enable
North Bridge -- L2 PBSRAM		
Signal Name	**I/O**	**Description**
CADS#	O	Cache Address Strobe
CADV#	O	Cache Advance
COE#	O	Cache Output Enable
CCS#	O	Cache Chip Select
GWE#	O	Global Write Enable
BWE#	O	Byte Write Enable
South Bridge -- CPU		
Signal Name	**I/O**	**Description**
CPURST	OD	CPU Reset
INTR	OD	CPU Interrupt
NMI	OD	Non-Maskable Interrupt
INIT	OD	Initialization
STPCLK#	OD	Stop Clock
SMI#	OD	System Management Interrupt
FERR#	I	Numerical Coprocessor Error
IGNNE#	OD	Ignore Numerical Error
A20M#	OD	A20 Mask

In the following sections, a layout example is given for each of the six cases above (NB-L2-CPU, NB-CPU, L2-CPU, L2-NB, Tag-NB, and SB-CPU). Routing guidelines are also provided.

North Bridge - L2 PBSRAM - CPU

A recommended layout example for host multi-drop control signals BE[7..0] is shown in Figure 2-28.

- It is recommended that the PBSRAM be placed between the North Bridge and the CPU.
- The traces for signals BE[7..0] should be a minimum of 6 mils in width and a minimum of 9 mils in spacing. The total length should be limited to be under 7 inches.

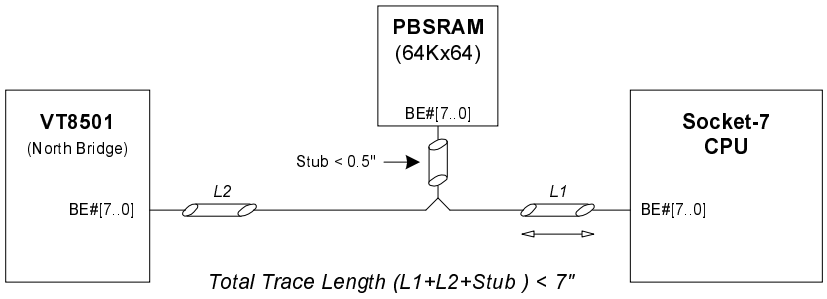


Figure 2-28. Layout Example of Host Multi-Drop Control Signals BE[7..0]

CPU to Apollo MVP4 North Bridge

The Point-to-point connection for host control signals between the VT8501 and the CPU is illustrated in Figure 2-29.

- Signals ADS#, M/IO#, W/R#, CACHE#, LOCK# are strongly recommended to be routed as short as possible. The trace width of those signals should be at least 6 mils wide. The trace length of those signals should be limited to be under 6 inches.
- Traces for the other signals should be at least 6 mils wide and at most 6 inches long.

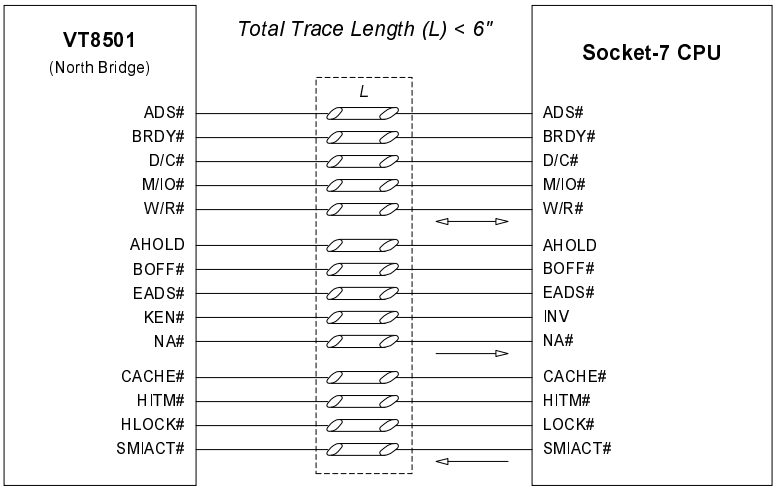


Figure 2-29. Layout Example of Host Control Signals from North Bridge to CPU

L2 Pipelined Burst Synchronous RAM to CPU

A recommended layout example for signal ADSP# between the PBSRAM and the CPU is shown in Figure 2-30.

- The trace for ADSP# of PBSRAM should be a minimum of 6 mils in width and a maximum of 6 inches in length for the single PBSRAM case (see section 2.3.4 for the dual PBSRAM case).

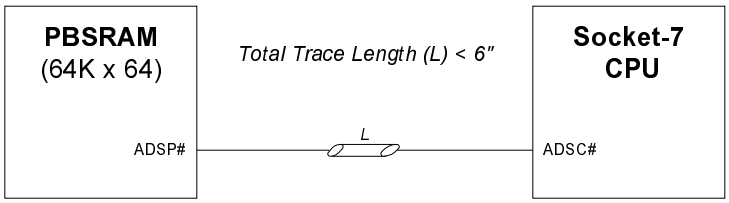


Figure 2-30. Layout Examples of Host Control Signal from PBSRAM to CPU

The Cache Control interface is between a North Bridge, a Tag RAM and one or two PBSRAM chips. All Tag RAM signals are point-to-point connections. The control signals of the PBSRAM could be point-to-point connections or multi-drop connections depending on whether one PBSRAM or two PBSRAM chips are used in the system design.

North Bridge to Tag RAM

The only point-to-point signals to the Tag RAM are the address bus TA[7..0]. A layout example for TA[7..0] and TWE# between the VT8501 North Bridge and the Tag RAM is shown in Figure 2-31. The requirement for running the Socket-7 host CPU bus at 100 MHz is to choose a Tag RAM with an access time less than 8 ns. Routing guidelines are listed below.

- The traces for signals TA[7..0] should be a minimum of 6 mils in width and a maximum of 2.5 inches in length.
- The trace for TWE# should also be a minimum of 6 mils in width and a maximum of 2.5 inches in length.

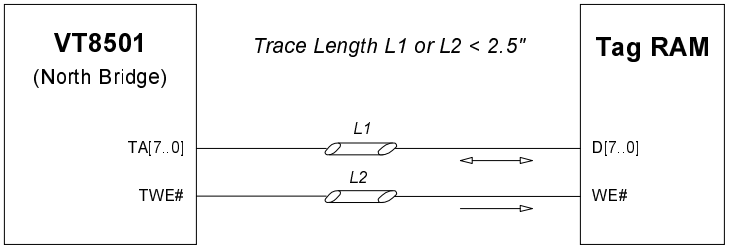


Figure 2-31. Layout Example of Tag RAM signals from North Bridge

North Bridge to PBSRAM

PBSRAM control signals CADS#, CADV#, BWE#, GWE#, COE# and CCS# may be routed point-to-point from the VT8501 (North Bridge) to the PBSRAM. One layout example is shown in Figure 2-32. Routing at a 100 MHz bus frequency requires a PBSRAM with an access time less than 8 ns. Routing guidelines are listed below:

- Signal traces should be a minimum of 6 mils in width and a minimum of 9 mils between traces for the single PBSRAM case (see section 2.3.4 for the dual PBSRAM case). The maximum length of these traces should be less than 4 inches.

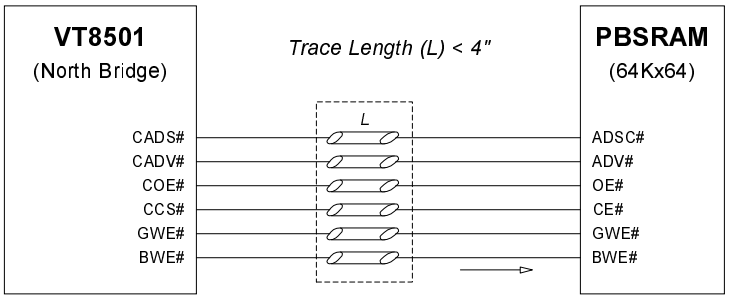


Figure 2-32. Layout Example of One PBSRAM Chip

South Bridge to CPU

A layout example of VT82C686A (South Bridge) control signals to the CPU is shown in Figure 2-33.

- Each south bridge Open Drain (OD) output control signal to the CPU needs a 4.7K ohm pull-up which should be placed as close to the VT82C686A chip as possible.
- A minimum of 6 mils in width and a minimum of 9 mils in spacing is sufficient for good signal quality.
- No specific limitation of the trace length for these control signals is required.

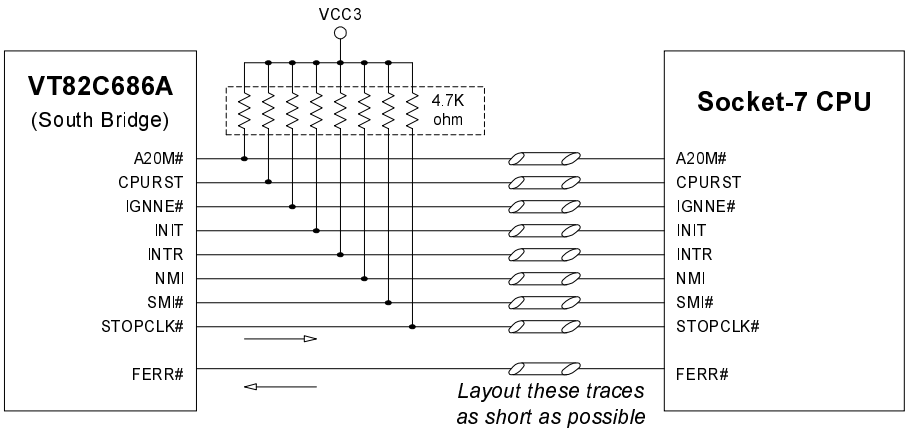


Figure 2-33. Layout Example of Control Signal from South Bridge to CPU

2.3.4 1MB L2 Cache Placement and Layout Guidelines

Placement and routing examples and layout guidelines for 1MB L2 cache (two 64Kx64 PBSRAM chips) are discussed in this section since the previous section only described the single-PBSRAM-chip case. For an Apollo MVP4 PC motherboard design, proposed placements and signal routings of the three most popular form factors (ATX, micro-ATX and Baby AT) are shown in following figures 2-34, 2-35, and 2-36. Detailed layout guidelines and signal routing are also addressed.

2.3.4.1 Placement and Routing for 1MB L2 Cache

Component placement and signal routing examples for ATX, Micro-ATX and Baby-AT form factors are shown in Figures 2-34, 2-35 and 2-36. The major components on the board are the single Socket-7 CPU, PCI slots (four or three), ISA slots (two or one), three DIMM slots, and two PBSRAM chips. These placement and routing examples are provided as a reference only. The placement should be re-evaluated if a different combination of PCI and ISA slots and other motherboard peripherals is desired.

Each figure shows a full size of its respective form factor. The empty area at the bottom of each placement figure can be eliminated to reduce board size. Table 2-7 shows the full size and the suggested compact size for each form factor.

Table 2-7. Different Board Size Lists for Two PBSRAM Chips

Form Factor Type	Full size	Compact Size	Specification
ATX	12" x 9.6" (30.5cm x 24.5cm)	12" x 7.8" (30.5cm x 20cm)	4 PCI, 2 ISA, 3 DIMM, 2 PBSRAM
Micro-ATX	9.6" x 9.6" (24.5cm x 24.5cm)	9.6" x 9.5" (24.5cm x 22cm)	3 PCI, 1 ISA, 3 DIMM, 2 PBSRAM
Baby-AT	8.7" x 13" (22cm x 33cm)	8.7" x 10.2" (22cm x 26cm)	3 PCI, 1 ISA, 3 DIMM, 2 PBSRAM

In addition, power partitions on the power layer for each form factor are similar to Figures 2-11, 2-12 and 2-13.

ATX with two PBSRAM Chips

A proposed component placement and signal group routing for an Apollo MVP4 ATX form factor system with two PBSRAM chips is illustrated in Figure 2-34. The major components on the board are the single Socket-7 CPU, four PCI slots, two ISA slots and three DIMM slots. This figure shows an ATX motherboard placement as a reference only. The placement might need to be different if a different combination of PCI and ISA slots and other motherboard peripherals is desired.

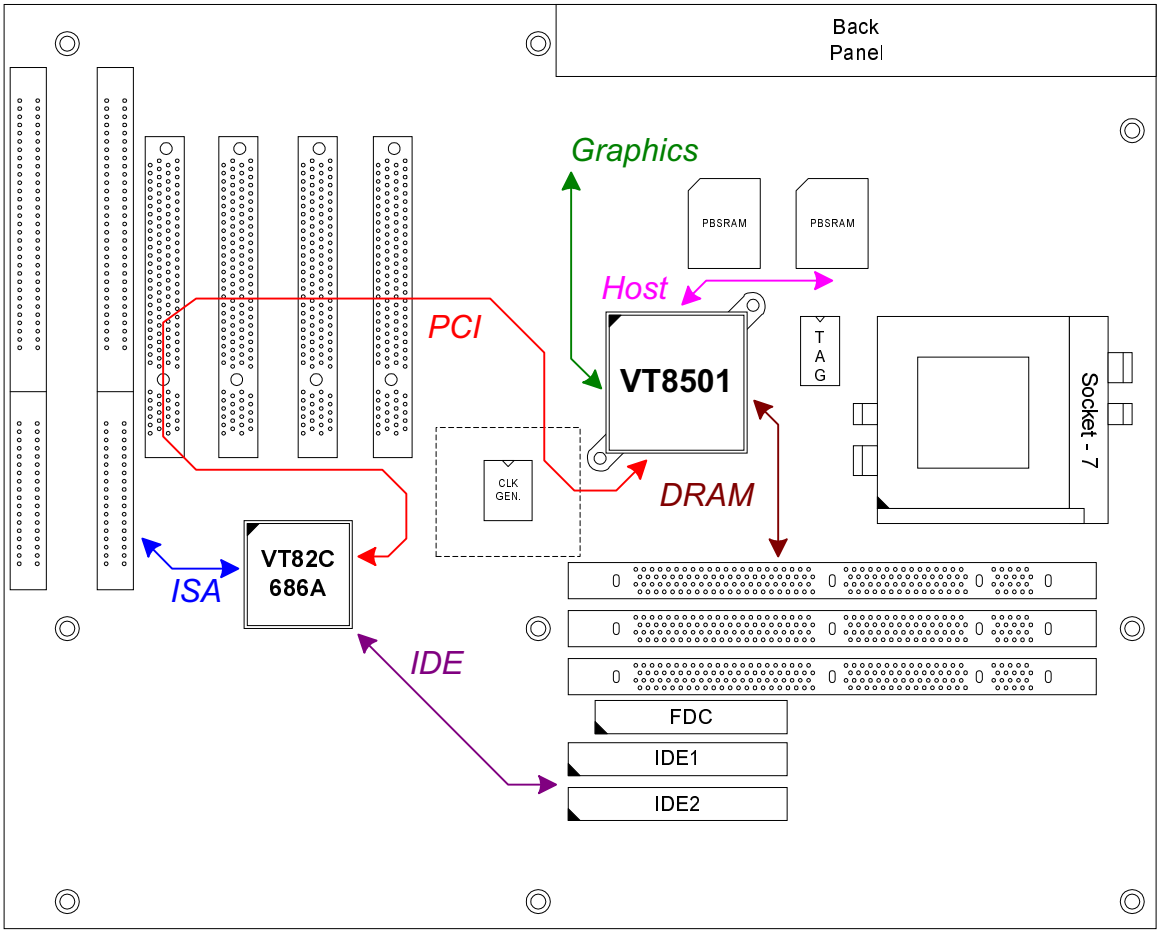


Figure 2-34. ATX Placement and Routing Example for Two PBSRAM Chips

Micro-ATX with two PBSRAM Chips

A proposed component placement and signal group routing for an Apollo MVP4 micro-ATX system design with two PBSRAM chips is illustrated in Figure 2-35. The major components on the board are the single Socket-7 CPU, three PCI slots, one ISA slot and three DIMM slots. This figure shows a reference only micro-ATX motherboard placement. The placement should be re-evaluated if a different combination of PCI and ISA slots and other motherboard peripherals is desired.

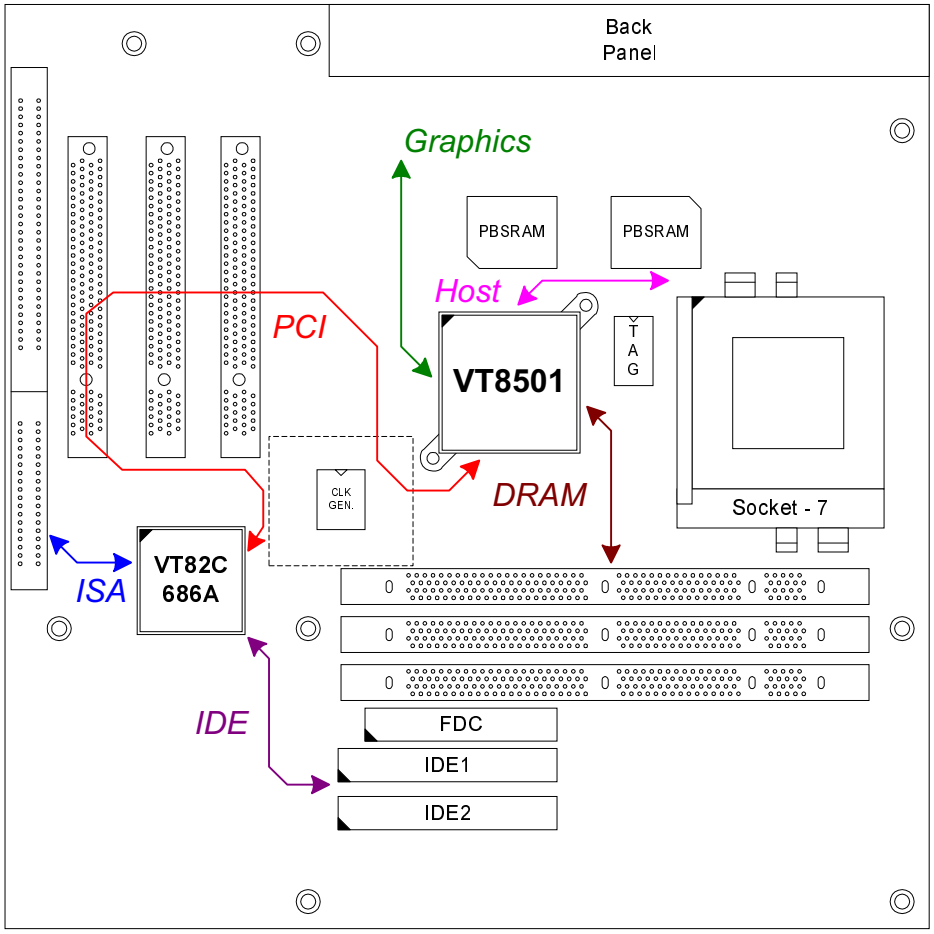


Figure 2-35. Micro-ATX Placement and Routing Example for Two PBSRAM Chips

Baby-AT with two PBSRAM Chips

Figure 2-36 illustrates a proposed component placement and signal group routing for an Apollo MVP4 Baby-AT form factor system design with two PBSRAM chips. The major component combination is the same as that of the Micro-ATX form factor above. A reference example of the Baby-AT motherboard placement is shown in this figure. The placement displayed should be re-evaluated if a different slot combination is chosen.

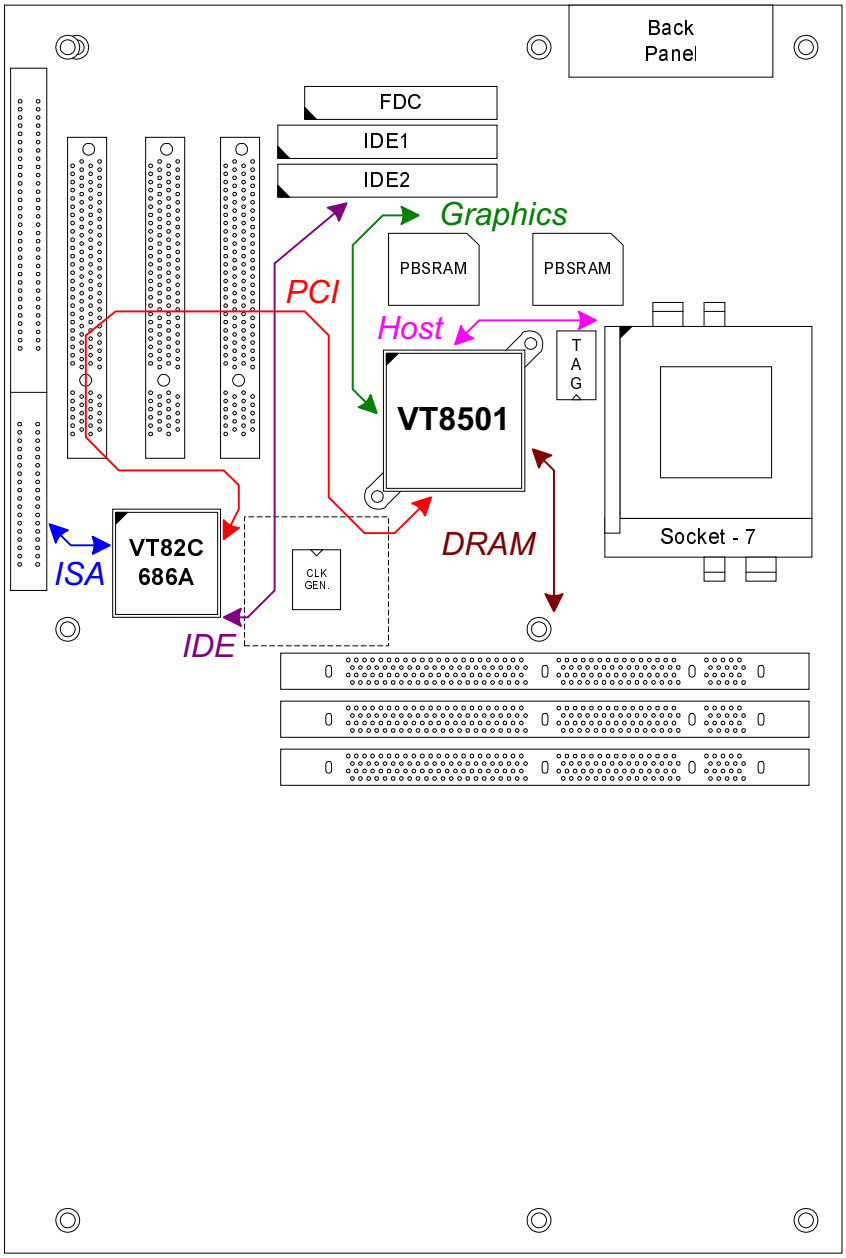


Figure 2-36. Baby-AT Placement and Routing Example for Two PBSRAM Chips

2.3.4.2 1MB L2 Cache Layout Rules

The L2 Cache system has two interfaces: Host interface and Cache Control interface. The host interface between CPU and two PBSRAM chips contains only one connection type. Host address bus, host data bus and byte enable signals are typical multi-drop connections. A daisy chain style of the routing is also strongly preferred for multi-drop connection even if two PBSRAM chips are used. The Cache Control interface between the VT8501 North Bridge and the two PBSRAM chips also uses multi-drop connection in daisy chain style.

Recommended layout guidelines and routing examples for each bus and control signal are given in the following sections.

Host Address Bus

Recommended routing is to place the CPU and VT8501 (North Bridge) at both ends of the daisy chain. A daisy chain topology includes CPU, Tag RAM, two PBSRAM chips, and VT8501 routed as shown in figure 2-37 below.

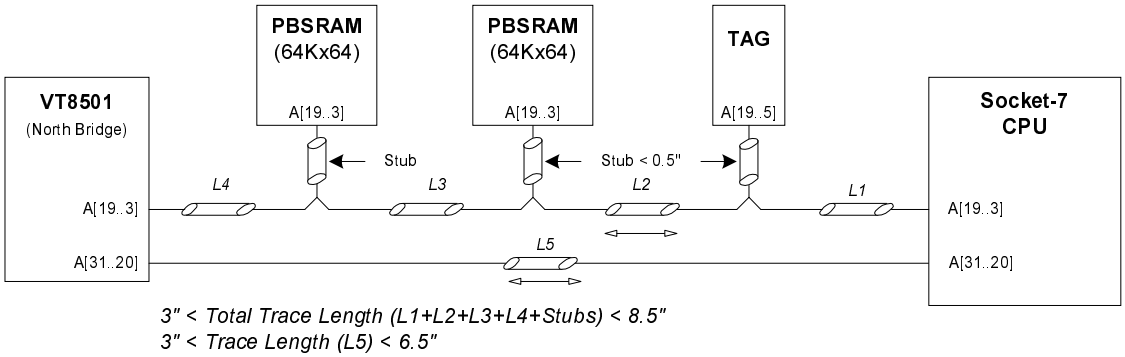


Figure 2-37. 1MB L2 Cache Host Address Bus Topology Example

Host Data Bus

The CPU, VT8501 (North Bridge), and two PBSRAM chips are connected to the host data bus. Similarly to the address bus, placing the CPU and the VT8501 at both ends of the daisy chain is recommended as shown in figure 2-38 below.

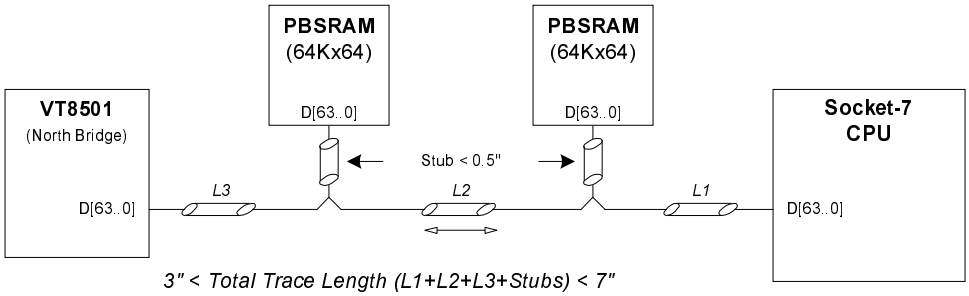


Figure 2-38. 1MB L2 Cache Host Data Bus Topology Example

Byte Enable Signals

A recommended layout example for host multi-drop control signals BE[7..0] is shown in Figure 2-39 below.

- It is recommended that the two PBSRAM chips be placed between the North Bridge and the CPU.
- The traces for BE[7..0]# should be a minimum of 6 mils in width and a minimum of 9 mils in spacing. The total length should be limited to be under 8 inches.

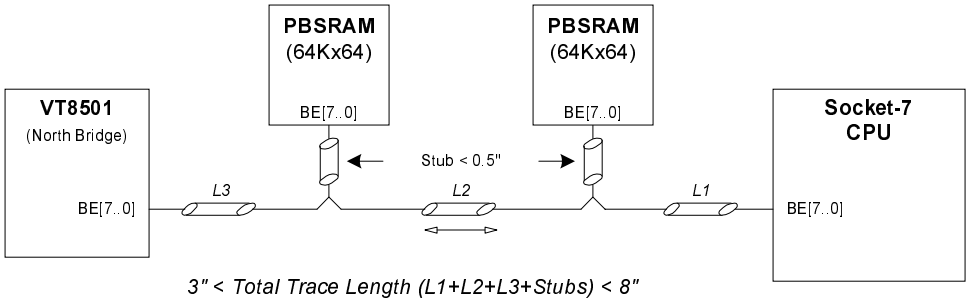


Figure 2-39. 1MB L2 Cache Host BE[7..0] Control Signal Topology Example

ADSP# Signal

A recommended layout example for signal ADSP# between the two PBSRAM chips and the CPU is shown in Figure 2-40 below.

- This signal trace should also be a minimum of 6 mils in width and a maximum of 8 inches in length when two PBSRAM chips are used.

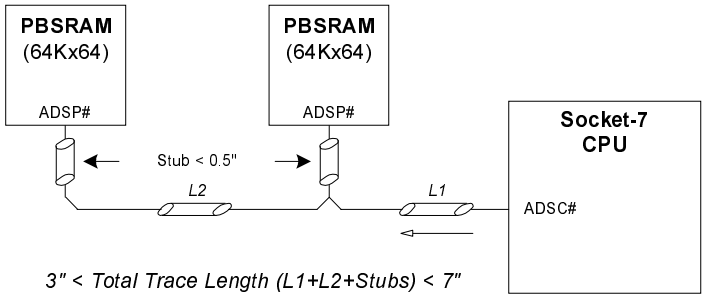


Figure 2-40. 1MB L2 Cache PBSRAM to Host CPU Control Signal Topology Example

Control Signals between VT8501 and Two PBSRAM Chips

Control signals CADS#, CADV#, BWE#, GWE#, COE# and CCS# connect the North Bridge to the two PBSRAM chips. One layout example for these control signals is shown in Figurer 2-41. Operating at a 100 MHz bus frequency requires choosing a PBSRAM with access time less than 8 ns. Routing guidelines are listed below.

- These signal traces should have the same trace attributes as previously mentioned (6 mil width / 9 mil space minimum) and a maximum of 4 inches in length for the double PBSRAM case.

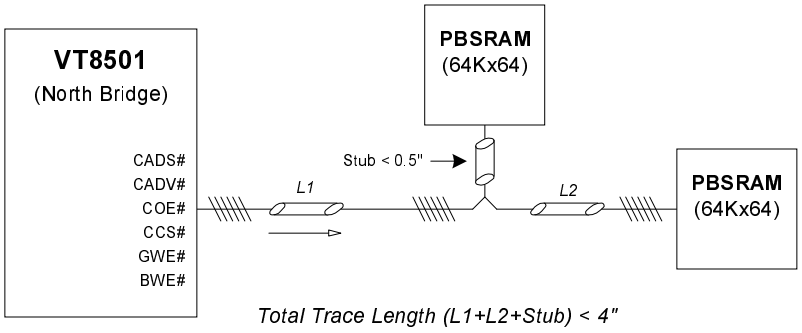


Figure 2-41. 1MB L2 Cache PBSRAM to North Bridge Control Signal Topology Example

2.3.5 Memory Subsystem Layout and Routing Guidelines

All DRAM signals are multi-drop connections. A brief description of the memory subsystem signals is provided in Table 2-8 below.

Table 2-8. Memory Subsystem Signals

North Bridge -- DRAM		
Signal Name	**I/O**	**Description**
MA[13..0]	O	Memory Address
MD[63..0]	IO	Memory Data
MECC[7..0]	IO	DRAM ECC or EC Data
RAS[5..0]#	O	Row Address Strobe of each bank
CAS[7..0]#	O	Column Address Strobe of each byte lane
SRASA# SRASB# SRASC#	O	Row Address Command Indicator
SCASA# SCASB# SCASC#	O	Column Address Command Indicator
SWEA# SWEB# SWEC#	O	Write Enable Command Indicator

The maximum DRAM installation is three DIMM slots. Two layout examples (Daisy Chain Ordering and Star Style) for all DRAM buses and control signals between the Apollo MVP4 North Bridge and the three DRAM DIMM slots is shown in Figure 2-42 and 2-43. The requirement to run at a 100 MHz frequency is to choose an SDRAM module with an access time less than 8 ns (i.e.,"PC100"). Routing recommendations are listed below.

- Traces for all DRAM signals should be a minimum of 6 mils in width and 9 mils in spacing.
- For daisy chain routing, traces of MA[13..0], MD[63..0], CAS[7..0]# and MECC[7..0] should be connected to DIMM modules in order of DIMM1, DIMM2, and DIMM3 (see figure 2-42). It is recommended to make both segments L2 and L3 as short as possible.
- For star style routing, traces of MA[13..0], MD[63..0], CAS[7..0]# and MECC[7..0] should be connected to DIMM2 first and then separated into two trace segments to DIMM1 and DIMM3 respectively (see figure 2-43). It is recommended to make both segments L1 and L3 equal length.
- Each trace for RAS[5..0]# should be separated into two traces with a serial damping resistor for each to the respective DIMM slots. For example, trace RAS0# is separated into two traces which are connected to DIMM1 with a serial damping resistor for each separate trace.

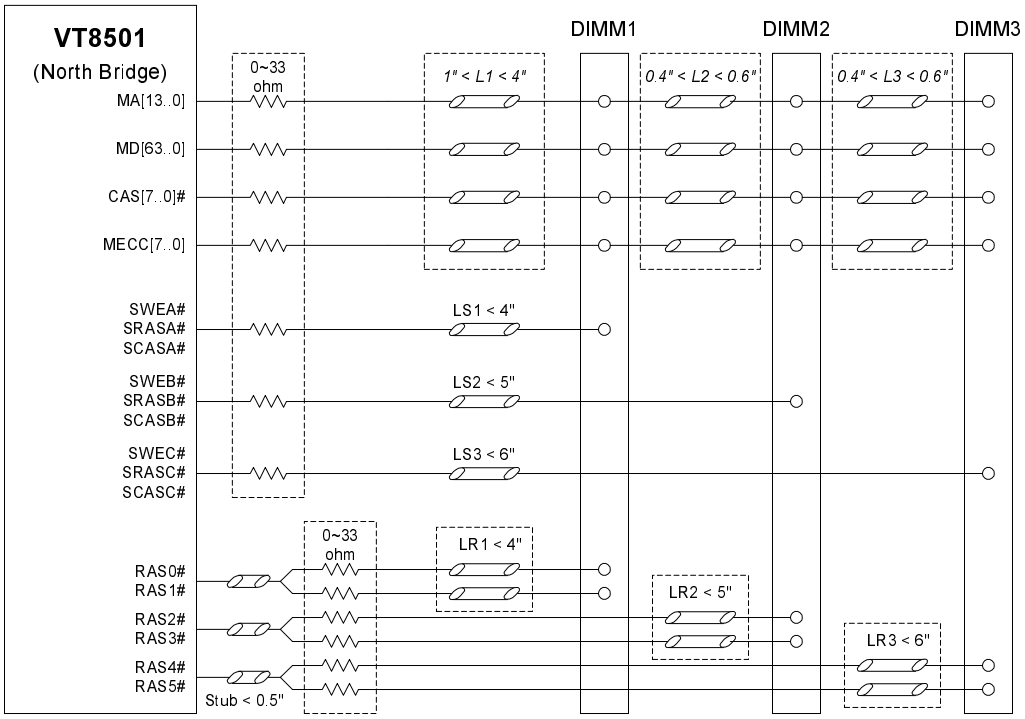


Figure 2-42. Daisy Chain Ordering Routings of Three-DRAM DIMM Slots

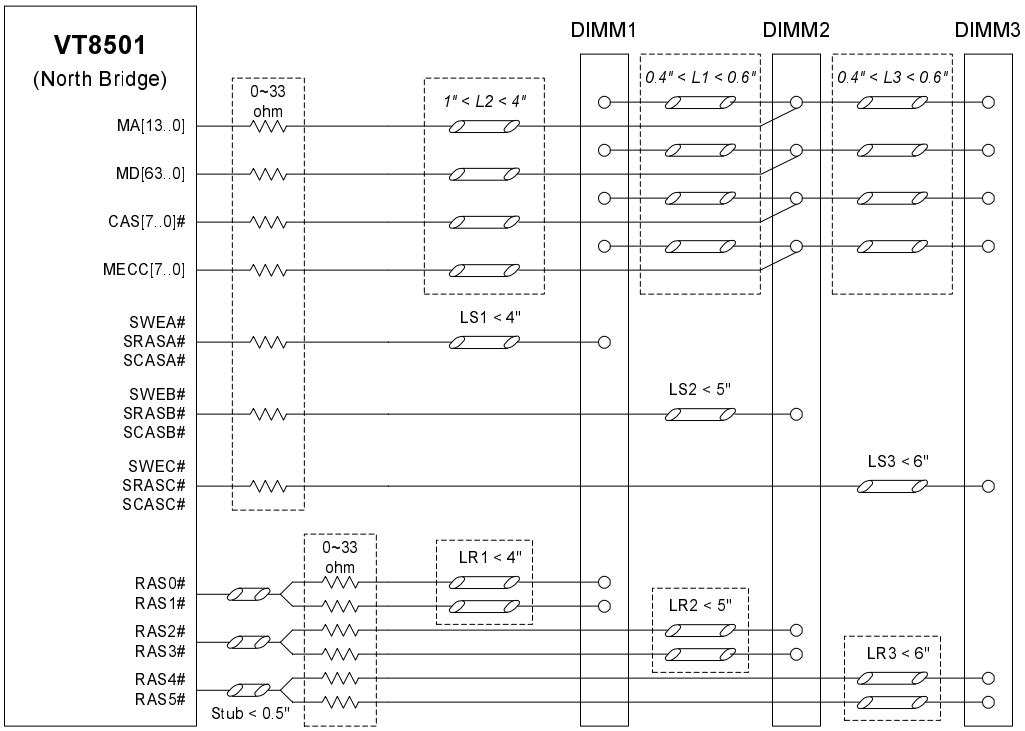


Figure 2-43. Star Style Routings of Three-DRAM DIMM Slots

Suspend to DRAM

A recommended schematic example of choosing Suspend to DRAM mode is shown in Figure 2-44. Only two SDRAM DIMM modules can be selected to implement Suspend to DRAM mode. If the Suspend to DRAM function is not implemented, nets CKE[5..0] of the DIMMs should be tied directly to VCC3 and all resistors (RA) on the left side should be removed. Signals RAS4#, RAS5#, SCASC# and SRASC# are swappable for CKE[3..0]. For example, RAS4# is not fixed for CKE0.

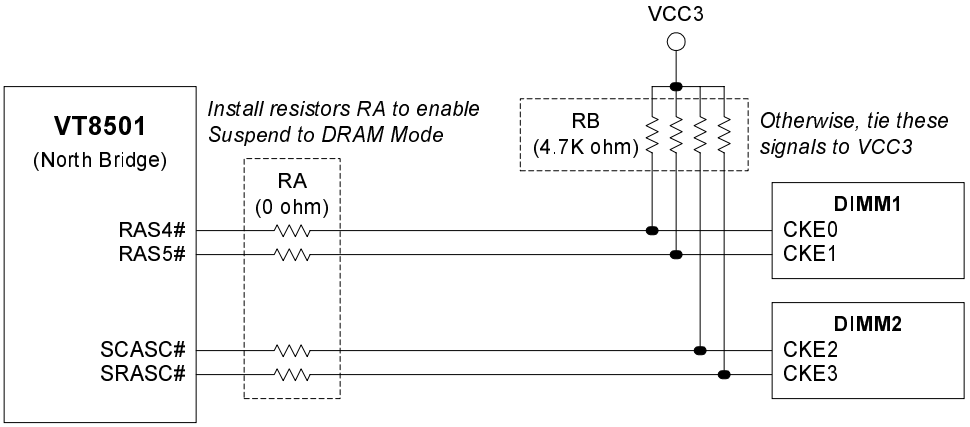


Figure 2-44. Schematic Example of Choosing Suspend to DRAM Mode

2.3.6 PCI Interface Layout and Routing Guidelines

It is recommended that the VT8501 and VT82C686A be placed at both ends of the PCI bus for better signal termination. An example topology of the PCI bus on an ATX form factor is shown in Figure 2-45 below.

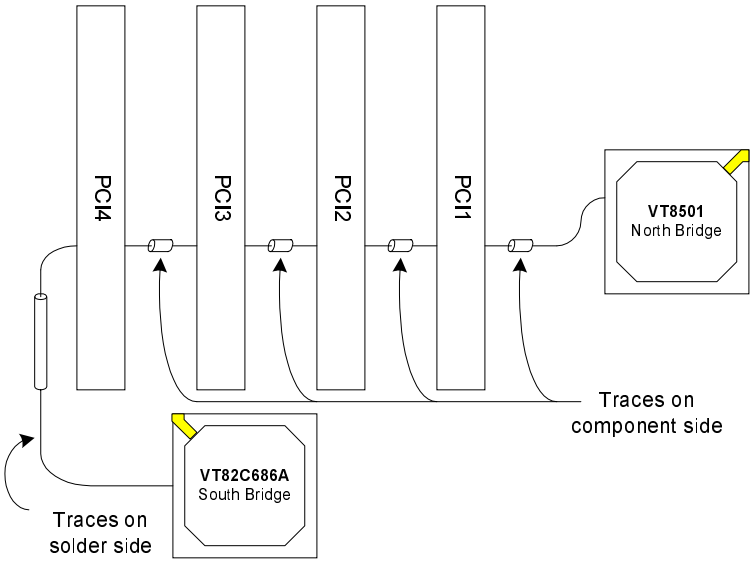


Figure 2-45. PCI Topology Example

Each of the following signals IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#, PERR#, SERR#, FRAME#, INTA#, INTB#, INTC#, and INTD# requires a 4.7K ohm pull-up to VCC. The REQ# signals need 2.2K ohm pull-ups to VCC. The GNT# signals need 2.2K ohm pull-ups to VCC3.

2.3.7 Graphic Subsystem Layout and Routing Guidelines

The material presented in this section provides schematic examples and layout guidelines for the graphic subsystem of the Apollo MVP4 North Bridge. The recommended trace sizes and restrictions are based on conservative "worst case" design conditions for an Apollo MVP4 based motherboard. There is a degree of flexibility in the trace widths, but the values presented in this section are strongly recommended if real estate and budget permit.

2.3.7.1 Clock Synthesizer

The on-chip clock synthesizer inside the MVP4 Graphics Controller requires a quartz crystal of the following characteristics:

Table 2-9. Clock Synthesizer Characteristics

Frequency	14.31818MHz +0.1% fundamental resonance
Load Capacitance	15 pF to 40 pF in parallel resonance mode
ESR	25 to 45 ohm
Shunt Capacitance	Approximately 5 pF

The crystal should be connected across XTL1 (pin AA4) and XTL2 (pin AA5). Both sides of the crystal should have solder pads to allow grounding of the case and attachment of the crystal to the PCB in a secure manner. A ground area should be present under the crystal for multi-layer board designs. There should not be any via close to or underneath the crystal case, so as to prevent shorts between the case and other signal traces or VCC.

If a 14.31818 MHz oscillator is used instead of a crystal, then the clock output of the oscillator should be connected to XTL1 only and XTL2 should be left open. The preferred solution is to connect a 14.31818 MHz reference clock output generated from an external clock synthesizer to XTLI instead of either a crystal or an oscillator (see figure 2-46 below).

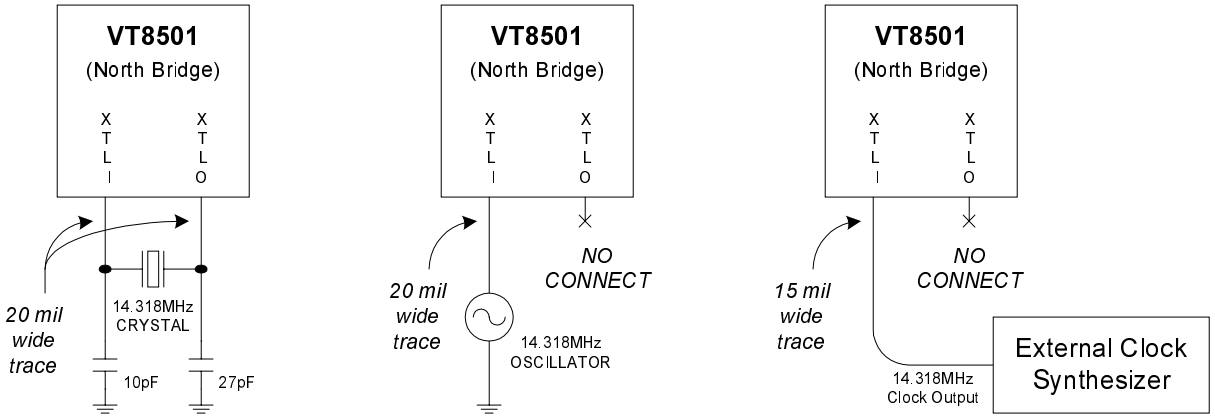


Figure 2-46. Connection Examples of the 14.318MHz Crystal Input Pad (XTLI)

2.3.7.2 Graphics Power Layout Recommendations

For the Graphics Controller portion of the Apollo MVP4 North Bridge, analog power and ground layout recommendations are given in this section. A brief description of Graphics Power signals is listed in Table 2-10. A schematic example for analog and digital power connections is shown in Figure 2-47.

Table 2-10. Power and Ground of Graphics Controller

Signal Name	Pin #	I/O	Description
VCCR	D1	P	Power for RAMDAC Digital Logic (2.5V)
VCCD	Y1	P	Power for PLL1 and PLL2 Digital Logic (2.5V)
VCCV1	Y2	P	Power for PLL1 Analog Circuitry (2.5V)
GNDV1	AA1	P	Ground for PLL1 Analog Circuitry
VCCV2	AA2	P	Power for PLL2 Analog Circuitry (2.5V)
GNDV2	AB1	P	Ground for PLL2 Analog Circuitry
VCCS	C1	P	Power for DAC Current Source Analog Circuitry (2.5V)
GNDS	B1	P	Ground for DAC Current Source Analog Circuitry
GNDRGB	A1	P	Ground for RGB Analog Output Current Balance Path

Analog and Digital Ground Separation

Analog and digital separations for power and ground are very important for mixed signal devices. For the design presented in Figure 2-47, not only is analog ground separated from digital ground, but also analog ground for the DAC side is separated from analog ground for the clock side of the chip. Traces for analog ground should not have any digital connections.

- Ferrite beads are used to isolate analog voltage and analog ground from digital voltage and digital ground respectively.
- All power and ground traces should be at least 50 mil wide and as short as possible before entering the BGA chip.
- Ceramic 0.1 uF and 0.001 uF decoupling capacitors act as local noise filters; hence they should be located as close to the respective power and ground pins as possible. Different values of ceramic capacitors are better at filtering different frequencies with lower values better at filtering higher frequencies, so using both 0.1 uF and 0.001 uF capacitors is effective in reducing a wider range of noise frequencies than could be done with any single capacitor value.
- 10uF bulk capacitors are used as a supply of local charge, thus smoothing power flow from the supply to the local circuit.
- Place a 560 pF ceramic capacitor (C1) as close to pin VLF1 of the VT8501 chip as possible. The trace width must be at least 20 mils.
- Place a 560 pF ceramic capacitor (C2) as close to pin VLF2 of the VT8501 chip as possible. The trace width must be at least 20 mils.
- Place a 0.1 uF ceramic capacitor (C3) as close as possible to the VT8501 chip COMP pin and a 360 ohm precision resistor (R3) as close as possible to the VT8501 chip IRSET pin. Each trace width should be wider than 30 mils.

Note: It is important that noise from the digital sections of the PCB should be prevented from coupling into the DAC and RGB output sections. Otherwise, visual artifacts will be created on the display.

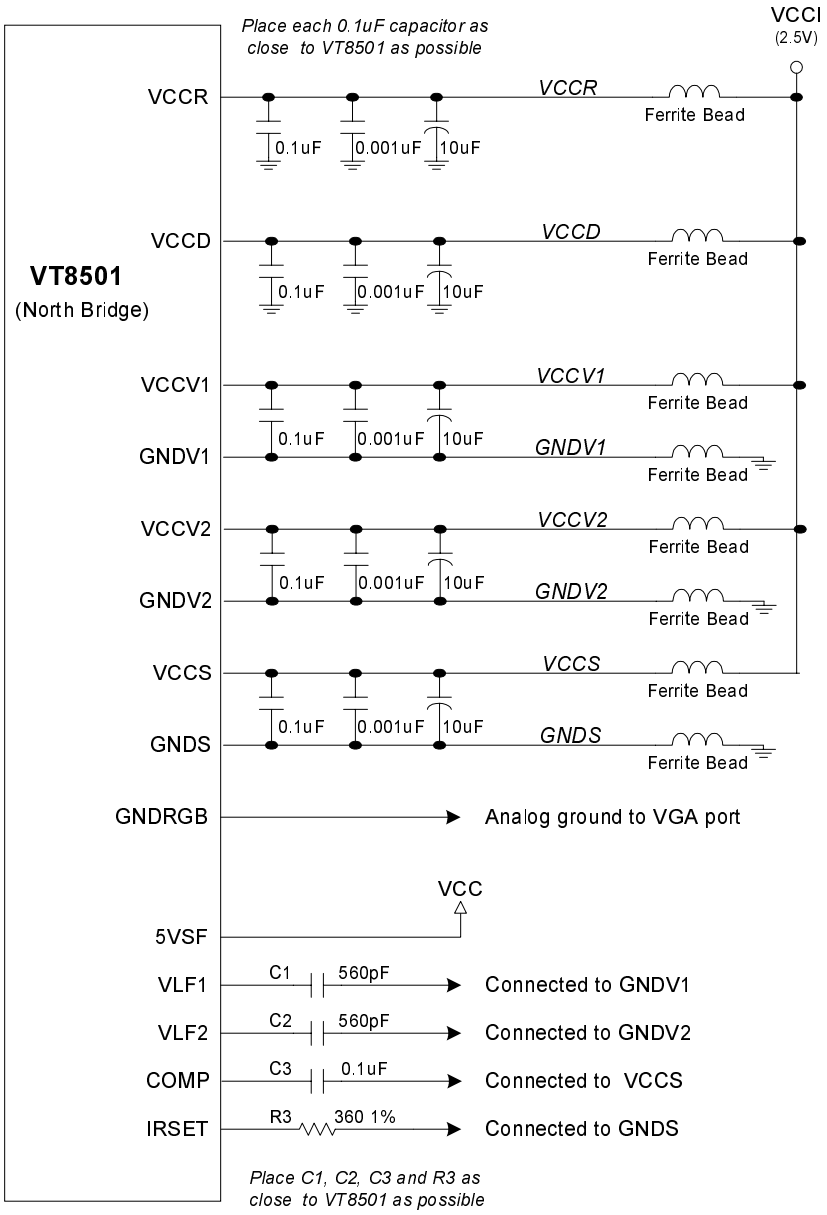
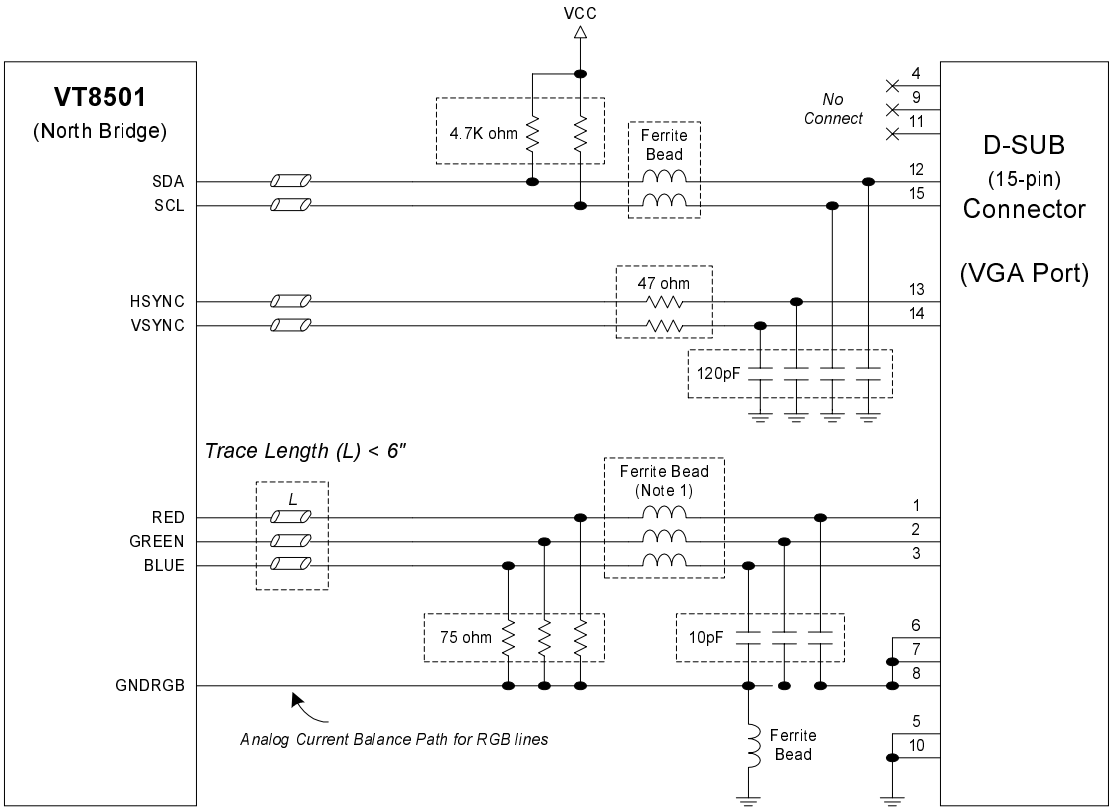


Figure 2-47. Analog and Digital Power Connections

2.3.7.3 Graphic Hardware Interfaces

CRT Interface

Analog R, G, and B (red, green, and blue) traces should be designed to be as short as possible. Careful design, however, will allow considerable trace lengths with no visible artifacts. GNDRGB is an "analog current balance path" for the RGB lines. The RGB outputs are current sources and therefore require 75 ohm load resistors from each RGB line to GNDRBG to create the output voltage (approximately 0 to 0.7 volts). These resistors should be placed near the VGA port (a 15-pin D-SUB connector). Serial ferrite beads for the RGB lines should have high frequency characteristics to eliminate relative noise. The 47 ohm series damping resistors for HSYNC and VSYNC should be placed near the D-SUB connector (see figure 2-48 below).



Note 1: These ferrite beads should have high frequency caracteristics. (ex. 26 Ohms at 100MHz)

Figure 2-48. CRT Interface

In terms of layout, GNDRGB should follow 2 traces that encapsulate the RGB traces all the way to the D-shell connector (VGA Port), and should not be tied to ground until connected to the Right Angle D-type connector. Refer to Figure 2-49 for more details. Routing guidelines are listed below:

- RGB lines should be at least 12 mils wide and no longer than 6 inches.
- The GNDRGB ground trace surrounding the RGB lines and their RLC components should be at least 15mils wide and spaced away from outside signals as much as possible possible. GNDRGB should also be tied to VGA connector pins 6, 7, and 8.
- The connection between GNDRGB and digital ground should be a ferrite bead or a narrow channel (a short ground trace about 30 mils wide). This connection near the D-SUB connector should be placed in a quiet area that has no nearby signals.

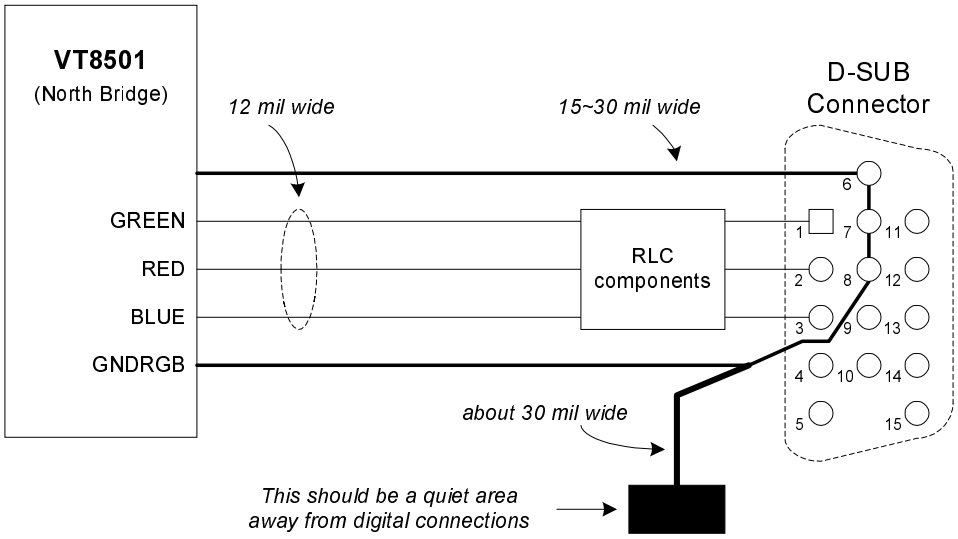


Figure 2-49. RGB Output Current Balance Path

Digital Monitor Interface

PanelLink ™ Technology implementing the VESA® Transition Minimized Differential Signaling (TMDS) standard can transfer data, clock, and control signals from the host graphics controller to high resolution, high color flat-panel-display-based monitors. This interface uses a Silicon Image TMDS transmitter chip (refer to the Silicon Image SIL140 datasheet and application notes for more details). A single pixel per clock interface example supporting the industry standard "DFP" interface is shown in figure 2-50 below. A complete schematic of this interface is shown in Appendix B.

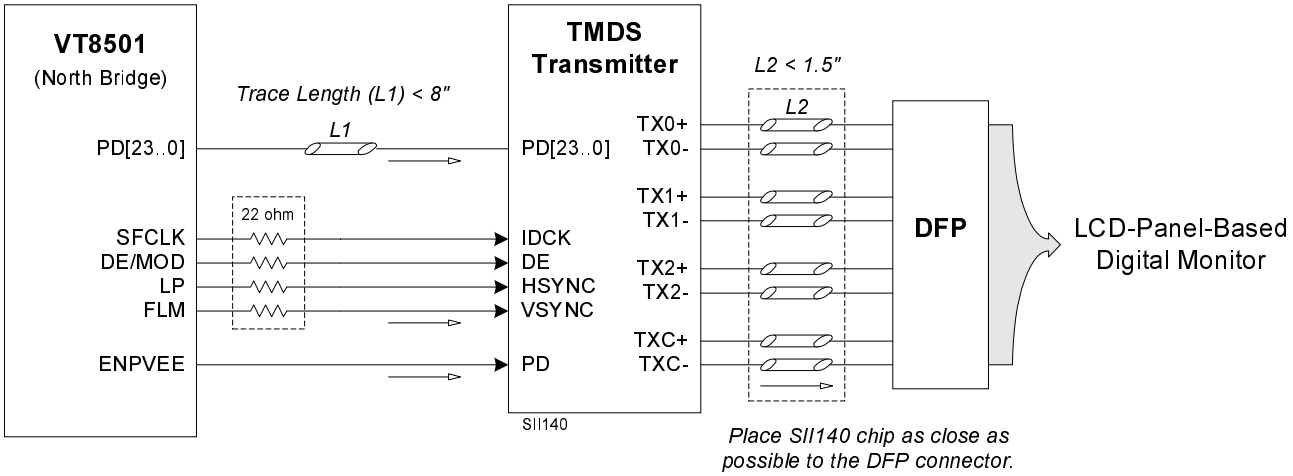


Figure 2-50. TFT Panel (Single Pixel/Clock) Interface using TMDS

Note: PanalLink and TMDS are trademarks of Silicon Image, Inc. VESA is a registered trademark of the Video Electronics Standards Association.

Direct Drive STN Flat Panel Interfaces - 24 Bit/Pixel, Single Pixel/Clock

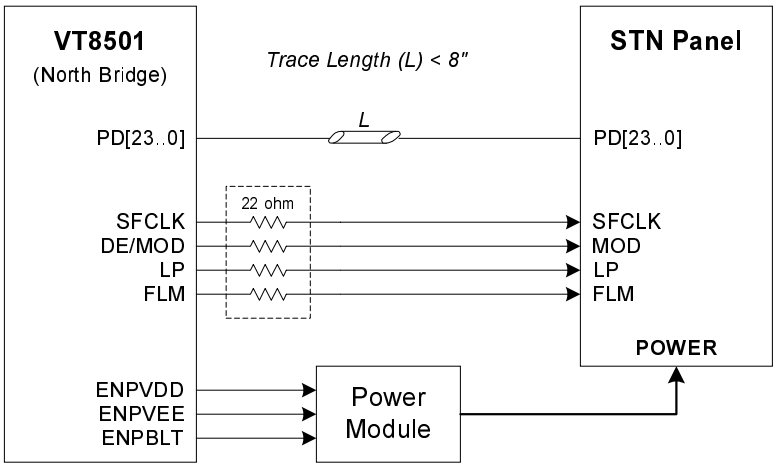


Figure 2-51. Direct Drive STN Panel (Single Pixel/Clock) Interface

Direct Drive TFT Flat Panel Interfaces - 24 Bit/Pixel, Single Pixel/Clock

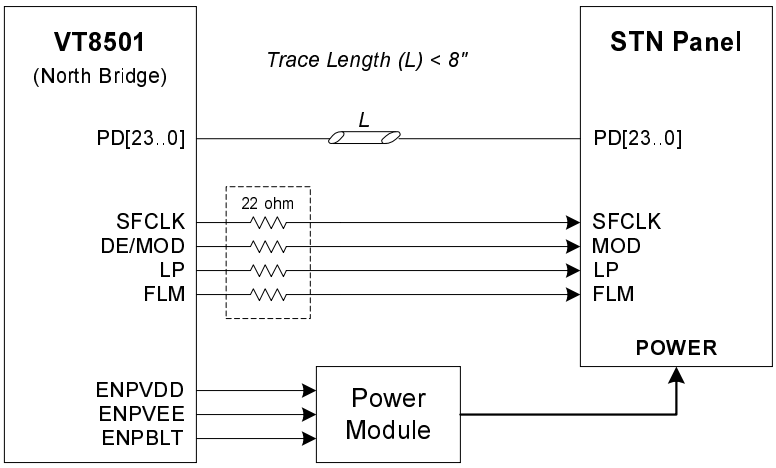


Figure 2-52. Direct Drive TFT Panel (Single Pixel/Clock) Interface

TFT Flat Panel Interface - 18 Bit / Pixel, Double Pixel / Clock

A double pixel per clock interface example supporting an 18+18-bit XGA LCD panel with LVDS is shown in Figure 2-53. If the LVDS transmitters are programmed to use the clock FALLING edge to latch data, S1 should be used to clock the LVDS transmitters. If the LVDS transmitters are programmed to use the clock RISING edge to latch data, S2 should be used to clock the LVDS transmitters.

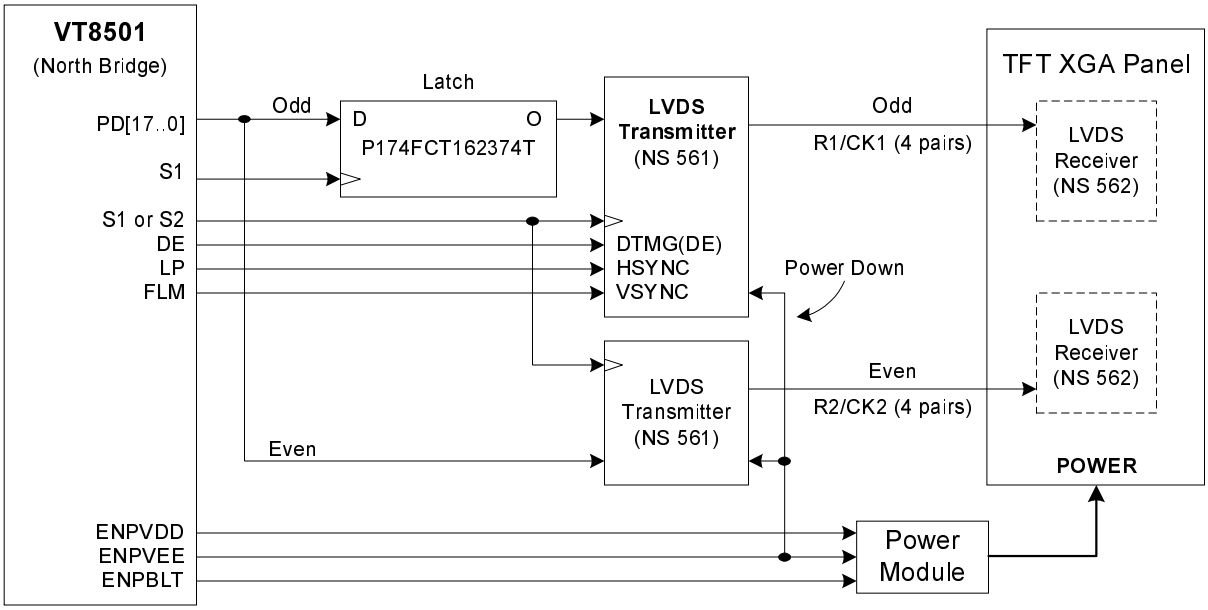


Figure 2-53. TFT Panel (Double Pixel / Clock) Interface

TV In / Video Capture Interface

The function of the video capture interface is to receive digital video pixel data streams from other video sources, such as a TV decoder, and store them in the frame buffer. The stored video image can be either displayed together with a graphic image or fetched by the CPU to perform further processing such as video editing or hard disk storage. An example of a video capture interface is shown in Figure 2-54. A video capture application circuit for implementing a TV decoder on board is shown in Appendix C.

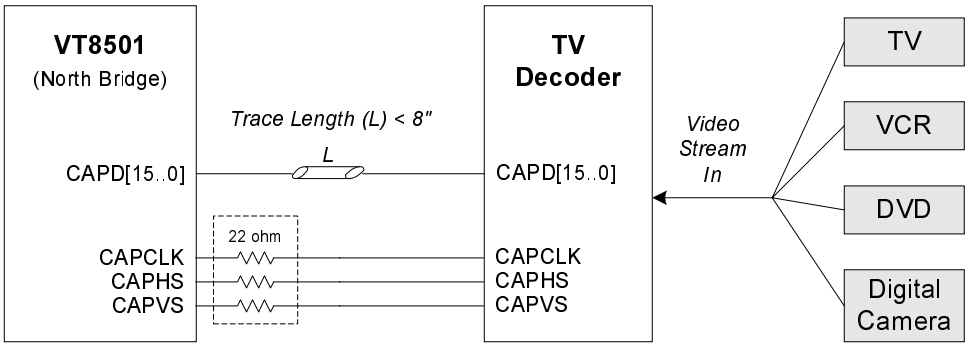


Figure 2-54. TV In / Video Capture Interface

TV Out Interface

By using a TV digital encoder, PC images can be displayed on a TV set. A TV-Out interface example is shown in Figure 2-55. A TV-Out application circuit for implementing a TV encoder on board is shown in Appendix D.

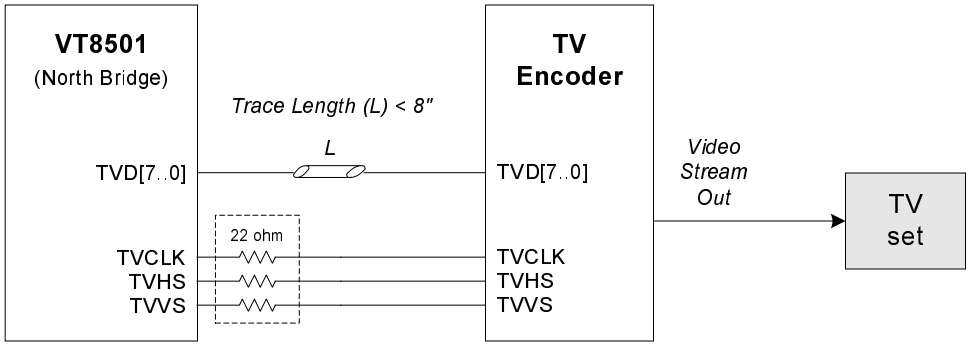


Figure 2-55. Digital TV-out Interface

2.3.8 South Bridge Interface Layout and Routing Guidelines

2.3.8.1 USB controller

The Universal Serial Bus (USB) provides a bi-directional, isochronous, hot-attachable Plug and Play serial interface for adding external peripheral devices such as game controllers, communication devices, and input devices on a single bus. Brief descriptions of the USB signals of the VT82C686A are listed in Table 2-11. The VT82C686A provides four USB ports. Only port 1 and port 2 have over-current detect pins (OC1# and OC2#), however, the over current status of port 0 and port 3 can still be sensed for implementing 4 USB ports. The VT82C686A will scan SD[3:0] during the ISA refresh period as OC[3:0]# of the USB ports. If this over-current scan logic is implemented, pins OC1# and OC2# may be left open or used for alternative functions. A schematic drawing for four over-current scans is illustrated in figure 2-56 below.

Table 2-11 Universal Serial Bus (USB) Signals

Signal Name	I/O	Description
USBP0+	IO	USB Port 0 Data +
USBP0-	IO	USB Port 0 Data -
USBP1+	IO	USB Port 1 Data +
USBP1-	IO	USB Port 1 Data -
OC1#	I	USB Port 1 Over Current Detect. Port 1 is disabled if this input is low.
USBP2+	IO	USB Port 2 Data +
USBP2-	IO	USB Port 2 Data -
OC2#	I	USB Port 2 Over Current Detect. Port 2 is disabled if this input is low.
USBP3+	IO	USB Port 3 Data +
USBP3-	IO	USB Port 3 Data -
USBCLK	I	USB clock. Connected to a 48MHz clock output of the system clock synthesizer.

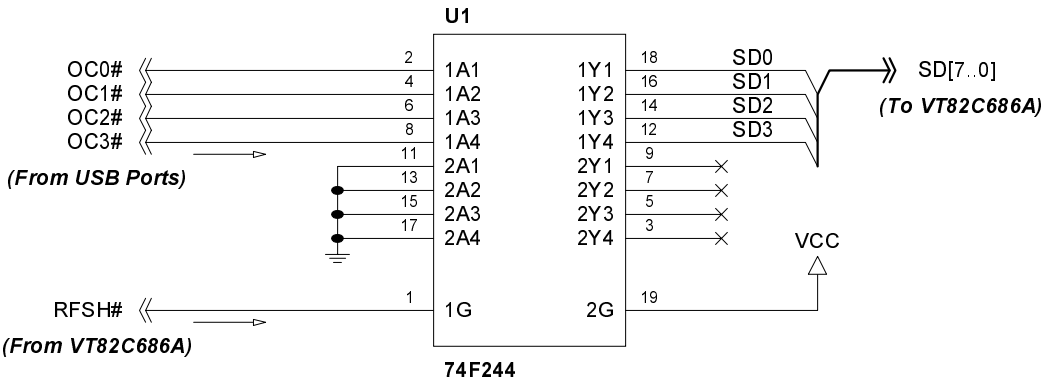


Figure 2-56. USB Over-Current Scan Logic

The layout guidelines for USB are listed below.

- Each pair of USB data signals is required to be parallel to each other with the same trace length.
- Each pair of USB data signals is required to be parallel to a respective ground plane.

A routing example of two pairs of USB data buses is shown in figure 2-57 below.

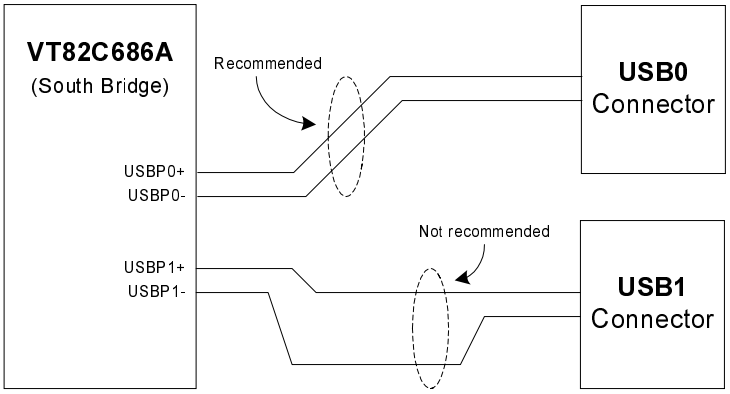


Figure 2-57. USB Differential Signal Routing Example

2.3.8.2 AC'97 Link and Game/MIDI Ports

Table 2-12 shows a brief description of the signals of AC'97 Link Controller and Game Ports. All those signals are multi-function pins with the second IDE channel bus. To enable both functions, the power up strapping of SPKR (pin V5 of the VT82C686A) must be pulled up to VCC3 with a 4.7K~10K ohm resistor.

Table 2-12. Signal Description of AC'97 Link and Game/MIDI Ports

Signal Name	I/O	Description
BITCLK (SDD0)	I	AC'97 Bit Clock
SDIN (SDD1)	I	AC'97 Serial Data In
Reserved (SDD2)	I	AC'97 Serial Data In 2 (reserved)
SYNC (SDD3)	O	AC'97 Sync
SDOUT (SDD4)	O	AC'97 Serial Data Out
ACRST (SDD5)	O	AC'97 Reset
JBY (SDD6)	I	Game Port Joystick B Y-axis
JBX (SDD7)	I	Game Port Joystick B X-axis
JAY (SDD8)	I	Game Port Joystick A Y-axis
JAX (SDD9)	I	Game Port Joystick A X-axis
JAB2 (SDD10)	I	Game Port Joystick A Button 2
JAB1 (SDD11)	I	Game Port Joystick A Button 1
JBB2 (SDD12)	I	Game Port Joystick B Button 2
JBB1 (SDD13)	I	Game Port Joystick B Button 1
MSO (SDD14)	O	MIDI Serial Out
MSI (SDD15)	I	MIDI Serial In

AC'97 Link

An AC'97 Controller is integrated in the VT82C686A and currently supports only one Codec. One Primary Codec (ID 00) is completely compatible with existing AC'97 definitions and extensions. The Codec ID functions as a chip set select. For more details, refer to the AC'97 Component Specification Revision 2.1.

AC-link is a digital serial link between the AC'97 Controller and AC'97 devices. AC-link signals are multi-function pins with the Second IDE channel bus (SDD[0..5]). A linking example between the AC'97 Controller and one AC'97 Codec is shown in figure 2-58. A complete schematic for implementing the VIA VT1611 AC'97 Audio Codec is shown in Appendix E.

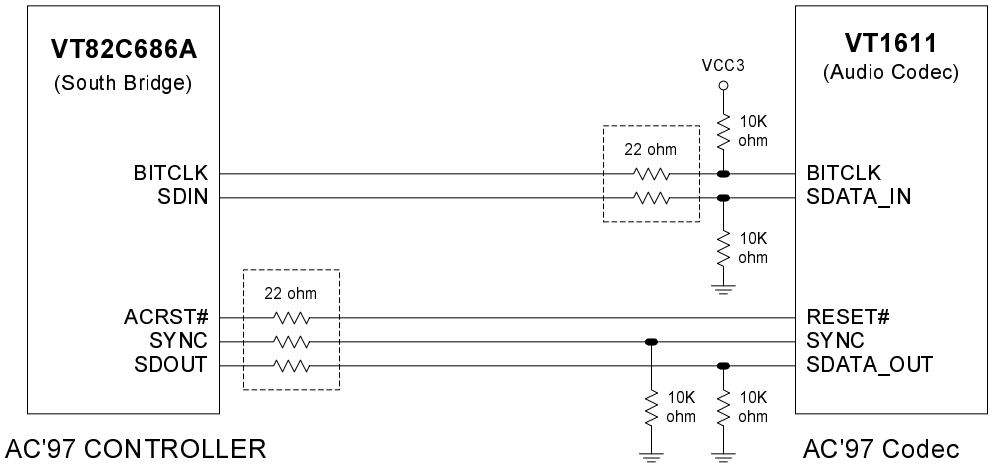


Figure 2-58. AC'97 Link Example

Game/MIDI ports

The VT82C686A supports two direct game ports (Joystick A and Joystick B) and one MIDI port interface. An application circuit of MIDI/Game port is shown in Figure 2-59.

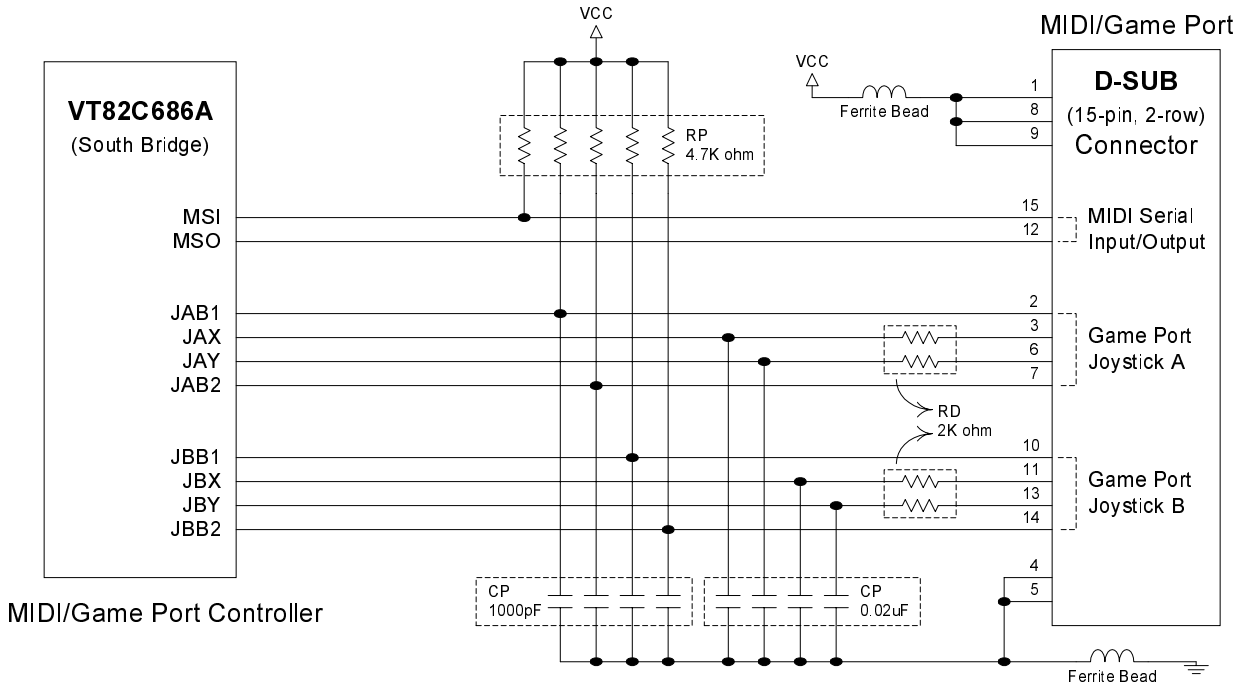


Figure 2-59. MIDI/Game Port Application Circuit

2.3.8.3 Hardware Monitoring

The hardware monitoring interface includes five positive voltage sensing inputs (four external and one internal), three temperature sensing inputs (two external and one internal), two fan-speed monitoring inputs and one chassis intrusion detection input. Programmable control, status, monitor and alarm are supported by the VT82C686A for flexible desktop management. The following sections provide detailed descriptions for each hardware monitor subsystem. An application circuit for hardware monitoring is shown in Figure 2.60. In order to achieve a stable VCC3 input to the Hardware Monitoring Subsystem, a 0.1uF decoupling capacitor should be placed as close to the Hardware Monitoring power and ground pins as possible.

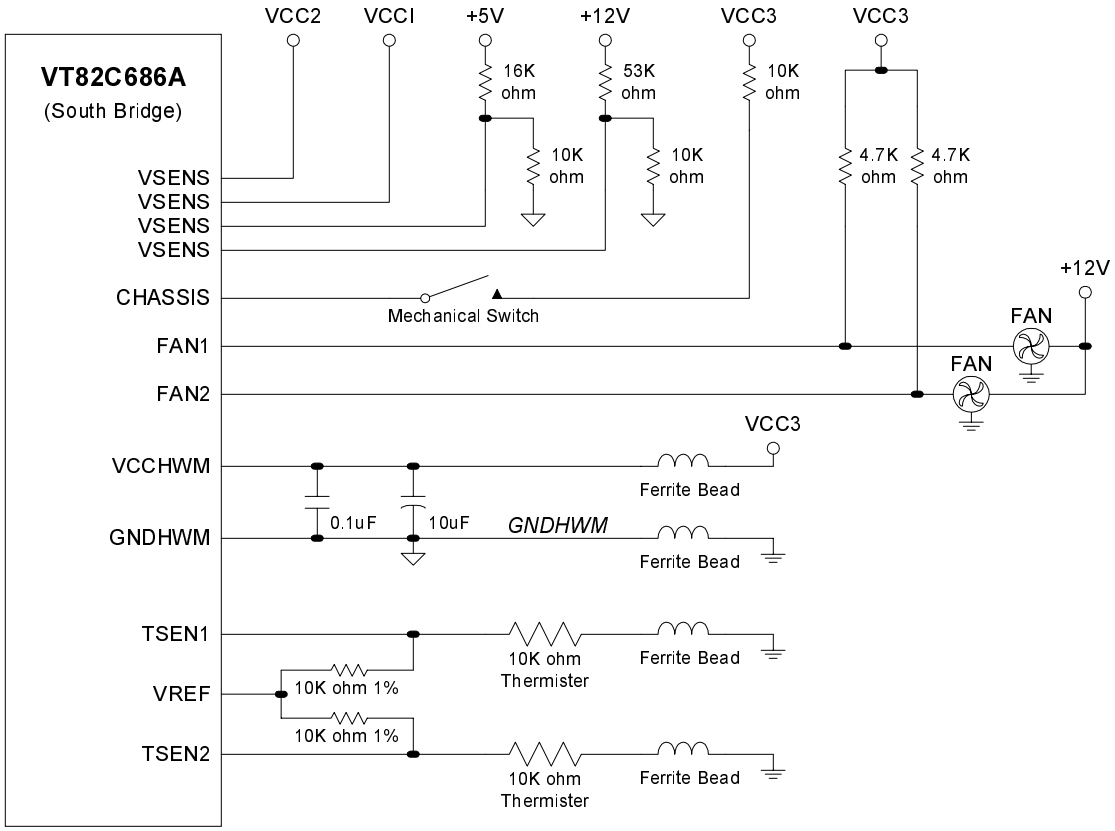


Figure 2-60. Hardware Monitoring Application Circuit

Voltage Monitoring

Typically VCC2 (core voltage of the CPU), VCCI (2.5V, core voltage of the VT8501), VCC3 (3.3V), 5V, and +12V are the five monitored voltage inputs. VCC2 and VCCI can be directly connected to the inputs. The +5V and 12V inputs should be attenuated with external resistors to any desired value within the input range. VCC3 is internally connected to the hardware monitoring system voltage detection circuitry for 3.3V monitoring. An alarm will issue when any monitored voltage level is out of range. Layout and grounding guidelines are listed below:

- These voltage inputs will provide better accuracy when referred to their respective ground (AGND) which is separated from digital common ground (GND). Please refer to the application circuit above.
- Voltage dividers should be located physically as close to the voltage input pins as possible.

Temperature Sensing

One internal thermal sensor is located inside the VT82C686A chip. Two external thermisters for two temperature sensing inputs are used to directly contact the device whose temperature will be monitored. Layout and grounding guidelines are listed below:

- The thermister should be placed very near a measured object. For example, a thermister can be placed right under a Socket-7 CPU.
- The other end of a thermister should be connected to ground through a ferrite bead.

Fan-Speed Monitoring

Fan speed inputs are provided for signals from fans equipped with tachometer outputs. One fan-speed-monitoring pin can be used to measure the CPU fan speed. The other can be an auxiliary one. A programmable fan-speed control can be implemented in the following three steps.

- **Speed Monitoring:** The fan speed value is measured by a fan-speed monitoring pin
- **Temperature Sensing:** The temperature value is measured by a temperature sensing pin
- **Speed Controlling:** The fan speed is controlled by a dedicated General Purpose Output (GPO) pin

Chassis Intrusion Detection

The detection is an active high interrupt from any chassis intrusion violation. It could be accomplished mechanically, optically, or electrically. Circuitry external to the chassis intrusion detect pin is expected to latch the event.

2.3.8.4 Integrated Super IO Controller

In the VT82C686A, an integrated Super IO Controller supports two UARTs for complete serial ports, one dedicated IR port, one multi-mode parallel port, and one floppy drive controller function. Refer to the Apollo MVP4 Reference Design Schematics in Appendix A for more details on application circuits.

2.3.8.5 System Management Bus Interface

The I2C bus signal pair of the VT8501 is dedicated to the I2C bus of the CRT interface. The I2C bus signal pair of the VT82C686A will handle the remaining I2C buses to other on-board devices such as the Clock Synthesizer and the three DIMM slots. A block diagram of System Management Bus Interfaces is shown in Figure 2-61. It is recommended to place both pull-ups at the end of the I2C bus.

- Adding 68pF capacitors in Figure 2-61 (b) for the pair at the end device is essential since the I2C bus travels a long way and might pick up noise along the route.

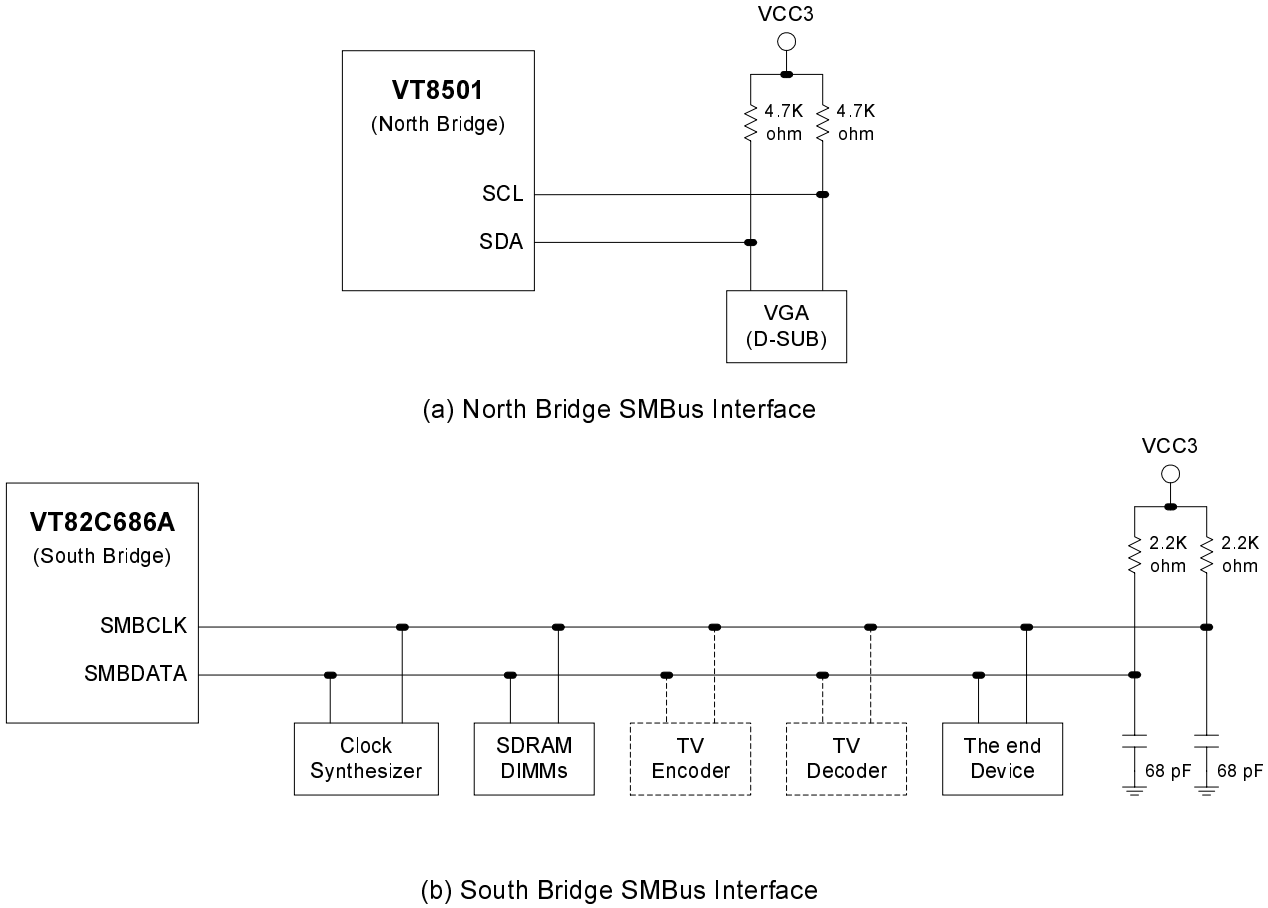
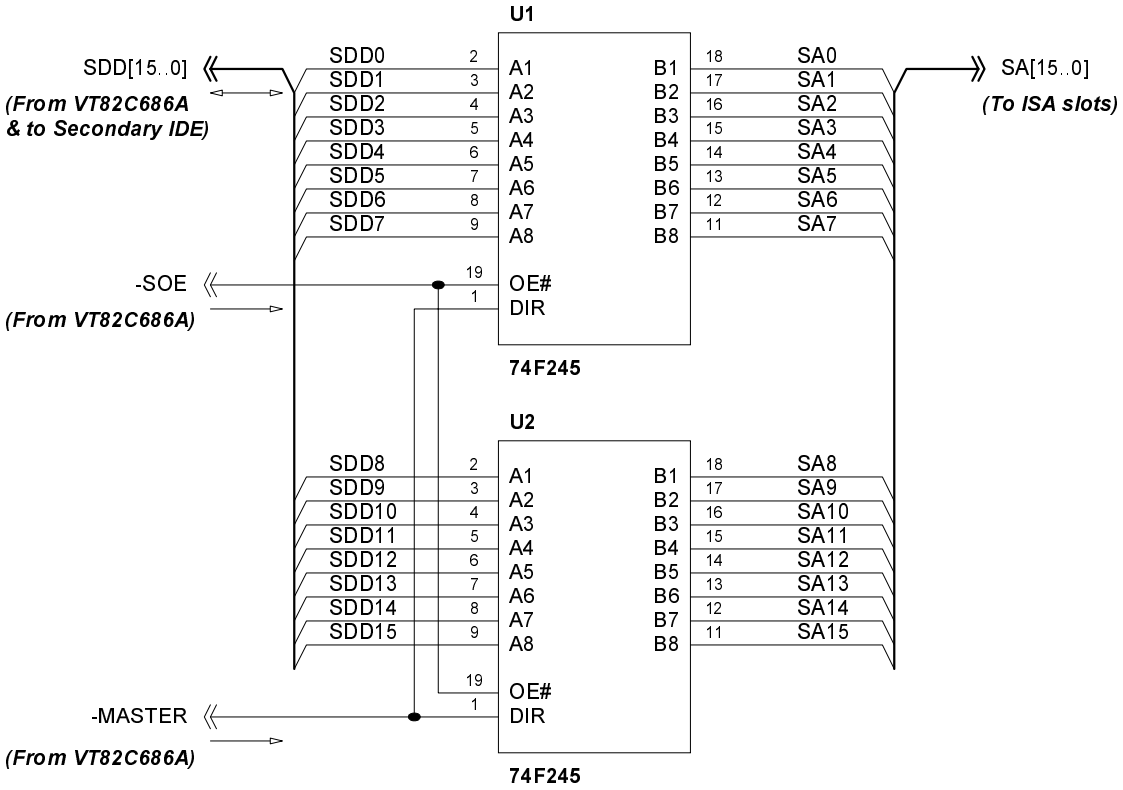


Figure 2-61. Two Separate System Management Bus Interfaces

2.3.8.6 IDE

Both Primary and secondary IDE channels of the VT82C686A have their own control signals. The Primary IDE channel has a dedicated data bus. However, the secondary IDE data bus is multiplexed with an Audio/Game port or it can share ISA address bus SA[15:0] as SDD[15:0]. The two options are listed below for selecting the secondary IDE data bus.

- Option 1: The secondary IDE data bus uses its own bus SDD[15:0] sharing with an Audio/Game port when the SPKR pin is strapped low. No Audio/Game port is supported in this case since these functions are shared with the SDD[15..0] pins.
- Option 2: The secondary IDE data bus shares ISA address bus SA[15:0] as SDD[15:0] through two 74F245 transceivers when the SPKR pin is strapped high. The sharing circuitry is shown in Figure 2-62. Audio/Game port functions are enabled on the SDD[15:0] pins.



Note: These 74F245 Transceivers are optional if ISA bus load is not a concern.

Figure 2-62. ISA Bus SA[15:0] / SDD[15:0] Sharing Circuitry

Dual channel master mode PCI supports four Enhanced IDE devices. The transfer rate for each device can support up 33 MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface. Transmission line effects and signal crosstalk emerge in the IDE related signals. To eliminate ringing and reflection caused by the transmission line effect, trace length and impedance match must be taken into account. An example IDE layout is shown in Figure 2-63. Recommended layout rules for both primary and second IDE ports are listed below:

- The trace attribute of all primary IDE signals is in a minimum of 6 mils wide and 9 mils between two adjacent traces. The recommended trace length is less than 6 inches.
- All ATA signals in Figure 2-63 require series termination resistors. The series resistors (R_A) should be placed within 1 inch of the VT82C686A chip. The series resistors (R_B) should be placed within 1 inch of the primary IDE connector.
- Signal DD7 needs a 10K pull-down on the VT82C686A chip side of series termination
- Signal DREQ needs a 5.6K pull-down on the connector side of the series termination
- Signal IRQ14 (or IRQ15) needs a 10K pull-down or pull-up (preferred) on the connector side of the series termination
- Signal IORDY# needs a 1K pull-up on the connector side of the series termination
- Pin 28 of the IDE connectors should be tied to ground with a 470 ohm serial resistor.
- It is recommended to layout the following signals to each IDE connector in equal length. They are signals DD[15..0], IOR#, IOW#, and IORDY#.

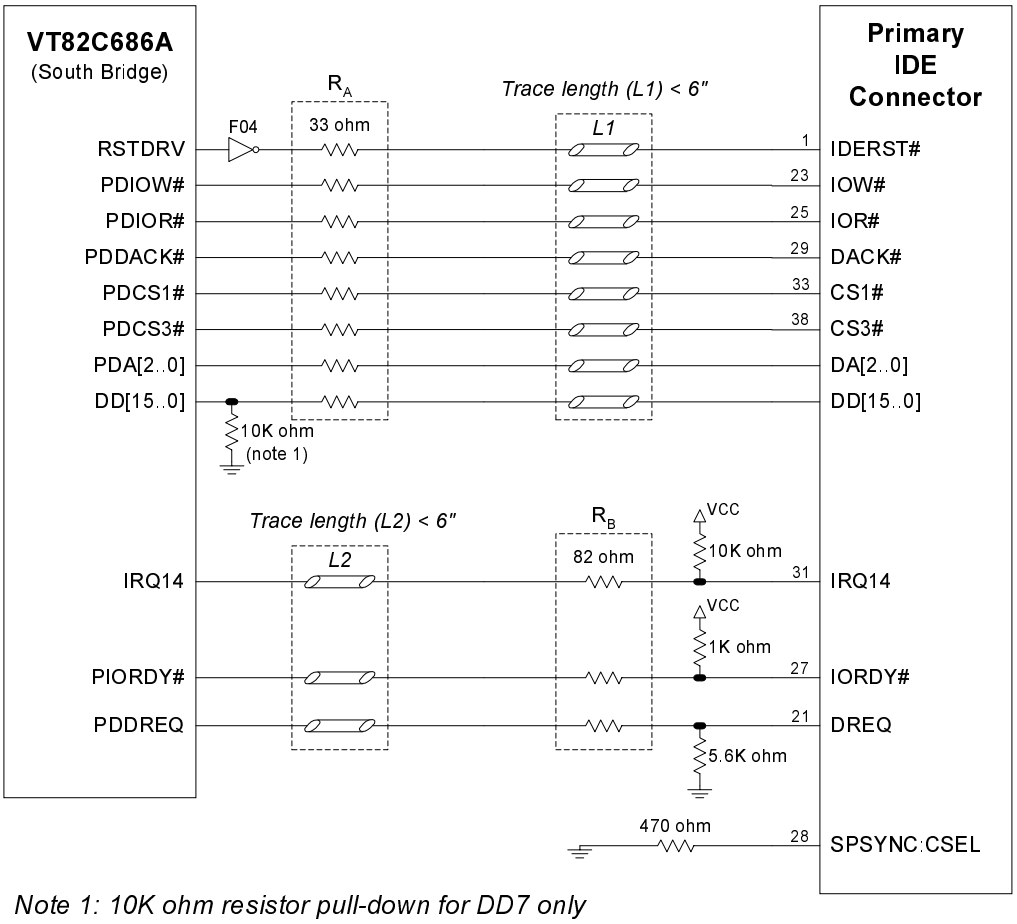


Figure 2-63. IDE Interfaces Layout Guidelines

Ultra DMA/66 Interface Layout Guidelines

VT82C686A supports Ultra DMA/66 IDE interfaces on both Primary IDE channel (IDE1) and Secondary IDE channel (IDE2). A Micro-ATX component placement example for implementing the Ultra DMA/66 interface (option 2) is shown in Figure 2-64. The detailed placement for the VT82C686A chip and two IDE connectors is illustrated in the lower left corner of the figure. The major difference from the former placement is the shorter distance between VT82C686A and primary IDE and Secondary IDE connectors. The shorter length for both IDE data buses is required because this bus is running at a high speed (66MHz). In order to fulfill this requirement, the VT82C686A chip can be lowered and both IDE connectors can be shifted to the left. Recommended layout guidelines are listed below.

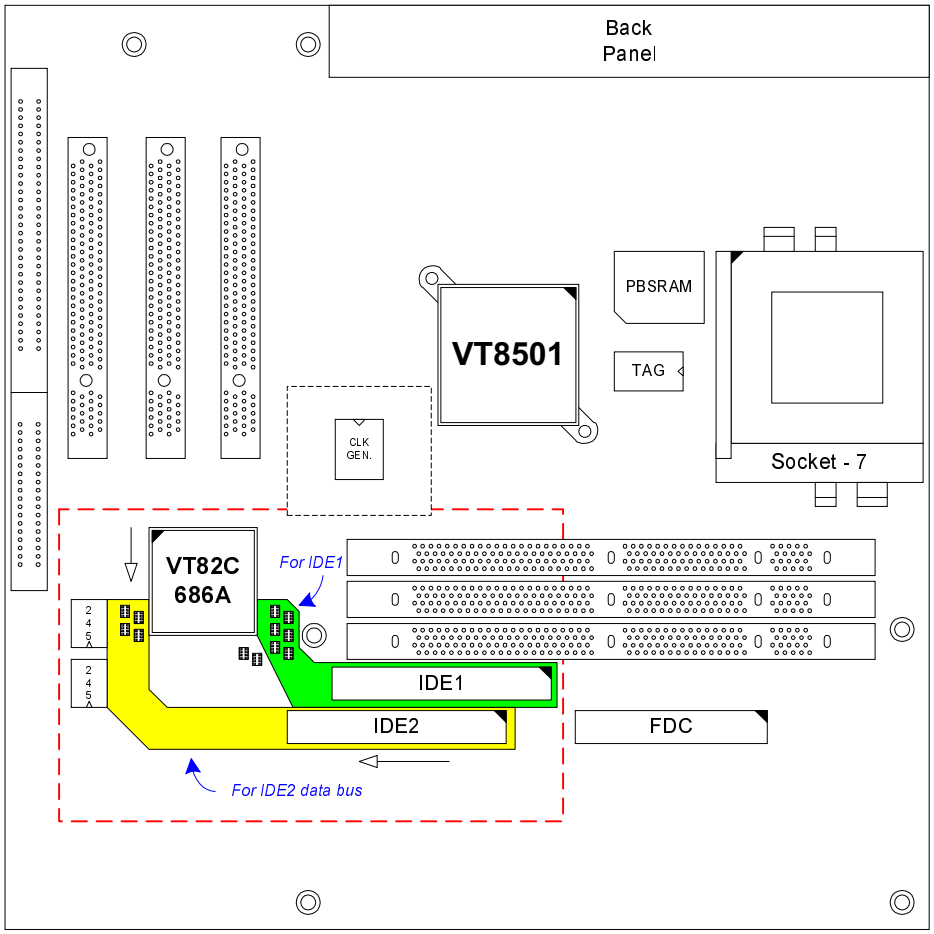
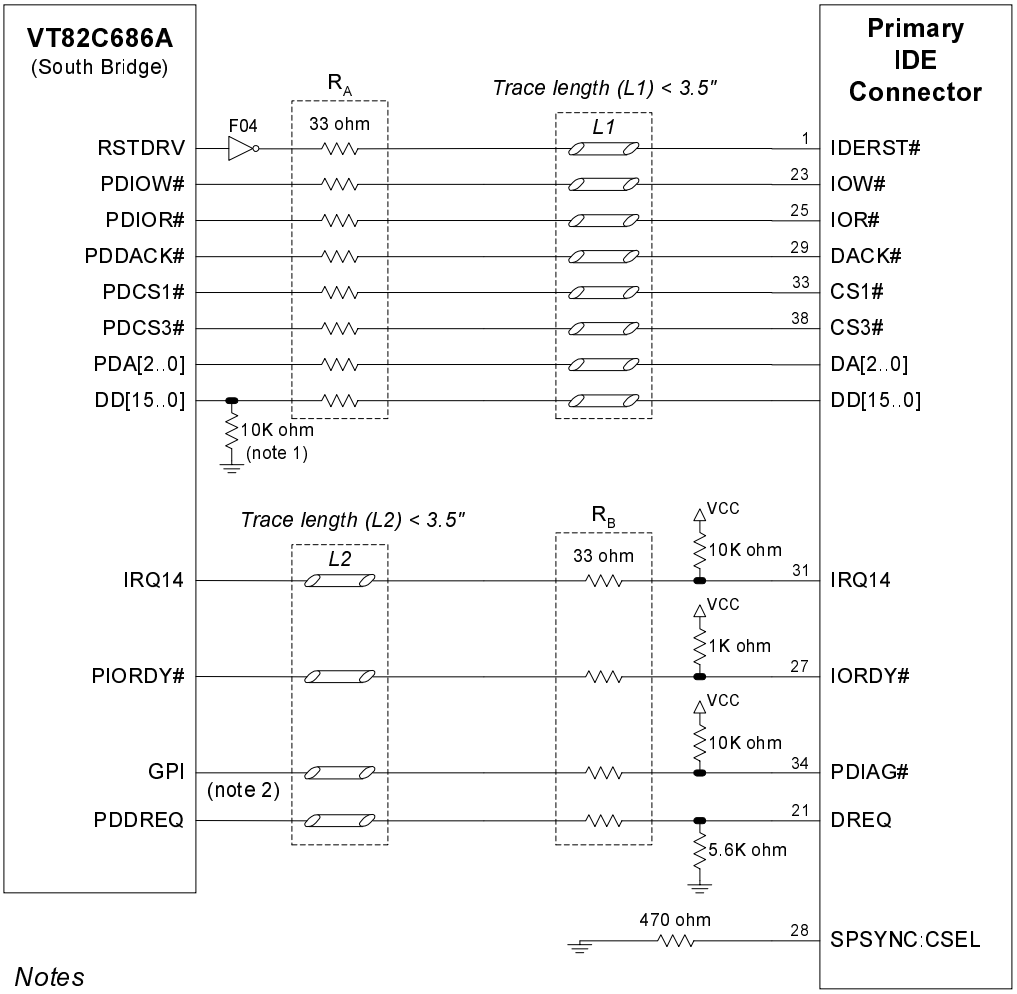


Figure 2-64. Ultra DMA/66 Placement and Routing Example

The application circuit of the ultra DMA/66 IDE interface is shown in Figure 2-65. The 80-conductor cable, required by the ultra DMA/66 IDE interface, is the major difference from the 40-conductor cable of the current IDE interface. For the detection of the 80-conductor cable, pin 34 (CBLID) of IDE connector may be used to provide a signal state from an ultra DMA/66 device to a GPI pin of the South Bridge Controller. The detection can be done in an alternative hardware solution too.

Layout rules for the IDE interface in the former section can be adapted for ultra DMA/66 use unless some of them are modified in the following layout guidelines.

- The trace attribute of all primary IDE signals is in a minimum of 6 mils wide and 9 mils between two adjacent traces.
- All signals for primary IDE and Secondary IDE require 33 ohm series termination resistors. Place these series terminations as close (less than 1 inch) to the VT82C686A as possible.
- Data and strobe lines should be routed as a bus. The trace length of these signals should be shorter than 4.5 inches. The maximum trace length difference among them must be less than 1 inch. Other lines should be as short as possible.



Notes

1. 10K ohm resistor pull-down for DD7 only.

2. Pin 34 of primary IDE connector is connected to one of GPI pins from VT82C686A.

Figure 2-65. Ultra DMA/66 Application Circuit

TIMING ANALYSIS AND SIMULATION

The 100 MHz timing analysis here will provide the concept of the trace length limitation for some high speed buses and control signals such as the CPU address bus (A[31..3]) and Tag RAM write enable signal (TAGWE#).

3.1 Timing Analysis

Cache control timing diagrams and memory read/write timing diagrams are discussed in this section. A brief analysis is given for each diagram. 100 MHz system frequency is assumed where one clock (1T) represents 10 ns. Reasons for the limited lengths of some signals (referring to Section 2.3) are described in the timing analyses.

3.1.1 Cache Control Timing

The timing diagrams for an L2 burst read cycle of 3-1-1-1 and an L2 burst write cycle of 3-1-1-1 with one PBSRAM chip (one bank) are shown in Figures 3-1 and 3-2. A timing diagram for an L2 burst read cycle of 3-1-1-1 2-1-1-1 with two PBSRAM chips (two banks) is shown in Figures 3-3. Figure 3-4 represents the timing diagram of CPU Read Miss and Dirty L2 Cache Write Back.

The timing analyses for three different cache hit cycles (see Figures 3-1, 3-2 and 3-3) are listed below:

- At T2, cache hit (Read hit or Write hit) is decided by the VT8501 North Bridge Controller. At the time ADS# is asserted, only 2 clocks (20 ns) are allowed for the VT8501 to decide a cache hit or not. During this period, the CPU asserts the address bus A[63..0] and then the VT8501 will assert the Tag RAM address bus TA[7..0]. Obviously, the timing margin is tight. In order to increase the timing margin of the cycle, one of the best solutions is to minimize the propagation delay of the TA[7..] signals on the PCB. It is recommended to place the Tag RAM chip near CPU. In other words, the length of TA[7..] should be as short as possible.
- At T3, only 1T (10 ns) is allowed for reading out or writing in the first pipelined burst data. The length of the CPU data bus should be limited to increase the timing margin of the cycle. If it is too long, the signal quality of the CPU data bus will be reduced. The clock skew between the CPU clock and the PBSRAM clock will affect the setup time and hold time for PBSRAM data to the CPU data bus. Therefore, clock alignment between the CPU clock and the PBSRAM clock should be maintained.
- Till T6, the L2 burst read and write cycle of 3-1-1-1 for the one-bank case is complete (see figures 3-1 and 3-2). For the two-bank case, the L2 burst read cycle of 3-1-1-1 2-1-1-1 is complete at T11 (see figure 3-3).

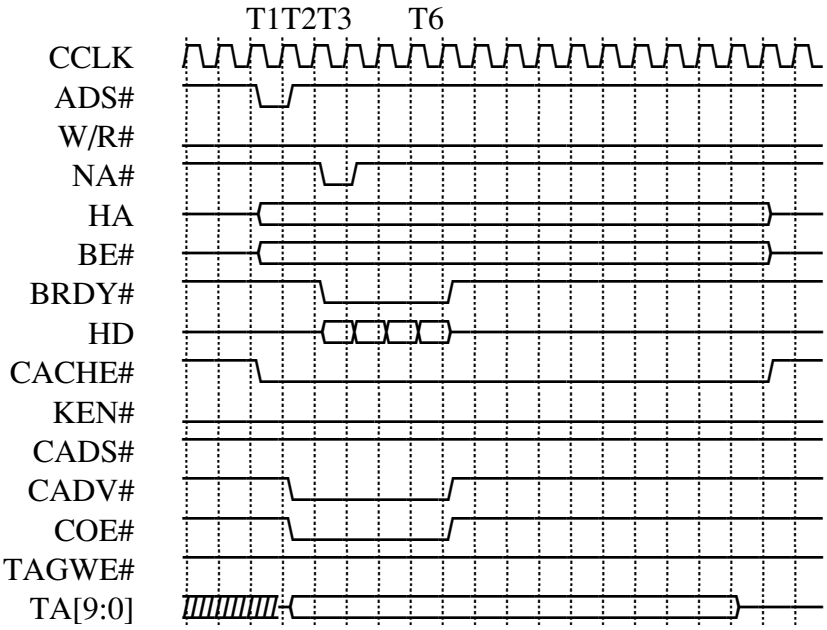


Figure 3-1. Read Hit Cycle of 3-1-1-1 (1 Bank)

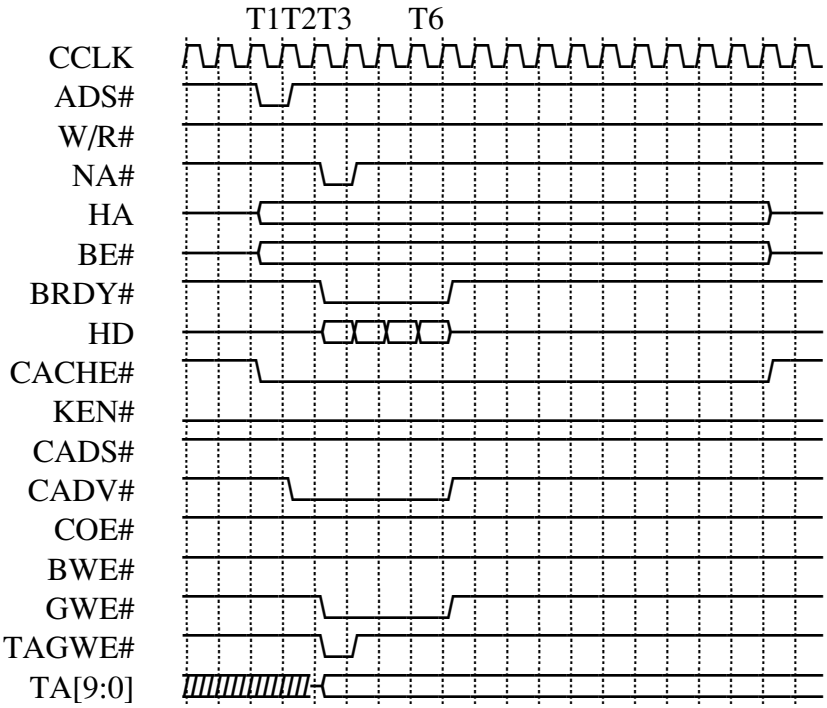


Figure 3-2. Write Hit Cycle of 3-1-1-1 (1 Bank)

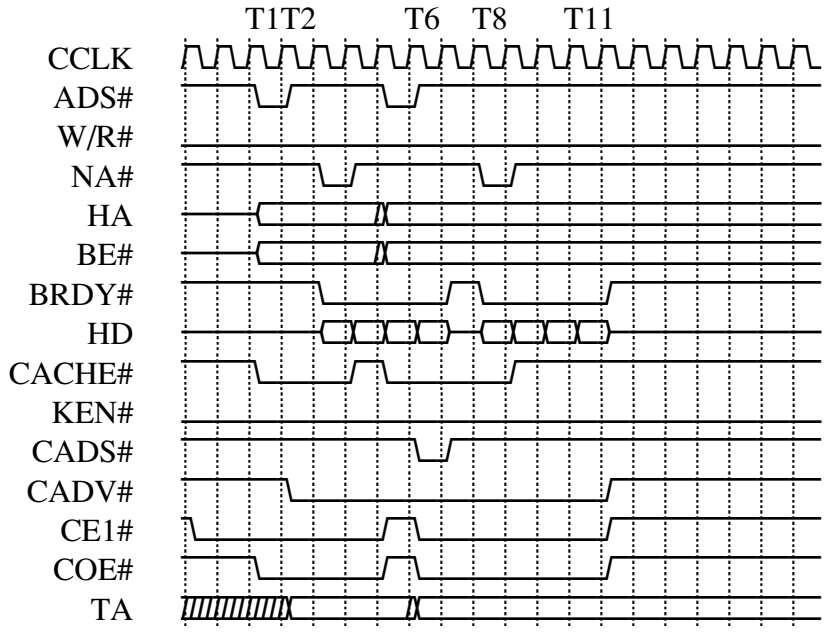


Figure 3-3. Read Hit Cycle of 3-1-1-1 2-1-1-1 (2 Banks)

The timing analyses for an L2 burst read miss cycle followed by a dirty L2 cache write back (see Figures 3-4) are listed below:

- At T2, an L2 burst read miss is decided by the VT8501 north bridge. The data in the L2 cache is read out to the CPU to Memory FIFO buffers in the VT8501. At the time ADS# is asserted, only 2 clocks (20 ns) are allowed for the VT8501 to decide an L2 read miss or not. During this period, the CPU asserts address bus A[63..0] signals and then the VT8501 will assert the Tag RAM address bus TA[7..0]. Obviously, the timing margin is tight. In order to increase the timing margin of the cycle, one of the best solutions is to minimize the propagation delay of TA[7..] signals on the PCB. It is recommended to place the Tag RAM chip near the CPU. In other words, the length of TA[7..] should be as short as possible.
- At T3, only 1T (10 ns) is allowed for the PBSRAM to output the first pipelined burst data. The length of the CPU data bus should be limited to increase the timing margin of the cycle. If it is too long, the signal quality of the CPU data bus will be reduced. The clock skew between the CPU clock and the PBSRAM clock will affect the setup time and hold time for PBSRAM data to the CPU data bus. Therefore, clock alignment between the CPU clock and the PBSRAM clock should be maintained.
- After T6, DRAM memory data is sent back to the CPU and the cache controller also copies it into the cache memory and updates directory information in the Tag RAM. After T20, the data stored in the VT8501 CPU-to-memory FIFO is sent to the DRAMs. According to the cycles above, the timing is critical. In order to increase the timing margin of the cycle, one of the best solutions is to minimize the propagation delay of the MD[63..0], TAGWE# and L2 control signals on the PCB. Therefore, the length of the MD[63..0], TAGWE# and L2 control signals should be limited because there is only one clock between assertion of the cache control signals and data output.

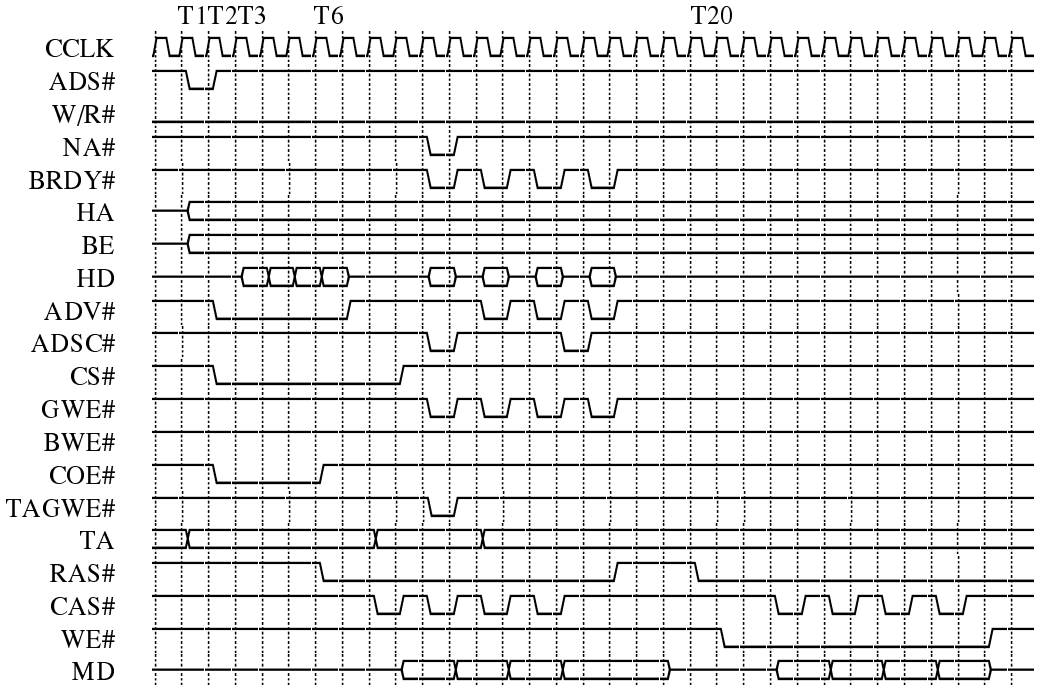


Figure 3-4. Read Miss and L2 Cache Write Back

3.1.2 SDRAM Timing

Timing diagrams for CPU Read from SDRAM and CPU Write to SDRAM are illustrated in Figures 3-5 and 3-6. Timing analyses for SDRAM read and write cycles are listed below:

- The clock skew between the CPU clock and the SDRAM clocks will affect the setup time and hold time of SDRAM command signals and the MD[63..0] because the CPU reads or writes the data out of or into the SDRAM. Therefore, clock alignment between the CPU clock and the SDRAM clocks should be maintained.
- According to the cycles above, the timing is critical. In order to increase the timing margin of the cycle, one of the best solutions is to minimize the propagation delay of the MD[63..0] and SDRAM control signals on the PCB. Therefore, the length of MD[63..0] and SDRAM control signals should be limited because there is only one clock between assertion of the SDRAM control signals and data input or output.

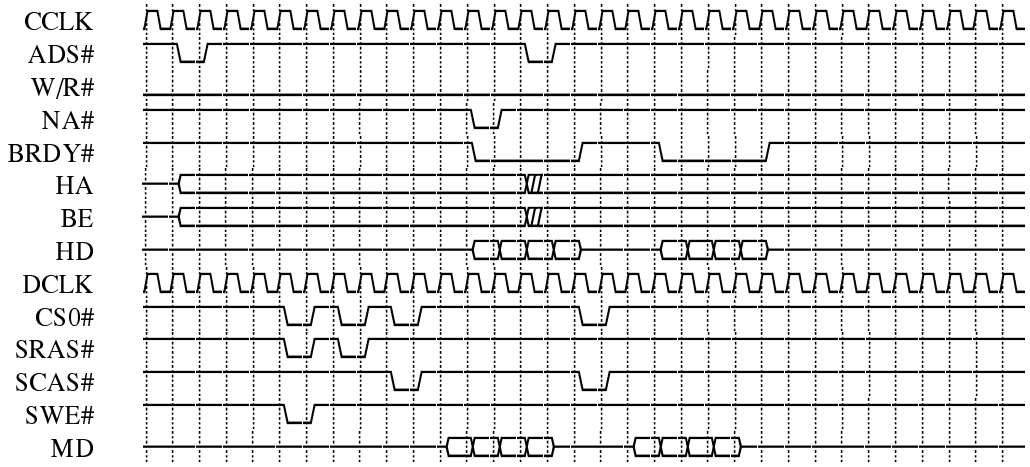


Figure 3-5. CPU Read from SDRAM

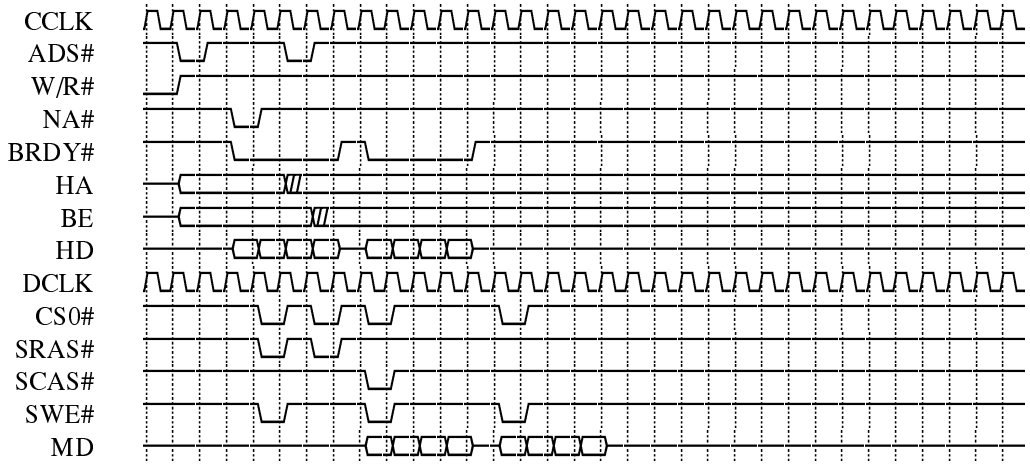


Figure 3-6. CPU Write to SDRAM

ELECTRICAL SPECIFICATIONS

This section describes the electrical specifications of the VT8501.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation is not implied under the ratings listed in Table 4-1.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_A	Ambient Operating Temperature	0	70	^{0}C	1
T_S	Storage Temperature	-55	125	^{0}C	1
V_{IN}	Input Voltage	-0.5	V_{RAIL} + 10%	Volts	1,2
V_{OUT}	Output Voltage	-0.5	V_{RAIL} + 10%	Volts	1,2

Notes:

1. *Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.*
2. *V_{RAIL} is defined as the VCC level of the respective rail. The CPU interface can be 3.3V or 2.5V. The Memory and Flat panel interfaces must be 3.3V only. The PCI and Video interfaces can be 3.3V or 5.0V.*

4.2 Recommended Operating Ranges

Functional operation of the VT8501 is guaranteed if the values of voltage and temperature are within the limits defined in Table 4-2.

Table 4-2. Recommended Operating Ranges

Symbol	Parameter	Min	Max	Notes
T_A	Ambient Operating Temperature	0 ^{0}C	70 ^{0}C	
V_{CC2_5}	2.5V Power (to Core Logic)	2.375 V	2.625 V	
V_{CC3}	3.3V Power to (IO Buffer)	3.135 V	3.465 V	
V_{CC}	+5V Power	4.7 V	5.25 V	

4.3 DC Characteristics

DC characteristics of the VT8501 are shown in Table 4-3.

Table 4-3. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	+2.0	V_{CC}+0.5	V	Note 1
V_{OL}	Output Low Voltage	-	0.55	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 1.0 mA
I_{IL}	Input Leakage Current	-	+/-10	uA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate Leakage Current	-	+/-20	uA	$0.55 < V_{OUT} < V_{CC}$
I_{CC2_5}	Power Supply Current	-	800	mA	Note 2
I_{CC3}	Power Supply Current	-	300	mA	Note 3

Notes:
1. V_{CC} refers to the voltage being applied to VCC during functional operation.
2. V_{CC2_5} = 2.5 V - The maximum power supply current must be taken into account when designing a power supply.
3. V_{CC3} = 3.3 V - The maximum power supply current must be taken into account when designing a power supply.

4.4 Power Dissipation

Table 4-4 contains the maximum power dissipation of the VT8501 during different system frequencies.

Table 4-4. Maximum Power Dissipation

Supply Voltage	66MHz	100MHz	Conditions
2.5V	1.75W (V_{CC2_5} = 700 mA)	2W (V_{CC2_5} = 800 mA)	Preliminary Estimation
3.3V	0.825W (V_{CC3} = 250 mA)	0.99W (V_{CC3} = 300 mA)	Preliminary Estimation
Total power consumption	2.575W	2.99W	Preliminary Estimation

SIGNAL CONNECTIVITY AND DESIGN CHECKLIST

5.1 Overview

The single Socket-7 processor, Apollo MVP4 North Bridge, and "Super South" South Bridge are the three major components in a VIA Apollo MVP4 based PC system. A signal connectivity table and a design checklist are given for both North Bridge and South Bridge in the following sections. Pin connections may vary in different circuit designs. Some pins have been repeatedly described for different functions in different sub-tables.

A signal connectivity table provides board designers a quick reference of signal connections. And it can be used to review schematics of an Apollo MVP4 system. The design checklist can provide a quick way to review the PCB layout of an Apollo MVP4 system.

5.2 Apollo MVP4 North Bridge Controller

The connectivity for each signal of the VT8501 South Bridge is listed in Table 5-1.

Table 5-1. VT8501 North Bridge Connectivity

CPU INTERFACE		
Signal Name	**I/O**	**Connection**
ADS#	IO	Connect to CPU. 4.7K ohm pull-up to VCC3.
M/IO#	IO	Same as the above.
W/R#	IO	Same as the above.
D/C#	IO	Same as the above.
BRDY#	IO	Same as the above.
KEN#/INV	O	Same as the above.
NA#	O	Same as the above.
BOFF#	O	Same as the above.
CACHE#	I	Same as the above.
HLOCK#	I	Same as the above.
SMIACT#	I	Same as the above.
EADS#	O	Connect to CPU.
HITM#	I	Connect to CPU.
AHOLD	O	Connect to CPU.
BE[7:0]#	IO	Connect between CPU, VT8501 and PBSRAM. 4.7K ohm pull-up to VCC3.
HA[31:3]	IO	Connected to CPU through a 22 ohm series resistor. And connect to PBSRAM directly.
HD[63:0]	IO	Connected to CPU through a 22 ohm series resistor. And connect to PBSRAM directly.

CACHE CONTROL		
Signal Name	**I/O**	**Connection**
CADS#	O	Connect to PBSRAM.
CADV#	O	Same as the above.
COE#	O	Same as the above.
CCS#	O	Same as the above.
GWE#	O	Same as the above.
BWE#	O	Same as the above.
TA[7:0]	IO	Connect to TAG SRAM.
TWE#	O	Same as the above.

DRAM INTERFACE		
Signal Name	**I/O**	**Connection**
MD[63:0]	IO	Connect to DRAM.
MECC[7:0]	IO	Same as the above.
MA[13:0]	O	Connected to DRAM through a 22 ohm series resistor.
RAS[5:0]#/CS[5:0]#	O	Same as the above. RAS4# and RAS5# have the DRAM clock enable (CKE) functions.
CAS[7:0]/DQM[7:0]#	O	Same as the above.
SRASA#	O	Same as the above.
SRASB#	O	Same as the above.
SRASC#	O	Same as the above. This pin can implement the DRAM clock enable (CKE) function.
SCASA#	O	Same as the above.
SCASB#	O	Same as the above.
SCASC#	O	Same as the above. This pin can implement the DRAM clock enable (CKE) function.
SWEA#/MWEA#	O	Same as the above.
SWEB#/MWEB#	O	Same as the above.
SWEC#/MWEC#	O	Same as the above.

PCI BUS INTERFACE		
Signal Name	**I/O**	**Connection**
CBE[3:0]#	IO	Connect toVT82C686A and PCI slots.
AD[31:0]	IO	Connect to VT82C686A and PCI slots.
FRAME#	IO	Connect between VT8501, PCI slots, and VT82C686A. 10K ohm pull-up to VCC.
IRDY#	IO	Same as the above.
TRDY#	IO	Same as the above.
STOP#	IO	Same as the above.
DEVSEL#	IO	Same as the above.
SERR#	I	Same as the above.
LOCK#	IO	Connect between VT8501 and PCI slots. 10K ohm pull-up to VCC.
PAR	IO	Connect to VT82C686A and PCI slots.
PREQ#	I	Connect to VT82C686A. 10K ohm pull-up to VCC3.
PGNT#	O	Connect to VT82C686A. 10K ohm pull-up to VCC3.
REQ[3:0]#	I	Connect to corresponding PCI slots. 2.2K ohm pull-up to VCC.
GNT[3:0]#	O	Connect to corresponding PCI slots. 2.2K ohm pull-up to VCC3.
REQX#	I	Connect to 1394 devices. Otherwise, 4.7K ohm pull-up to VCC3.
GNTX#	O	Connect to 1394 devices. Otherwise, no connect.
INTA#	O	Connect to one of the PIRQ[D:A]# pin of VT82C686A.

CRT INTERFACE		
Signal Name	**I/O**	**Connection**
RED	A	Connected to VGA port through a series ferrite bead and a 10pF capacitor to VGA analog ground (GNDRGB).
GRN	A	Same as the above.
BLUE	A	Same as the above.
HSYNC	O	Connected to VGA port through a series 47 ohm resistor and a 120pF capacitor to ground.
VSYNC	O	Same as the above.
COMP	A	Connected to VCCS through a series 0.1uF capacitor.
IRSET	A	Connect to GNDS through a series 360 ohm (precision 1%) resistor.
SDA	IO	Connect to VGA port only. 4.7K ohm pull-up to VCC.
SCL	IO	Same as the above.

PANEL INTERFACE		
Signal Name	**I/O**	**Connection**
PD[23:0]	O	Connect to TMDS or LVDS transmitters of LCD panel circuitry.
SHFCLK	O	Connected to TMDS or LVDS transmitters of LCD panel circuitry through a 22 ohm series resistor.
DE	O	Same as the above.
LP	O	Same as the above.
FLM	O	Same as the above.
ENPVDD	O	Connect to LCD panel circuitry.
ENPVEE	O	Same as the above.
ENPBLT	O	Same as the above.
IMIO	O	Connect to Clock Modulator for effective EMI reduction.
IMIIN	I	Connect to Clock Modulator for effective EMI reduction and 4.7K ohm pull-up to VCC3.

VIDEO INTERFACE		
Signal Name	**I/O**	**Connection**
VIDD[15:0]	IO	Connect to VMI connector or TV decoder.
VIDHS	IO	Same as the above
VIDVS	IO	Same as the above.
VIDCLK	IO	Connected to VMI connector or TV decoder through a 22 ohm series resistor.

TV INTERFACE		
Signal Name	**I/O**	**Connection**
TVD[7:0]	O	Connect to TV encoder.
TVHS	O	Same as the above.
TVVS	O	Same as the above.
TVCLK	O	Connected to TV encoder through a 22 ohm series resistor.

CLOCK AND RESET CONTROL		
Signal Name	**I/O**	**Connection**
HCLK	I	Connect to the CPU clock output of the system clock synthesizer.
MCLKI	I	Connect to the SDRAM clock output of the system clock synthesizer.
MCLKO	O	Connect to the SDRAM clock input of the system clock synthesizer.
PCLK	I	Connect to the PCI clock output of the system clock synthesizer.
PCKRUN#	IO	Connected to VT82C686A and the system clock synthesizer if the function is applied. Otherwise, connect to VT82C686A then through a 100 ohm serial resistor to ground.
XTLI	I	Connect to a 14.318MHz crystal or Connect to a 14.318MHz output of the system clock synthesizer.
XTLO	O	Same as the above.
RESET#	I	Connected to VT82C686A through a 74F240 inverter.
PWROK	I	Connect to VT82C686A and Power Good circuitry.
SUST#	I	Connect to VT82C686A.
SUSP	I	4.7K ohm pull-up to VCC3 if SUSPEND function is not applied. If applied, one example is to connect it to a GPO pin.

MISCELLANEOUS		
Signal Name	**I/O**	**Connection**
ENTEST#	I	4.7K ohm pull-up to VCC3 if test mode function is not applied.
VLF1		Connected to ground through a 560pF series capacitor.
VLF2		Same as the above.

5.3 "Super South" South Bridge Controller

The connectivity for each signal of VT82C686A South Bridge is listed in Table 5-2. Motherboard designers can use this table as a quick reference to review their schematics. Some pins have been repeatedly described for different functions in different sub-tables, please be careful in using the following table.

Table 5-2. VT82C686A South Bridge Connectivity

PCI BUS INTERFACE		
Signal Name	**I/O**	**Connection**
PCLK	I	Connect to the PCI clock output of an external Clock Synthesizer.
AD[31:0]	IO	Connect to VT8501 and PCI slots.
C/BE[3..0]#	IO	Connect to VT8501 and PCI slots.
FRAME#	IO	Connect between VT8501, PCI slots, and VT82C686A. 10K ohm pull-up to VCC.
IRDY#	IO	Same as the above.
TRDY#	IO	Same as the above.
STOP#	IO	Same as the above.
DEVSEL#	IO	Same as the above.
SERR#	I	Same as the above.
PAR	IO	Connect to VT8501 and PCI slots.
IDSEL	I	Connect to AD18 with a series 100 ohm resistor.
PIRQ[D:A]#	I	Connect to pins INT[D..A]# of each PCI slot as follows: PIRQA# PIRQB# PIRQC# PIRQD# PCI slot 1 INTA# INTB# INTC# INTD# PCI slot 2 INTB# INTC# INTD# INTA# PCI slot 3 INTC# INTD# INTA# INTB# PCI slot 4 INTD# INTA# INTB# INTC# Connect one of these pins to pin INTA# of VT8501.
PREQ#	O	Connect to VT8501.
PGNT#	I	Connect to VT8501.
PCKRUN#	IO	Connect to ground with a series 100 ohm resistor if the function is not applied.

CPU INTERFACE		
Signal Name	**I/O**	**Connection**
A20M#	OD	Connect to CPU. 4.7K ohm pull-up to VCC3.
CPURST	OD	Same as the above.
IGNNE#	OD	Same as the above.
INIT	OD	Same as the above.
INTR	OD	Same as the above.
NMI	OD	Same as the above.
SMI#	OD	Same as the above.
STPCLK#	OD	Same as the above.
FERR#	I	Same as the above.
SLP#/GPO7	OD	Connect to Slot-1 CPU only if the function is applied. 4.7K ohm pull-up to VCC3.

ISA BUS INTERFACE		
Signal Name	**I/O**	**Connection**
SA[19:16]	IO	Connect to ISA slots and BIOS ROM. 4.7K ohm pull-up to VCC. Connect SA[19:17] also to LA{19:17}.
SA[15:0]/SDD[15:0]	IO	Connect to ISA slots and BIOS ROM. 4.7K ohm pull-up to VCC. And connected to secondary IDE connector through two 74F245 ICs.
LA[23:20]	IO	Connect to ISA slots. 4.7K ohm pull-up to VCC.
SD[15:0]	IO	Connect to ISA slots and a 74F245 transceiver. 4.7K ohm pull-up to VCC.
SBHE#	IO	Connect to ISA slots. 4.7K ohm pull-up to VCC.
IOR#	IO	Same as the above.
IOW#	IO	Same as the above.
MEMR#	IO	Same as the above.
MEMW#	IO	Same as the above.
SMEMR#	O	Same as the above.
SMEMW	O	Same as the above.
BALE	O	Connect to ISA slots.
IOCS16#	I	Connect to ISA slots. 330 ohm pull-up to VCC.
MCS16#	I	Connect to ISA slots. 330 ohm pull-up to VCC.
IOCHCK#/GPI0	I	Connect to ISA slots. 4.7K ohm pull-up to VCC.
IOCHRDY	I	Connect to ISA slots. 4.7K ohm pull-up to VCC.
RFSH#	IO	Connect to ISA slots. 330 ohm pull-up to VCC.
AEN	O	Connect to ISA slots.
IRQ1/MSCK	I/IO	No connect.
IRQ[5:3]	I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ6/ GPI4/ SLPBTN#	I I I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ7	I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ8#/GPI1	I	No connect.
IRQ[11:9]	I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ12/MSDT	I/IO	No connect.
IRQ[15:14]	I	Connect to ISA slots and IDE connectors. 4.7K ohm pull-up to VCC and 68pF capacitor to ground. Both passive components should be placed near the slots.
DRQ[1:0]	I	Connect to ISA slots. 5.6K ohm pull-down.
DRQ2/ SERIRQ/ GPIOE/ OC1#	I I IO I	Connect to ISA slots. 5.6K ohm pull-down.
DRQ3	I	Connect to ISA slots. 5.6K ohm pull-down.
DRQ[7:5]	I	Connect to ISA slots. 5.6K ohm pull-down.
DACK[1:0]#	O	Connect to ISA slots.
DACK2#/ GPIOF/ OC0#	I IO I	Connect to ISA slots.
DACK3#	I	Connect to ISA slots.
DACK[7:5]	I	Connect to ISA slots.
TC	O	Connect to ISA slots. 68pF capacitor to ground
SPKR	O	Connected to speaker circuitry or AC'97 CODEC through a series 100 ohm resistor. 4.7K ohm pull-up to VCC3 for assigning SDD bus to Audio/Game or 4.7K ohm pull-down for unchanging SDD bus function.

USB INTERFACE		
Signal Name	**I/O**	**Connection**
USBP0+, USBP0-	IO	Connect to USB(0) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
OC0#/ DACK2#/ GPIOF	I I IO	Connect to the corresponding USB(0) over-current detection voltage divider.
USBP1+, USBP1-	IO	Connect to USB(1) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
OC1#/ DRQ2/ GPIOF/ SERIRQ	I I IO I	Connect to the corresponding USB(1) over-current detection voltage divider.
USBP2+, USBP2-	IO	Connect to USB(2) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
USBP3+, USBP3-	IO	Connect to USB(3) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
USBCLK	I	Connect to a 48MHz clock output of the system clock synthesizer.

SYSTEM MANAGEMENT BUS INTERFACE		
Signal Name	**I/O**	**Connection**
SMBCLK, SMBDATA	IO	Connect to all devices on SMBus (I2C bus) except for the VGA port. 2.2K ohm pull-up to VCC3. This resistor value is varied based on the bus loading.
SMBALRT/GPI6	I	10K ohm pull-up to 3VSB (3.3V stand-by power source).

ULTRA DMA-66 ENHANCED IDE INTERFACE		
Signal Name	**I/O**	**Connection**
PDIOR#	O	Connected to primary IDE connector through a 33 ohm series resistor.
PDIOW#	O	Same as the above.
PDDACK#	O	Same as the above.
PDCS1#	O	Same as the above.
PDCS3#	O	Same as the above.
PDA[2:0]	O	Same as the above.
PDDRQ	I	Connected to primary IDE connector through a 33 ohm series resistor. 5.6K ohm pull-down on the connector side of the series resistor.
PDRDY#	I	Connected to primary IDE connector through a 33 ohm series resistor. 1K ohm pull-up to VCC on the connector side of the series resistor.
DD[15:0] /PDD[15:0]	IO	Connected to primary IDE connector through 33 ohm series resistors or also connected to secondary IDE connector through 33 ohm series resistors if SPKR is pulled up to VCC3. 10K ohm pull-down on the VT82C686A side of the series resistor.
SDIOR#	O	Connected to secondary IDE connector through a 33 ohm series resistor.
SDIOW#	O	Same as the above.
SDDACK#	O	Same as the above.
SDCS1#	O	Same as the above.
SDCS3#	O	Same as the above.
SDA[2:0]	O	Same as the above.
SDDRQ	I	Connected to secondary IDE connector through a 33 ohm series resistor. 5.6K ohm pull-down on the connector side of the series resistor.
SDRDY#	I	Connected to secondary IDE connector through a 33 ohm series resistor. 1K ohm pull-up to VCC on the connector side of the series resistor.
SDD15/MSI **SDD14**/MSO **SDD13**/JBB1 **SDD12**/JBB2 **SDD11**/JAB1 **SDD10**/JAB2 **SDD9**/JAX **SDD8**/JAY **SDD7**/JBX **SDD6**/JBY **SDD5**/ACRST **SDD4**/SDOUT **SDD3**/SYNC **SDD2**/SDIN2 **SDD1**/SDIN **SDD0**/BITCLK	IO/I IO/O IO/I IO/I IO/I IO/I IO/I IO/I IO/I IO/I IO/O IO/O IO/O IO/I IO/I IO/I	Connected to secondary IDE connector through 33 ohm series resistors when pin SPEAK is strapped to low. Otherwise, Connected to Audio/Game port instead when pin SPEAK is strapped to high.

PARALLEL PORT INTERFACE		
Signal Name	**I/O**	**Connection**
PD[7:0]	IO	Connect to the printer connector. 4.7K ohm pull-up to VCC and a 180pF decoupling capacitor to ground. These passive components should be placed near the connector.
AUTOFD#	IO	Same as the above.
PINIT#	IO	Same as the above.
SLCTIN#	IO	Same as the above.
STROBE#	IO	Same as the above.
ACK#	I	Same as the above.
BUSY	I	Same as the above.
ERROR#	I	Same as the above.
PE	I	Same as the above.
SLCT	I	Same as the above.

FLOPPY DISK INTERFACE		
Signal Name	**I/O**	**Connection**
DRVEN0	OD	Connect to primary floppy drive connector.
DRVEN1	OD	Connect to secondary floppy drive connector if it is installed. Otherwise, no connect.
DIR#	OD	Connect to the floppy drive connector.
DS0#	OD	Same as the above.
DS1#	OD	Same as the above.
HDSEL#	OD	Same as the above.
MTR0#	OD	Same as the above.
MTR1#	OD	Same as the above.
STEP#	OD	Same as the above.
WDATA	OD	Same as the above.
WGATE#	OD	Same as the above.
DSKCHG#	I	Connect to the floppy drive connector. 1K ohm pull-up to VCC.
INDEX#	I	Same as the above.
RDATA#	I	Same as the above.
TRK00#	I	Same as the above.
WRTPRT#	I	Same as the above.

SERIAL PORTS AND INFRARED INTERFACE		
Signal Name	**I/O**	**Connection**
TXD1	O	Connected to a corresponding 9-pin serial connector (usually COM1) through a serial RS232 interface buffer and a 330pF decoupling capacitor to ground.
RXD1	I	Same as the above.
RTS1#	O	Same as the above.
CTS1#	I	Same as the above.
DTR1#	O	Same as the above.
DSR1#	I	Same as the above.
DCD1#	I	Same as the above.
RI1#	I	Same as the above.
TXD2	O	Connected to a corresponding 9-pin serial connector (usually COM2) through a serial RS232 interface buffer and a 330pF decoupling capacitor to ground.
RXD2	I	Same as the above.
RTS2#	O	Same as the above.
CTS2#	I	Same as the above.
DTR2#	O	Same as the above.
DSR2#	I	Same as the above.
DCD2#	I	Same as the above.
RI2#	I	Same as the above.
IRTX/GPO14	O	Connect to an Infrared connector. 4.7K ohm pull-up to VCC.
IRRX/GPO15	IO	Connect to an Infrared connector.

SERIAL IRQ		
Signal Name	**I/O**	**Connection**
SERIRQ/ GPIOE/ OC1# DRQ2	I IO I I	4.7K ohm pull-up to VCC3.

INTERNAL KEYBOARD CONTROLLER		
Signal Name	**I/O**	**Connection**
KBCK/A20GATE	IO/I	Connected to a keyboard connector through a 4.7K ohm pull-up to VCC, a 47pF capacitor to ground, and a series ferrite bead.
KBDT/KBRC	IO/I	Same as the above.
MSCK/IRQ1	IO/I	Connected to a mouse connector through a 4.7K ohm pull-up to VCC, a 47pF capacitor to ground, and a series ferrite bead.
MSDT/IRQ12	IO/I	Same as the above.

GENERAL PURPOSE INPUTS		
Signal Name	**I/O**	**Connection**
GPI0/IOCHCK#	I	4.7K ohm pull-up to VCC3 if no multiplexed function is applied.
GPI1/IRQ8#	I	10K ohm pull-up to 3VSB if its function is applied. Same, if not applied.
GPI2/BATLOW#	I	4.7K ohm pull-up to VCC3 if no multiplexed function is applied.
GPI3/LID	I	Same as the above.
GPI4/IRQ6/SLPBTN#	I	Same as the above.
GPI5/PME#/THRM	I	Same as the above.
GPI6/SMBALRT#	I	Same as the above.
GPI7/RING#	I	Same as the above.
GPI8/GPO8/GPIOA/ GPOWE#	IO	Same as the above.
GPI9/GPO9/GPIOB/ FAN2	IO	Same as the above.
GPI10/GPO10/GPIOC/ CHAS	IO	Same as the above.
GPI11/GPO11/ GPIOD	IO	Same as the above.

GENERAL PURPOSE OUTPUTS		
Signal Name	**I/O**	**Connection**
GPO0	O	10K ohm pull-up to 3VSB if its function is applied. Otherwise, no connect.
GPO1/SUSA#	IO	No connect if no multiplexed function is applied.
GPO2/SUSB#	IO	Same as the above.
GPO3/SDD2/SDIN2	O	Same as the above.
GPO4/CPUSTP#	O	Same as the above.
GPO5/PCISTP#	O	Same as the above.
GPO6/SUSST1#	O	Same as the above.
GPO7/SLP#	IO	Same as the above.
GPO8/GP18/GPIOA/ GPOWE#	IO	Same as the above.
GPO9/GPI9/GPIOB/ FAN2	IO	Same as the above.
GPO10/GPI10/GPIOC/ CHAS	IO	Same as the above.
GPO11/GPI11/GPIOD	IO	Same as the above.
GPO12/XDIR/PCS0#	O	Same as the above.
GPO13/SOE#/MCCS#	O	Same as the above.
GPO14/IRTX	O	Same as the above.
GPO15/IRRX	IO	Same as the above.
GPOWE#/GPIOA/ GPIO8	IO	Same as the above.

GENERAL PURPOSE I/O		
Signal Name	**I/O**	**Connection**
GPIOA(GPIO8)	IO	4.7K ohm pull-up to VCC3 if no multiplexed function is applied.
GPIOB(GPIO9)/FAN2	IO	Same as the above.
GPIOC(GPIO10)/ CHAS	IO	Same as the above.
GPIOD(GPIO11)	IO	Same as the above.
GPIOE/ OC1/ SERIRQ/ DRQ2	IO I I I	Same as the above.
GPIOF/ OC0/ DACK2#	IO I I	Same as the above.

HARDWARE MONITORING		
Signal Name	**I/O**	**Connection**
VSENS1	I	Connected to a monitored voltage (usually VCC2) through a voltage divider circuitry.
VSENS2	I	Connected to a monitored voltage (usually 2.5V) through a voltage divider circuitry.
VSENS3	I	Connected to a monitored voltage (usually VCC) through a voltage divider circuitry.
VSENS4	I	Connected to a monitored voltage (usually +12V) through a voltage divider circuitry.
TMPSENS1	I	Connect to a thermister that is near the sensed component or device.
TMPSENS2	I	Same as the above.
VREF	P	Connected to each thermister through a 10K ohm (1%) series resistor.
FAN1	I	Connect to a fan tachometer output
FAN2/GPIOB(GPIO9)	IO	Same as the above.
CHAS/GPIOC(GPIO10)	IO	Connect to chassis intrusion circuitry.

XD INTERFACE		
Signal Name	**I/O**	**Connection**
XDIR/PCS0#/GPO12	O	Connect to the direction control of a 74F245 transceiver that buffers the X-Bus data and ISA Bus data.
SOE#/MCCS#/GPO13	O	Connect to the output enable control of two 74F245 transceivers that buffers the secondary IDE data bus data and ISA address bus when the audio function is enabled.

CHIP SELECTS		
Signal Name	**I/O**	**Connection**
PCS0#/GPO12/XDIR	**O**	Connect to addressed devices which drive data to the SD pins if XDIR and SOE# are disabled and the X-Bus is not implemented.
MCCS#/GPO13/SOE#	**O**	Connect to the chip enable control of a micro-controller chip if XDIR and SOE# are disabled and the X-Bus is not implemented.
ROMCS#/KBCS#	**O**	Connect to the chip enable control of BIOS ROM. 4.7K ohm pull-down for Socket-7 configuration or 4.7K ohm pull-up to VCC3 for Slot-1 configuration.

POWER MANAGEMENT		
Signal Name	**I/O**	**Connection**
PME#/THRM/GPI5	**I**	10K ohm pull-up to 3VSB if the function is not applied.
PWRBTN#	**I**	Connect to Power Button circuitry.
SLPBTN#/IRQ6/GPI4	**I**	10K ohm pull-up to VCC3 if the function is not applied.
RSMRST	**I**	Connect to Resume Reset circuitry.
EXTSMI#	**IOD**	10K ohm pull-up to 3VSB if the function is not applied.
SMBALRT#/GPI6	**I**	10K ohm pull-up to 3VSB if the function is not applied.
LID/GP13	**I**	10K ohm pull-up to 3VSB if the function is not applied.
RING#/GP17	**I**	Connected to external modem circuitry to allow the system to be re-activated by a received phone call. 10K ohm pull-up to 3VSB.
BATLOW#/GP12	I	10K ohm pull-up to 3VSB if the function is not applied.
CPUSTP#/GPO4	**O**	Connect to the system clock synthesizer to disable the CPU clock outputs if the function is applied. Otherwise, no connect.
PCISTP#/GPO5	**O**	Connect to the system clock synthesizer to disable the PCI clock outputs if the function is applied. Otherwise, no connect.
SUSA#/GPO1	**O**	10K ohm pull-up to 3VSB if the function is not applied.
SUSB#/GPO2	**O**	10K ohm pull-up to 3VSB if the function is not applied.
SUSC#	**O**	Connect to ATX Power On circuitry.
SUSST1#/GPO6	**O**	Connect to VT8501. 10K ohm pull-up to 3VSB.
SUSCLK	**O**	10K ohm pull-up to 3VSB

RESET AND CLOCKS		
Signal Name	**I/O**	**Connection**
PWRGD	I	Connect to VT8501 and Power Good circuitry.
PCIRST#	O	Connect to PCI slots and PCI devices.
RSTDRV	O	Connected to VT8501 and IDE connectors through a 74F240 inverter IC. And direct connect to ISA slots not through inverter.
OSC	I	Connect to the 14.318MHz clock output of the system clock synthesizer.
BCLK	O	Connected to ISA slots through corresponding 33 ohm series resistors.
RTCX1	I	Connect to a 32.768KHz (RTC) crystal circuitry.
RTCX2	O	Connect to a 32.768KHz (RTC) crystal circuitry.

POWER AND GROUND		
Signal Name	**I/O**	**Connection**
VCC	P	Connect to VCC3.
VCCSUS	P	Connect to 3VSB.
VCCHWM	P	Connected to VCC3 through a ferrite bead.
GNDHWM	P	Connected to ground through a ferrite bead.
VCCUSB	P	Connected to VCC3 through a ferrite bead.
GNDUSB	P	Connected to ground through a ferrite bead.
VBAT	P	Connect to battery circuitry.
GND	P	Connect to digital ground

APPENDICES

The following schematics are provides "as is" with no warranties whatsoever, including any warranty of merchantability, fitness of any particular purpose, or any warranty otherwise arising out of proposal, specification or sample. No license, express or implied, by estoppel or otherwise, to any intellectual property rights are granted herein. VIA Technologies, Inc. disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. VIA Technologies, Inc. does not warrant or represent that such use will not infringe such rights. Third-party brands and names are the property of their respective owners.

Appendix A - Apollo MVP4 Reference Design Schematics

Appendix B - TMDS Transmitter Reference Design Schematic

Appendix C - VIA AC'97 CODEC Reference Design Schematic

Appendix D - TV Decoder Reference Design Schematic

Appendix E - TV Encoder Reference Design Schematic

Appendix F - Application Circuits of SPKR Strapping

Appendix A - Apollo MVP4 Reference Design Schematics

Apollo MVP4 Reference design schematics are shown in the following 16 pages. The component placement for this reference design is shown in Figure A-1. The system specification for this motherboard design is listed below:

- Single Socket 7 CPU (66-100MHz)
- MVP4 single chip clock synthesizer
- Apollo MVP4 North Bridge (Host/PCI) Controller (VT8501)
- 512KB L2 Cache & 32KB Tag RAM
- Three DIMM Slots (maximum 768MB and 100MHz memory frequency)
- One CRT Interface (support of non-interlaced 1280x1024x64K, 1024x768x16M, 800x600x16M, and 640x480x16M)
- One board-to-board for Video Capture and TV Out Interfaces
- Three PCI Slots (30-33MHz)
- One ISA Slot
- One 2MB Flash ROM
- One AC'97 Link Controller (to cooperate with a AC'97 Codec chip)
- Four Universal Serial Bus Ports
- PS2 Keyboard/Mouse Support
- Two Enhanced IDE Interfaces
- One Floppy Drive Interface
- One Infrared Interface
- Various Hardware Monitoring (support 5 positive voltage, 3 temperature, and 2 fan-speed monitoring)
- One parallel Port and Two Serial Ports
- One MIDI/GAME Port

VIA MVP4 Reference Schematics
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SOCKET-7 PROCESSOR	2
NORTH BRIDGE VT8501 (MVP4)	3,4
SOUTH BRIDGE VT82C686A	5,6
CLOCK SYNTHESIZER	7
L2 CACHE & TAG RAM & WAKE UP	8
DRAM	9
PCI SLOTS	10
ISA SLOTS & SYSTEM ROM	11
IDE CONNECTORS	12
FRONT PANEL & BACK PANEL	13
AC97 AUDIO CODEC & AUDIO PORTS	14
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AT & ATX POWER CONNECTORS & BYPASS CAPACITORS	16

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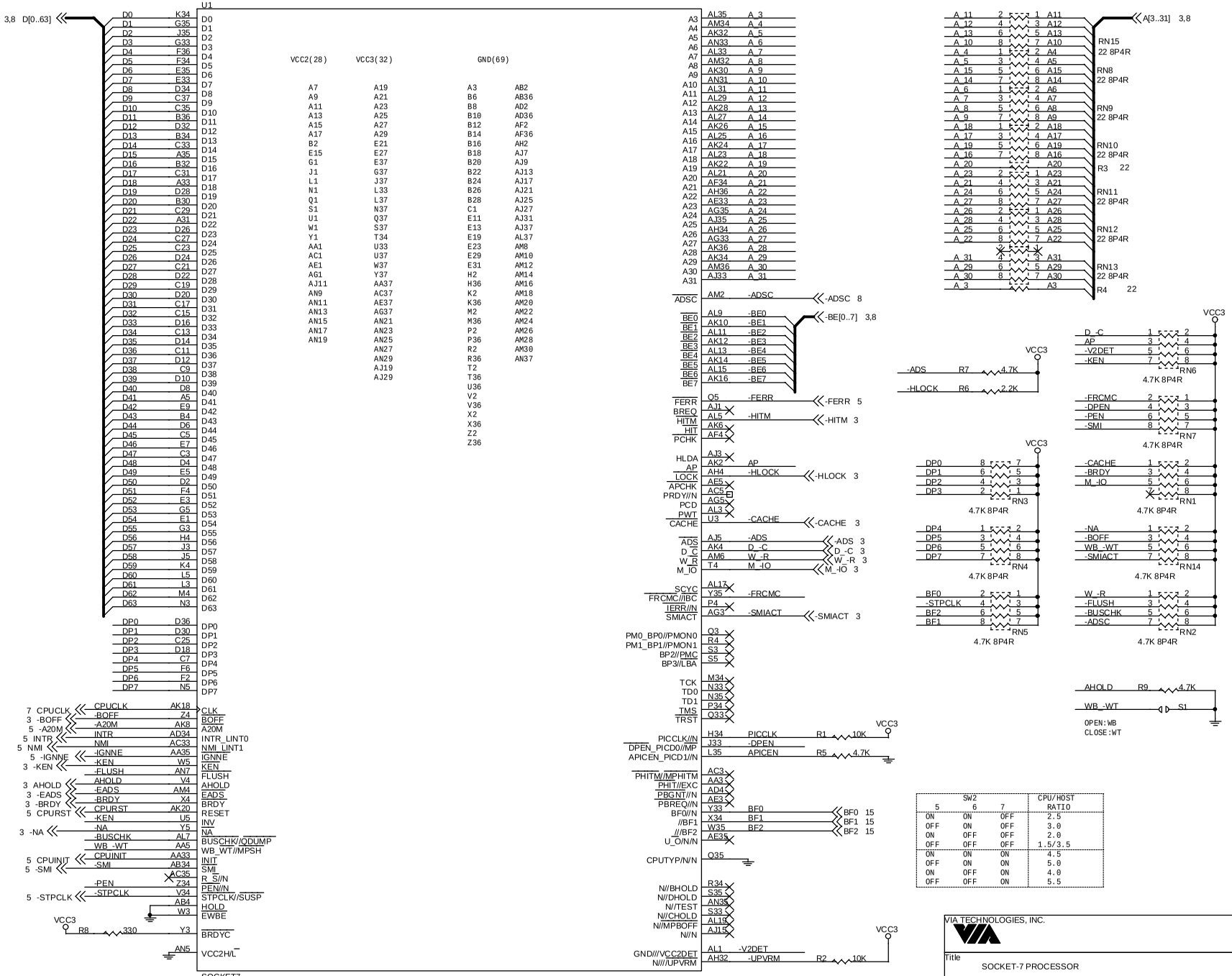
U1
SOCKET7
VCC2(28)
VCC3(32)
GND(69)
3,8 D[0..63]
D0 K34
D1 G35
D2 J35
D3 G33
D4 F36
D5 F34
D6 E35
D7 E33
D8 D34
D9 C37
D10 C35
D11 B36
D12 D32
D13 B34
D14 C33
D15 A35
D16 B32
D17 C31
D18 A33
D19 D28
D20 B30
D21 C29
D22 A31
D23 D26
D24 C27
D25 C23
D26 D24
D27 C21
D28 D22
D29 C19
D30 D20
D31 C17
D32 C15
D33 D16
D34 C13
D35 D14
D36 C11
D37 D12
D38 C9
D39 D10
D40 D8
D41 A5
D42 E9
D43 B4
D44 D6
D45 C5
D46 E7
D47 C3
D48 D4
D49 E5
D50 D2
D51 F4
D52 E3
D53 G5
D54 E1
D55 G3
D56 H4
D57 J3
D58 J5
D59 K4
D60 L5
D61 L3
D62 M4
D63 N3
DP0 D36
DP1 D30
DP2 C25
DP3 D18
DP4 C7
DP5 F6
DP6 F2
DP7 N5
7 CPUCLK CPUCLK AK18 CLK
3 -BOFF -BOFF Z4 BOFF
5 -A20M -A20M AK8 A20M
5 INTR INTR AD34 INTR_LINT0
5 NMI NMI AC33 NMI_LINT1
5 -IGNNE -IGNNE AA35 IGNNE
3 -KEN -KEN W5 KEN
-FLUSH AN7 FLUSH
3 AHOLD AHOLD V4 AHOLD
3 -EADS -EADS AM4 EADS
3 -BRDY -BRDY X4 BRDY
5 CPURST CPURST AK20 RESET
-KEN U5 INV
3 -NA -NA Y5 NA
-BUSCHK AL7 BUSCHK/IQDUMP
WB_-WT AA5 WB_WT//MPSH
5 CPUINIT CPUINIT AA33 INIT
5 -SMI -SMI AB34 SMI
AC35 R_S//N
-PEN Z34 PEN//N
5 -STPCLK -STPCLK V34 STPCLK//SUSP
AB4 HOLD
W3 EWBE
VCC3
R8 330 Y3 BRDYC
AN5 VCC2H/L
A7 A19 A3 AB2
A9 A21 B6 AB36
A11 A23 B8 AD2
A13 A25 B10 AD36
A15 A27 B12 AF2
A17 A29 B14 AF36
B2 E21 B16 AH2
E15 E27 B18 AJ7
G1 E37 B20 AJ9
J1 G37 B22 AJ13
L1 J37 B24 AJ17
N1 L33 B26 AJ21
Q1 L37 B28 AJ25
S1 N37 C1 AJ27
U1 Q37 E11 AJ31
W1 S37 E13 AJ37
Y1 T34 E19 AL37
AA1 U33 E23 AM8
AC1 U37 E29 AM10
AE1 W37 E31 AM12
AG1 Y37 H2 AM14
AJ11 AA37 H36 AM16
AN9 AC37 K2 AM18
AN11 AE37 K36 AM20
AN13 AG37 M2 AM22
AN15 AN21 M36 AM24
AN17 AN23 P2 AM26
AN19 AN25 P36 AM28
AN27 R2 AM30
AN29 R36 AN37
AJ19 T2
AJ29 T36
U36
V2
V36
X2
X36
Z2
Z36
A3 AL35 A_3
A4 AM34 A_4
A5 AK32 A_5
A6 AN33 A_6
A7 AL33 A_7
A8 AM32 A_8
A9 AK30 A_9
A10 AN31 A_10
A11 AL31 A_11
A12 AL29 A_12
A13 AK28 A_13
A14 AL27 A_14
A15 AK26 A_15
A16 AL25 A_16
A17 AK24 A_17
A18 AL23 A_18
A19 AK22 A_19
A20 AL21 A_20
A21 AF34 A_21
A22 AH36 A_22
A23 AE33 A_23
A24 AG35 A_24
A25 AJ35 A_25
A26 AH34 A_26
A27 AG33 A_27
A28 AK36 A_28
A29 AK34 A_29
A30 AM36 A_30
A31 AJ33 A_31
ADSC AM2 -ADSC -ADSC 8
BE0 AL9 -BE0
BE1 AK10 -BE1
BE2 AL11 -BE2
BE3 AK12 -BE3
BE4 AL13 -BE4
BE5 AK14 -BE5
BE6 AL15 -BE6
BE7 AK16 -BE7
-BE[0..7] 3,8
FERR Q5 -FERR -FERR 5
BREQ AJ1
HITM AL5 -HITM -HITM 3
HIT AK6
PCHK AF4
HLDA AJ3
AP AK2 AP
LOCK AH4 -HLOCK -HLOCK 3
APCHK AE5
PRDY//N AC5
PCD AG5
PWT AL3
CACHE U3 -CACHE -CACHE 3
ADS AJ5 -ADS -ADS 3
D_C AK4 D_-C D_-C 3
W_R AM6 W_-R W_-R 3
M_IO T4 M_-IO M_-IO 3
SCYC AL17
FRCMC//IBC Y35 -FRCMC
IERR//N P4
SMIACT AG3 -SMIACT -SMIACT 3
PM0_BP0//PMON0 Q3
PM1_BP1//PMON1 R4
BP2//PMC S3
BP3/LBA S5
TCK M34
TD0 N33
TD1 N35
TMS P34
TRST Q33
PICCLK//N H34 PICCLK R1 10K VCC3
DPEN_PICD0//MP J33 -DPEN
APICEN_PICD1//N L35 APICEN R5 4.7K
PHITM//MPHITM AC3
PHIT//EXC AA3
PBGNT//N AD4
PBREQ//N AE3
BF0//N Y33 BF0 BF0 15
//BF1 X34 BF1 BF1 15
//BF2 W35 BF2 BF2 15
U_O/N/N AE35
CPUTYP/N/N Q35
N//BHOLD R34
N//DHOLD S35
N//TEST AN3
N//CHOLD S33
N//MPBOFF AL13
N//N AJ15 VCC3
GND///VCC2DET AL1 -V2DET
N///UPVRM AH32 -UPVRM R2 10K
A_11 2 1 A11
A_12 4 3 A12
A_13 6 5 A13
A_10 8 7 A10
RN15 22 8P4R
A_4 1 2 A4
A_5 3 4 A5
A_15 5 6 A15
RN8 22 8P4R
A_14 7 8 A14
A_6 1 2 A6
A_7 3 4 A7
A_8 5 6 A8
RN9 22 8P4R
A_9 7 8 A9
A_18 1 2 A18
A_17 3 4 A17
A_19 5 6 A19
RN10 22 8P4R
A_16 7 8 A16
A_20 A20
R3 22
A_23 2 1 A23
A_21 4 3 A21
A_24 6 5 A24
RN11 22 8P4R
A_27 8 7 A27
A_26 2 1 A26
A_28 4 3 A28
A_25 6 5 A25
RN12 22 8P4R
A_22 8 7 A22
A_31 4 3 A31
A_29 6 5 A29
RN13 22 8P4R
A_30 8 7 A30
A_3 A3
R4 22
A[3..31] 3,8
VCC3
-ADS R7 4.7K
-HLOCK R6 2.2K
DP0 8 7
DP1 6 5
DP2 4 3
DP3 2 1
RN3 4.7K 8P4R
DP4 1 2
DP5 3 4
DP6 5 6
DP7 7 8
RN4 4.7K 8P4R
BF0 2 1
-STPCLK 4 3
BF2 6 5
BF1 8 7
RN5 4.7K 8P4R
D_-C 1 2
AP 3 4
-V2DET 5 6
-KEN 7 8
RN6 4.7K 8P4R
-FRCMC 2 1
-DPEN 4 3
-PEN 6 5
-SMI 8 7
RN7 4.7K 8P4R
-CACHE 1 2
-BRDY 3 4
M_-IO 5 6
RN1 4.7K 8P4R
-NA 1 2
-BOFF 3 4
WB_-WT 5 6
-SMIACT 7 8
RN14 4.7K 8P4R
W_-R 1 2
-FLUSH 3 4
-BUSCHK 5 6
-ADSC 7 8
RN2 4.7K 8P4R
AHOLD R9 4.7K
WB_-WT S1
OPEN:WB
CLOSE:WT
SW2
5 6 7 CPU/HOST RATIO
ON ON OFF 2.5
OFF ON OFF 3.0
ON OFF OFF 2.0
OFF OFF OFF 1.5/3.5
ON ON ON 4.5
OFF ON ON 5.0
ON OFF ON 4.0
OFF OFF ON 5.5
VIA TECHNOLOGIES, INC.
Title
SOCKET-7 PROCESSOR
Size C
Document Number VIA Apollo MVP4
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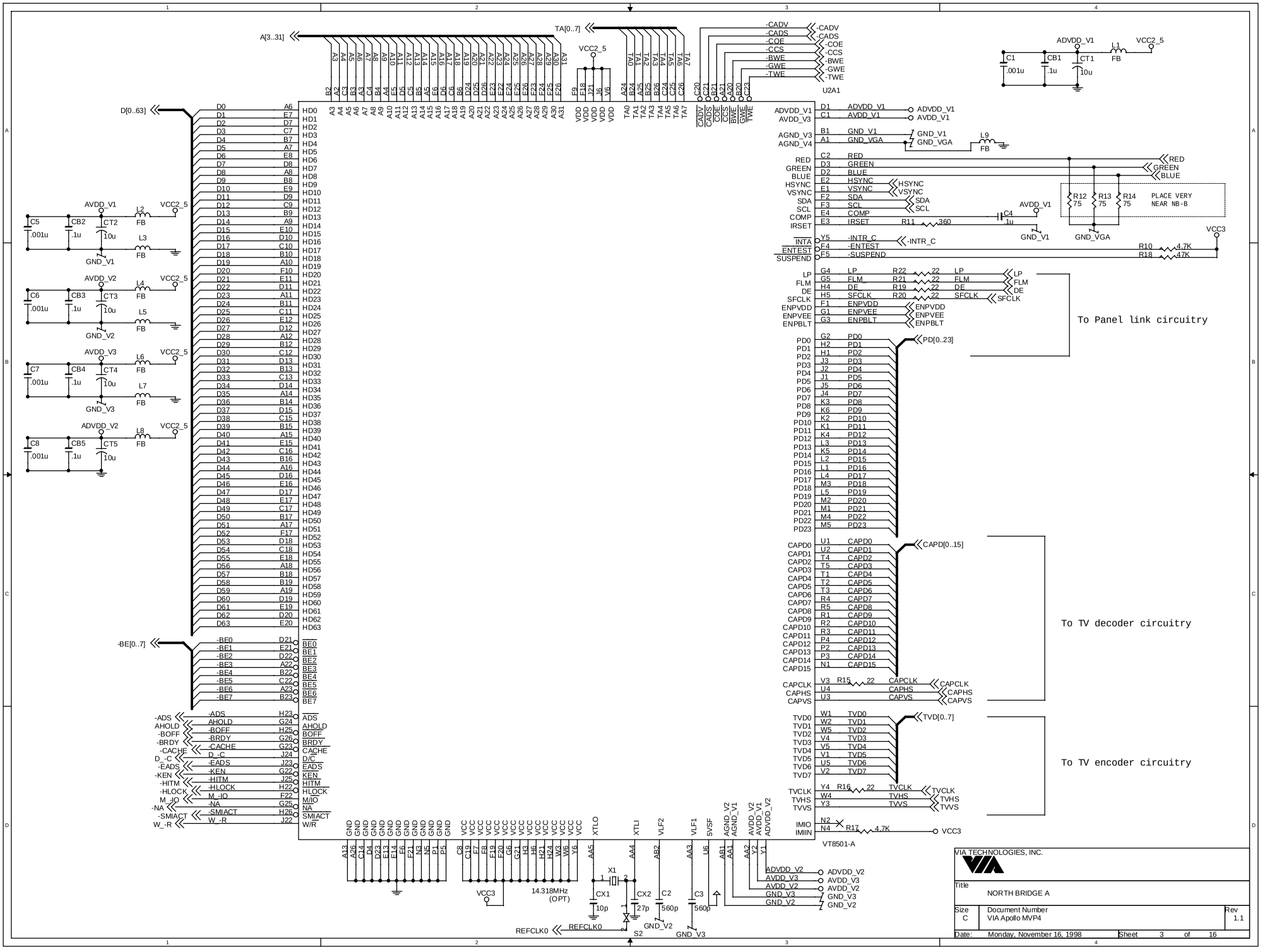
A[3..31]
TA[0..7]
-CADV
-CADS
-COE
-CCS
-BWE
-GWE
-TWE
U2A1
D[0..63]
-BE[0..7]
-ADS
AHOLD
-BOFF
-BRDY
-CACHE
D_-C
-EADS
-KEN
-HITM
-HLOCK
M_-IO
-NA
-SMIACT
W_-R
AVDD_V1
AVDD_V2
AVDD_V3
VCC2_5
VCC3
GND_V1
GND_V2
GND_V3
GND_VGA
L1
L2
L3
L4
L5
L6
L7
L8
L9
FB
C1
.001u
CB1
.1u
CT1
10u
CB2
CT2
C5
CB3
CT3
C6
CB4
CT4
C7
CB5
CT5
C8
RED
GREEN
BLUE
HSYNC
VSYNC
SDA
SCL
COMP
IRSET
R11
360
C4
R12
75
R13
R14
PLACE VERY
NEAR NB-B
-INTA
-ENTEST
-SUSPEND
R10
4.7K
R18
LP
FLM
DE
SFCLK
ENPVDD
ENPVEE
ENPBLT
R22
R21
R19
R20
22
To Panel link circuitry
PD[0..23]
CAPD[0..15]
To TV decoder circuitry
CAPCLK
CAPHS
CAPVS
R15
TVD[0..7]
To TV encoder circuitry
TVCLK
TVHS
TVVS
R16
IMIO
IMIIN
R17
VT8501-A
X1
14.318MHz
(OPT)
CX1
10p
CX2
27p
C2
560p
C3
560p
REFCLK0
S2
VIA TECHNOLOGIES, INC.
Title
NORTH BRIDGE A
Size
C
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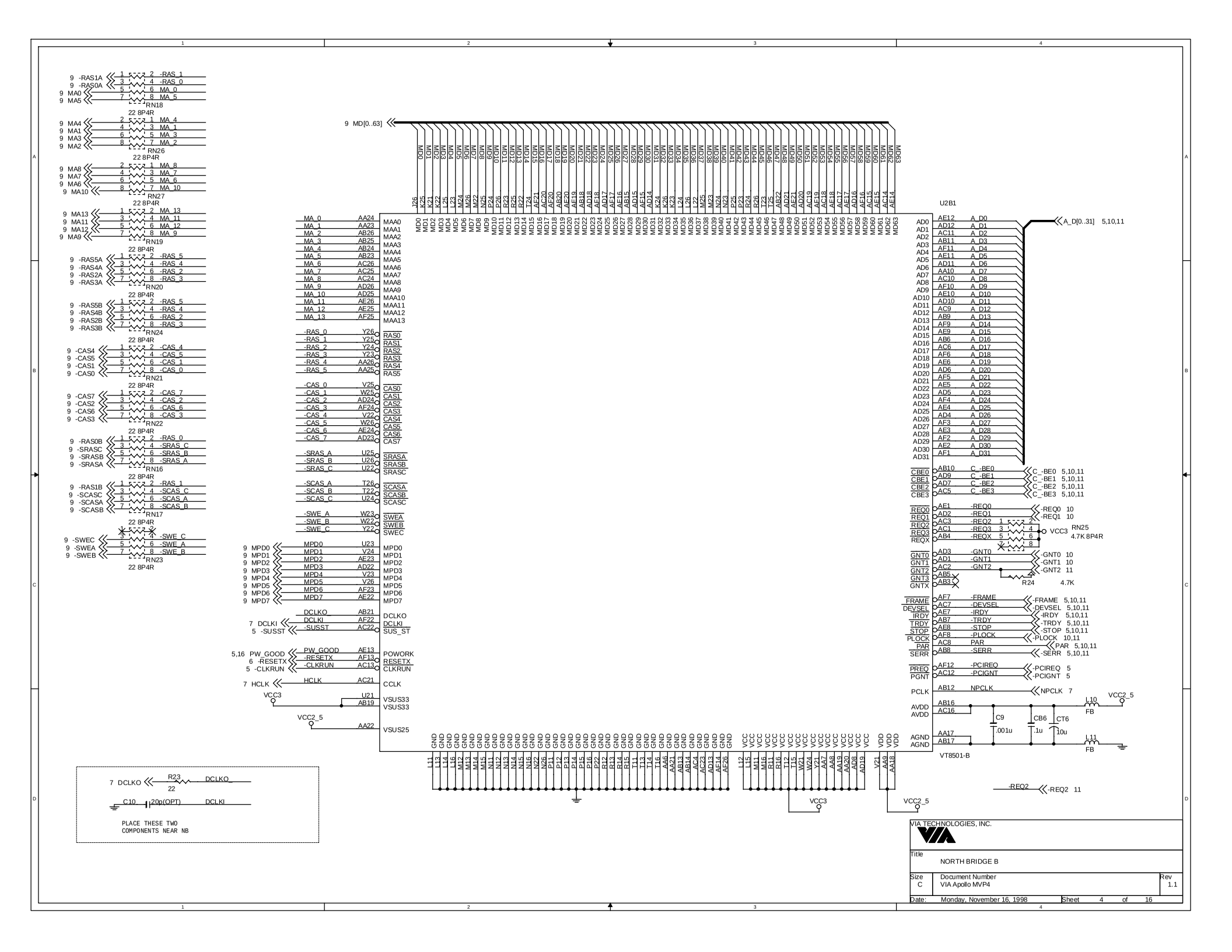
9 -RAS1A
9 -RAS0A
9 MA0
9 MA5
-RAS_1
-RAS_0
MA_0
MA_5
RN18
22 8P4R
9 MA4
9 MA1
9 MA3
9 MA2
MA_4
MA_1
MA_3
MA_2
RN26
9 MA8
9 MA7
9 MA6
9 MA10
MA_8
MA_7
MA_6
MA_10
RN27
9 MA13
9 MA11
9 MA12
9 MA9
MA_13
MA_11
MA_12
MA_9
RN19
9 -RAS5A
9 -RAS4A
9 -RAS2A
9 -RAS3A
-RAS_5
-RAS_4
-RAS_2
-RAS_3
RN20
9 -RAS5B
9 -RAS4B
9 -RAS2B
9 -RAS3B
RN24
9 -CAS4
9 -CAS5
9 -CAS1
9 -CAS0
-CAS_4
-CAS_5
-CAS_1
-CAS_0
RN21
9 -CAS7
9 -CAS2
9 -CAS6
9 -CAS3
-CAS_7
-CAS_2
-CAS_6
-CAS_3
RN22
9 -RAS0B
9 -SRASC
9 -SRASB
9 -SRASA
-SRAS_C
-SRAS_B
-SRAS_A
RN16
9 -RAS1B
9 -SCASC
9 -SCASA
9 -SCASB
-SCAS_C
-SCAS_A
-SCAS_B
RN17
9 -SWEC
9 -SWEA
9 -SWEB
-SWE_C
-SWE_A
-SWE_B
RN23
9 MD[0..63]
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
RAS0
RAS1
RAS2
RAS3
RAS4
RAS5
CAS0
CAS1
CAS2
CAS3
CAS4
CAS5
CAS6
CAS7
SRASA
SRASB
SRASC
SCASA
SCASB
SCASC
SWEA
SWEB
SWEC
MPD0
MPD1
MPD2
MPD3
MPD4
MPD5
MPD6
MPD7
DCLKO
DCLKI
SUS_ST
POWORK
RESETX
CLKRUN
CCLK
VSUS33
VSUS25
7 DCLKI
5 -SUSST
5,16 PW_GOOD
6 -RESETX
5 -CLKRUN
7 HCLK
VCC3
VCC2_5
U2B1
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
A_D0
A_D1
A_D2
A_D3
A_D4
A_D5
A_D6
A_D7
A_D8
A_D9
A_D10
A_D11
A_D12
A_D13
A_D14
A_D15
A_D16
A_D17
A_D18
A_D19
A_D20
A_D21
A_D22
A_D23
A_D24
A_D25
A_D26
A_D27
A_D28
A_D29
A_D30
A_D31
A_D[0..31] 5,10,11
CBE0
CBE1
CBE2
CBE3
C_-BE0 5,10,11
C_-BE1 5,10,11
C_-BE2 5,10,11
C_-BE3 5,10,11
REQ0
REQ1
REQ2
REQ3
REQX
-REQ0 10
-REQ1 10
-REQ2 1
-REQ3 3
-REQX 5
VCC3
RN25
4.7K 8P4R
GNT0
GNT1
GNT2
GNT3
GNTX
-GNT0 10
-GNT1 10
-GNT2 11
R24
4.7K
FRAME
DEVSEL
IRDY
TRDY
STOP
PLOCK
PAR
SERR
-FRAME 5,10,11
-DEVSEL 5,10,11
-IRDY 5,10,11
-TRDY 5,10,11
-STOP 5,10,11
-PLOCK 10,11
PAR 5,10,11
-SERR 5,10,11
PREQ
PGNT
-PCIREQ 5
-PCIGNT 5
PCLK
NPCLK 7
AVDD
AGND
VCC2_5
L10
FB
C9
.001u
CB6
.1u
CT6
10u
L11
FB
VT8501-B
-REQ2
-REQ2 11
7 DCLKO
R23
22
DCLKO_
C10
20p(OPT)
DCLKI
PLACE THESE TWO
COMPONENTS NEAR NB
VIA TECHNOLOGIES, INC.
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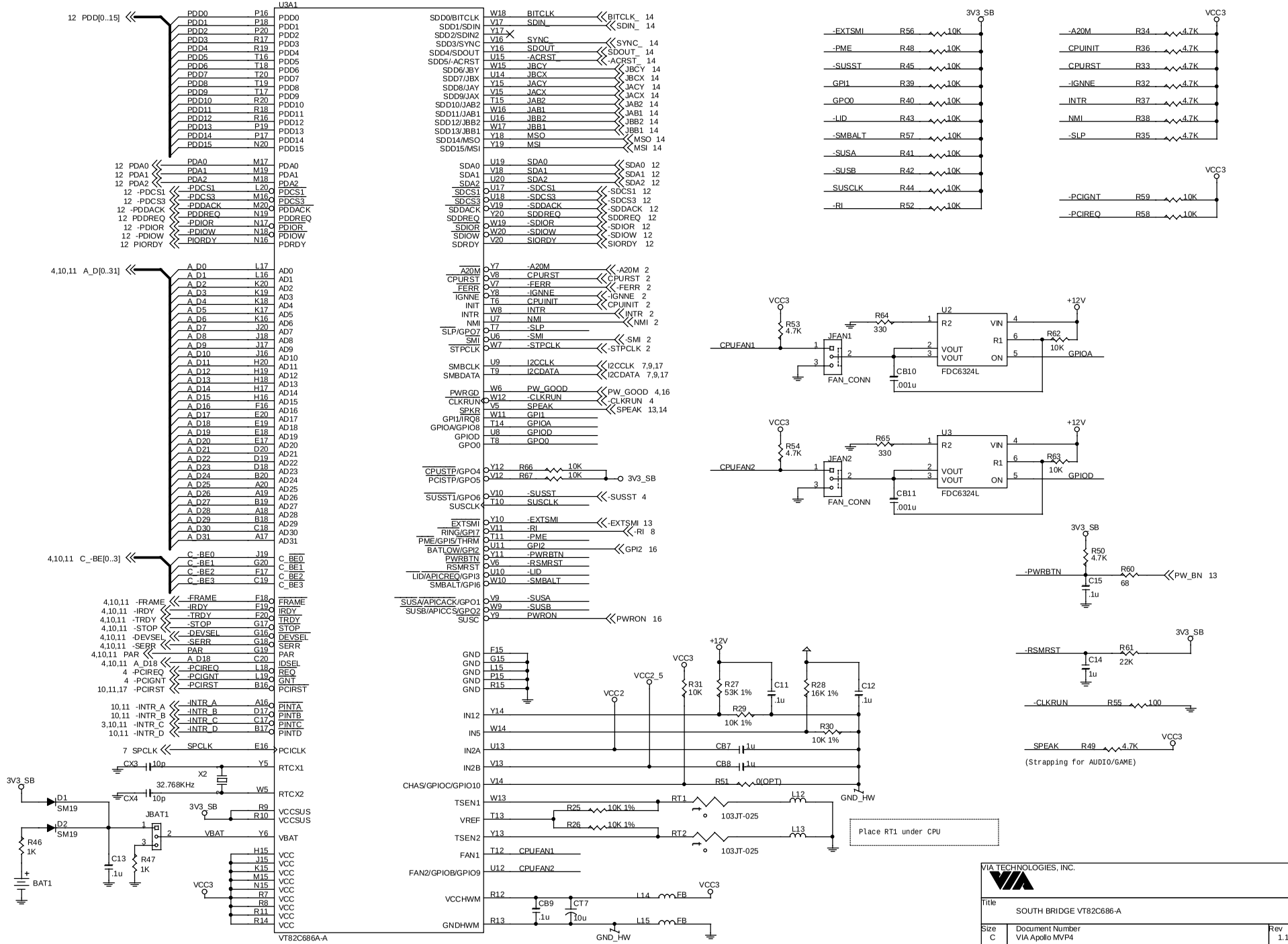
U3A1
VT82C686A-A
Place RT1 under CPU
(Strapping for AUDIO/GAME)
VIA TECHNOLOGIES, INC.
Title
SOUTH BRIDGE VT82C686-A
Size
C
Document Number
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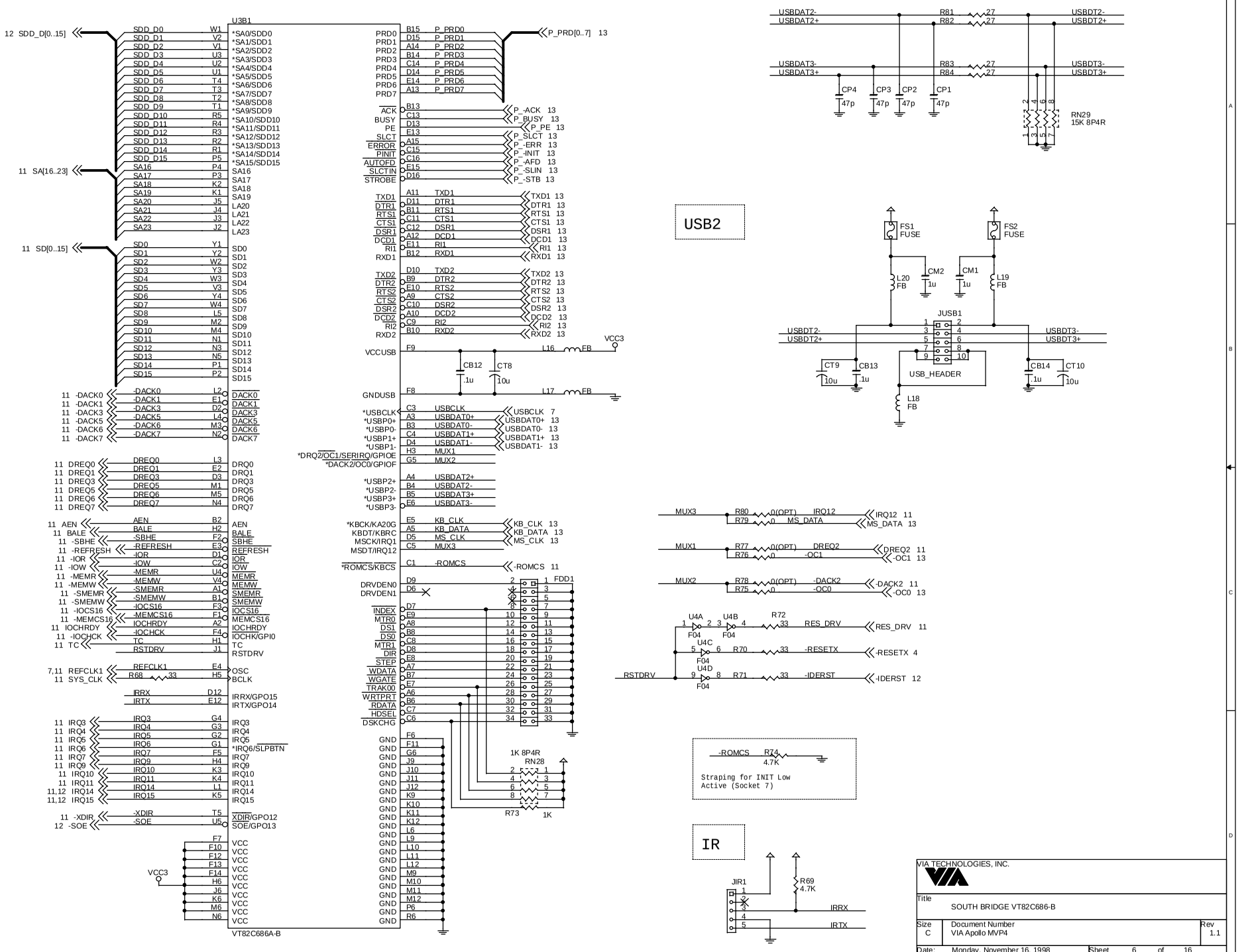
U3B1
VT82C686A-B
12 SDD_D[0..15]
11 SA[16..23]
11 SD[0..15]
SDD_D0 W1
SDD_D1 V2
SDD_D2 V1
SDD_D3 U3
SDD_D4 U2
SDD_D5 U1
SDD_D6 T4
SDD_D7 T3
SDD_D8 T2
SDD_D9 T1
SDD_D10 R5
SDD_D11 R4
SDD_D12 R3
SDD_D13 R2
SDD_D14 R1
SDD_D15 P5
*SA0/SDD0
*SA1/SDD1
*SA2/SDD2
*SA3/SDD3
*SA4/SDD4
*SA5/SDD5
*SA6/SDD6
*SA7/SDD7
*SA8/SDD8
*SA9/SDD9
*SA10/SDD10
*SA11/SDD11
*SA12/SDD12
*SA13/SDD13
*SA14/SDD14
*SA15/SDD15
SA16 P4
SA17 P3
SA18 K2
SA19 K1
SA20 J5
SA21 J4
SA22 J3
SA23 J2
SA16
SA17
SA18
SA19
LA20
LA21
LA22
LA23
SD0 Y1
SD1 Y2
SD2 W2
SD3 Y3
SD4 W3
SD5 V3
SD6 Y4
SD7 W4
SD8 L5
SD9 M2
SD10 M4
SD11 N1
SD12 N3
SD13 N5
SD14 P1
SD15 P2
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
11 -DACK0
11 -DACK1
11 -DACK3
11 -DACK5
11 -DACK6
11 -DACK7
-DACK0 L2
-DACK1 E1
-DACK3 D2
-DACK5 L4
-DACK6 M3
-DACK7 N2
DACK0
DACK1
DACK3
DACK5
DACK6
DACK7
11 DREQ0
11 DREQ1
11 DREQ3
11 DREQ5
11 DREQ6
11 DREQ7
DREQ0 L3
DREQ1 E2
DREQ3 D3
DREQ5 M1
DREQ6 M5
DREQ7 N4
DRQ0
DRQ1
DRQ3
DRQ5
DRQ6
DRQ7
11 AEN
11 BALE
11 -SBHE
11 -REFRESH
11 -IOR
11 -IOW
11 -MEMR
11 -MEMW
11 -SMEMR
11 -SMEMW
11 -IOCS16
11 -MEMCS16
11 IOCHRDY
11 -IOCHCK
11 TC
AEN B2
BALE H2
-SBHE F2
-REFRESH E3
-IOR D1
-IOW C2
-MEMR U4
-MEMW V4
-SMEMR A1
-SMEMW B1
-IOCS16 F3
-MEMCS16 F1
IOCHRDY A2
-IOCHCK F4
TC H1
RSTDRV J1
AEN
BALE
SBHE
REFRESH
IOR
IOW
MEMR
MEMW
SMEMR
SMEMW
IOCS16
MEMCS16
IOCHRDY
IOCHK/GPI0
TC
RSTDRV
7,11 REFCLK1
11 SYS_CLK
R68 33
REFCLK1 E4
BCLK H5
OSC
BCLK
IRRX D12
IRTX E12
IRRX/GPO15
IRTX/GPO14
11 IRQ3
11 IRQ4
11 IRQ5
11 IRQ6
11 IRQ7
11 IRQ9
11 IRQ10
11 IRQ11
11,12 IRQ14
11,12 IRQ15
IRQ3 G4
IRQ4 G3
IRQ5 G2
IRQ6 G1
IRQ7 F5
IRQ9 H4
IRQ10 K3
IRQ11 K4
IRQ14 L1
IRQ15 K5
IRQ3
IRQ4
IRQ5
*IRQ6/SLPBTN
IRQ7
IRQ9
IRQ10
IRQ11
IRQ14
IRQ15
11 -XDIR
12 -SOE
-XDIR T5
-SOE U5
XDIR/GPO12
SOE/GPO13
VCC3
F7 VCC
F10 VCC
F12 VCC
F13 VCC
F14 VCC
H6 VCC
J6 VCC
K6 VCC
M6 VCC
N6 VCC
PRD0 B15 P_PRD0
PRD1 D15 P_PRD1
PRD2 A14 P_PRD2
PRD3 B14 P_PRD3
PRD4 C14 P_PRD4
PRD5 D14 P_PRD5
PRD6 E14 P_PRD6
PRD7 A13 P_PRD7
P_PRD[0..7] 13
ACK B13 P_-ACK 13
BUSY C13 P_BUSY 13
PE D13 P_PE 13
SLCT E13 P_SLCT 13
ERROR A15 P_-ERR 13
PINIT C15 P_-INIT 13
AUTOFD C16 P_-AFD 13
SLCTIN E15 P_-SLIN 13
STROBE D16 P_-STB 13
TXD1 A11 TXD1 TXD1 13
DTR1 D11 DTR1 DTR1 13
RTS1 B11 RTS1 RTS1 13
CTS1 C11 CTS1 CTS1 13
DSR1 C12 DSR1 DSR1 13
DCD1 A12 DCD1 DCD1 13
RI1 E11 RI1 RI1 13
RXD1 B12 RXD1 RXD1 13
TXD2 D10 TXD2 TXD2 13
DTR2 B9 DTR2 DTR2 13
RTS2 E10 RTS2 RTS2 13
CTS2 A9 CTS2 CTS2 13
DSR2 C10 DSR2 DSR2 13
DCD2 A10 DCD2 DCD2 13
RI2 C9 RI2 RI2 13
RXD2 B10 RXD2 RXD2 13
VCCUSB F9
GNDUSB F8
VCC3
L16 FB
L17 FB
CB12 .1u
CT8 10u
*USBCLK C3 USBCLK USBCLK 7
*USBP0+ A3 USBDAT0+ USBDAT0+ 13
*USBP0- B3 USBDAT0- USBDAT0- 13
*USBP1+ C4 USBDAT1+ USBDAT1+ 13
*USBP1- D4 USBDAT1- USBDAT1- 13
*DRQ2/OC1/SERIRQ/GPIOE H3 MUX1
*DACK2/OC0/GPIOF G5 MUX2
*USBP2+ A4 USBDAT2+
*USBP2- B4 USBDAT2-
*USBP3+ B5 USBDAT3+
*USBP3- E6 USBDAT3-
*KBCK/KA20G E5 KB_CLK KB_CLK 13
KBDT/KBRC A5 KB_DATA KB_DATA 13
MSCK/IRQ1 D5 MS_CLK MS_CLK 13
MSDT/IRQ12 C5 MUX3
*ROMCS/KBCS C1 -ROMCS -ROMCS 11
DRVDEN0 D9
DRVDEN1 D6
INDEX D7
MTR0 E9
DS1 A8
DS0 B8
MTR1 C8
DIR D8
STEP E8
WDATA A7
WGATE B7
TRAK0 E7
WRTPRT A6
RDATA B6
HDSEL C7
DSKCHG C6
FDD1
1K 8P4R
RN28
R73 1K
GND F6
GND F11
GND G6
GND J9
GND J10
GND J11
GND J12
GND K9
GND K10
GND K11
GND K12
GND L6
GND L9
GND L10
GND L11
GND L12
GND M9
GND M10
GND M11
GND M12
GND P6
GND R6
GND
USBDAT2- R81 27 USBDT2-
USBDAT2+ R82 27 USBDT2+
USBDAT3- R83 27 USBDT3-
USBDAT3+ R84 27 USBDT3+
CP4 47p
CP3 47p
CP2 47p
CP1 47p
RN29 15K 8P4R
USB2
FS1 FUSE
FS2 FUSE
L20 FB
CM2 1u
CM1 1u
L19 FB
JUSB1
USB_HEADER
CT9 10u
CB13 .1u
CB14 .1u
CT10 10u
L18 FB
MUX3 R80 0(OPT) IRQ12 IRQ12 11
R79 0 MS_DATA MS_DATA 13
MUX1 R77 0(OPT) DREQ2 DREQ2 11
R76 0 -OC1 -OC1 13
MUX2 R78 0(OPT) -DACK2 -DACK2 11
R75 0 -OC0 -OC0 13
U4A F04
U4B F04
U4C F04
U4D F04
R72 33 RES_DRV RES_DRV 11
R70 33 -RESETX -RESETX 4
R71 33 -IDERST -IDERST 12
RSTDRV
-ROMCS R74 4.7K
Straping for INIT Low
Active (Socket 7)
IR
JIR1
R69 4.7K
IRRX
IRTX
VIA TECHNOLOGIES, INC.
Title
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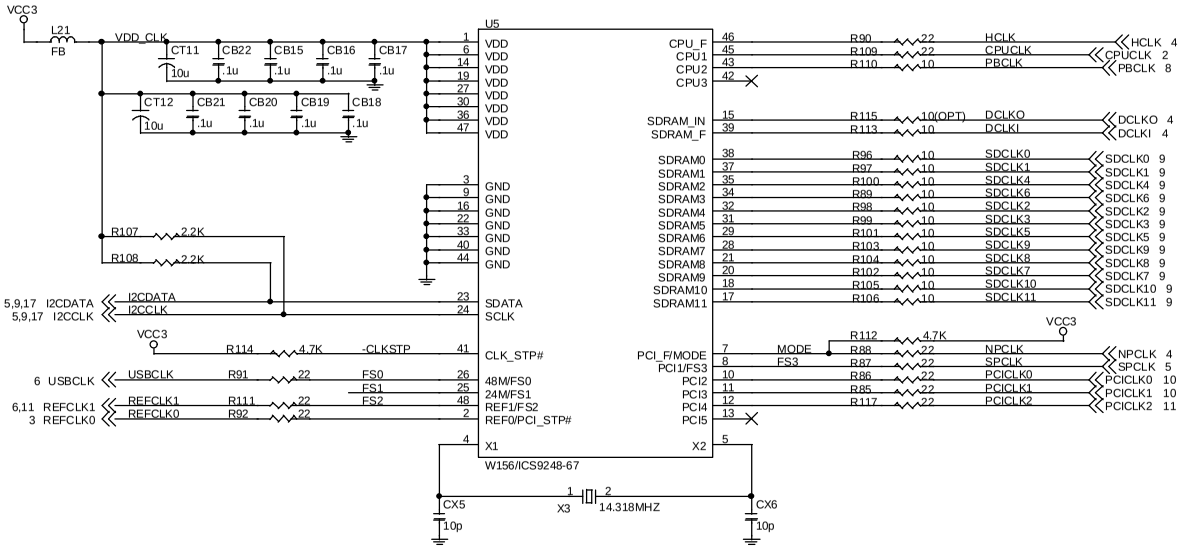
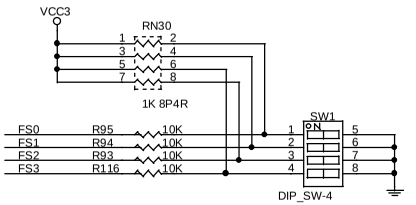
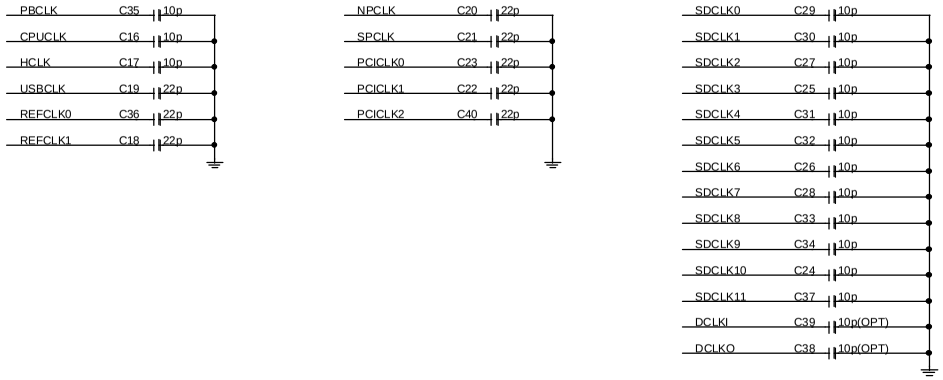


SW1 4	SW1 3	SW1 2	SW1 1	CPU	RATIO	PCI
OFF	OFF	OFF	OFF	60	2	30
OFF	OFF	OFF	ON	66.8	2	33.4
OFF	OFF	ON	OFF	70	2	35
OFF	OFF	ON	ON	75	3	25
OFF	ON	OFF	OFF	80	3	26.67
OFF	ON	OFF	ON	83.3	3	27.76
OFF	ON	ON	OFF	95.25	3	31.75
OFF	ON	ON	ON	100	3	33.33
ON	OFF	OFF	OFF	75	2	37.5
ON	OFF	OFF	ON	80	2	40
ON	OFF	ON	OFF	83.3	2	41.65
ON	OFF	ON	ON	105(103)	3	35
ON	ON	OFF	OFF	110(107)	3	36.67
ON	ON	OFF	ON	115(112)	3	38.33
ON	ON	ON	OFF	120(117)	3	40
ON	ON	ON	ON	124(122)	3	41.33





VIA TECHNOLOGIES, INC.

Title: CLOCK SYNTHESIZER

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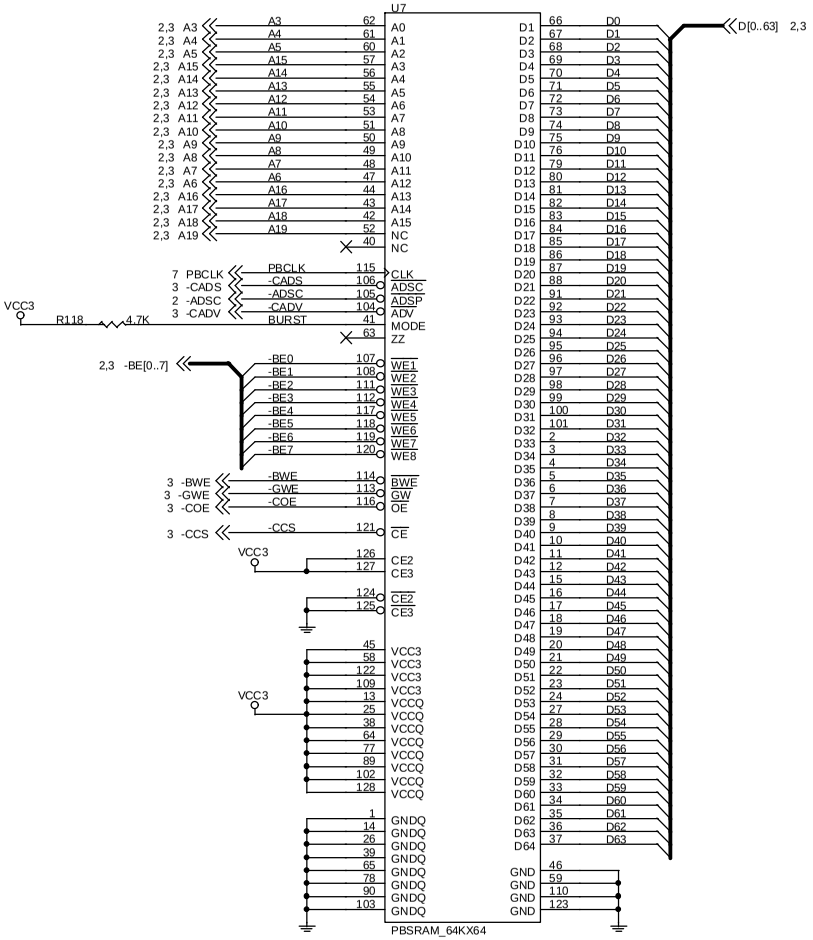

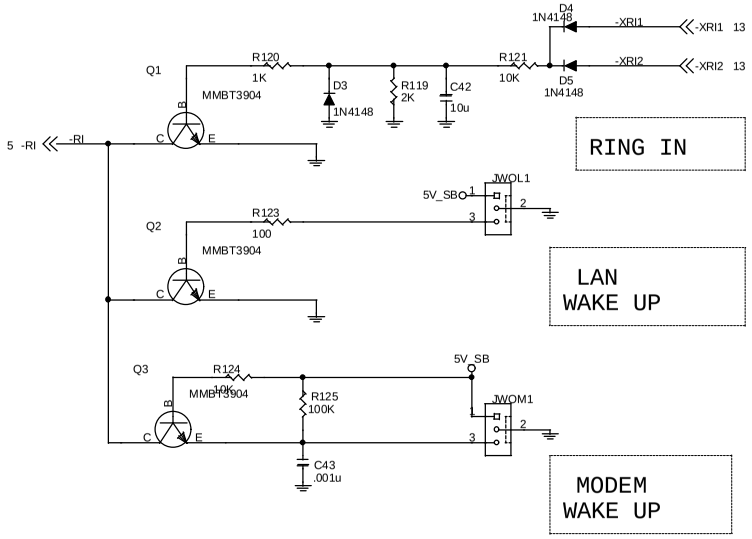

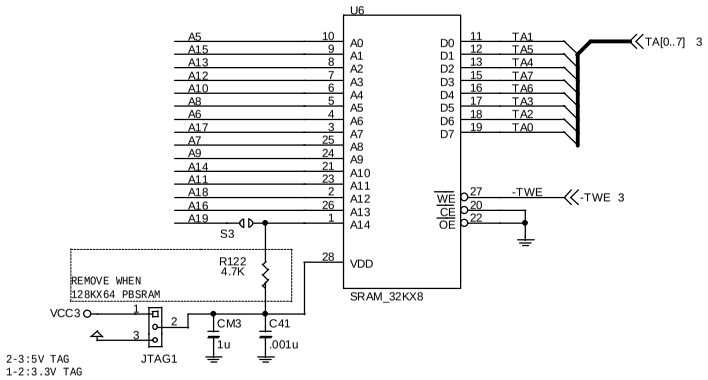

VIA TECHNOLOGIES, INC.

Title	L2 CACHE & WAKE UP CIRCUIT	
Size C	Document Number VIA Apollo MVP4	Rev 1.1
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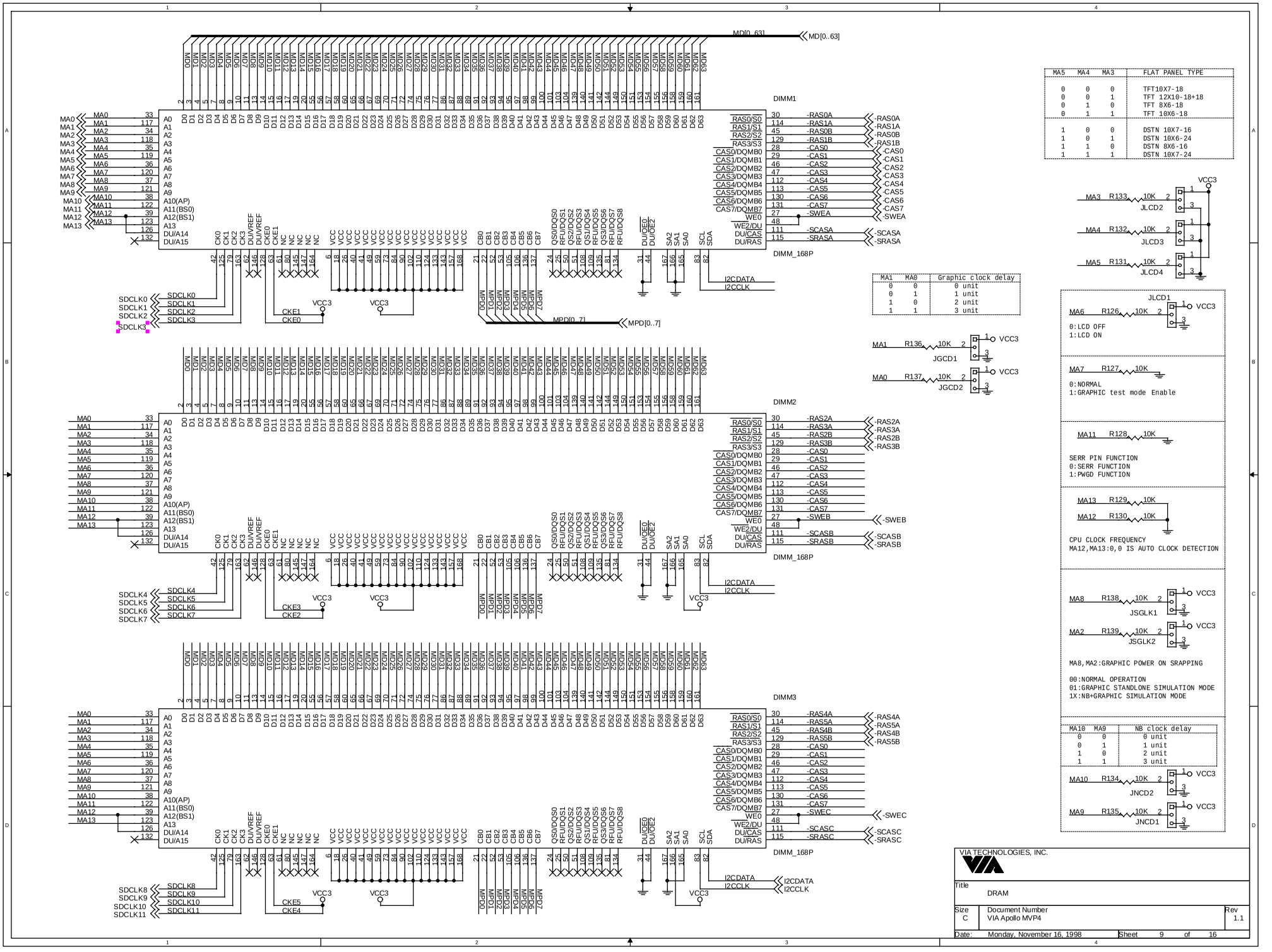

MA5	MA4	MA3	FLAT PANEL TYPE
0	0	0	TFT10X7-18
0	0	1	TFT 12X10-18+18
0	1	0	TFT 8X6-18
0	1	1	TFT 10X6-18
1	0	0	DSTN 10X7-16
1	0	1	DSTN 10X6-24
1	1	0	DSTN 8X6-16
1	1	1	DSTN 10X7-24

MA1	MA0	Graphic clock delay
0	0	0 unit
0	1	1 unit
1	0	2 unit
1	1	3 unit

MA10	MA9	NB clock delay
0	0	0 unit
0	1	1 unit
1	0	2 unit
1	1	3 unit

VIA TECHNOLOGIES, INC.

Title: DRAM

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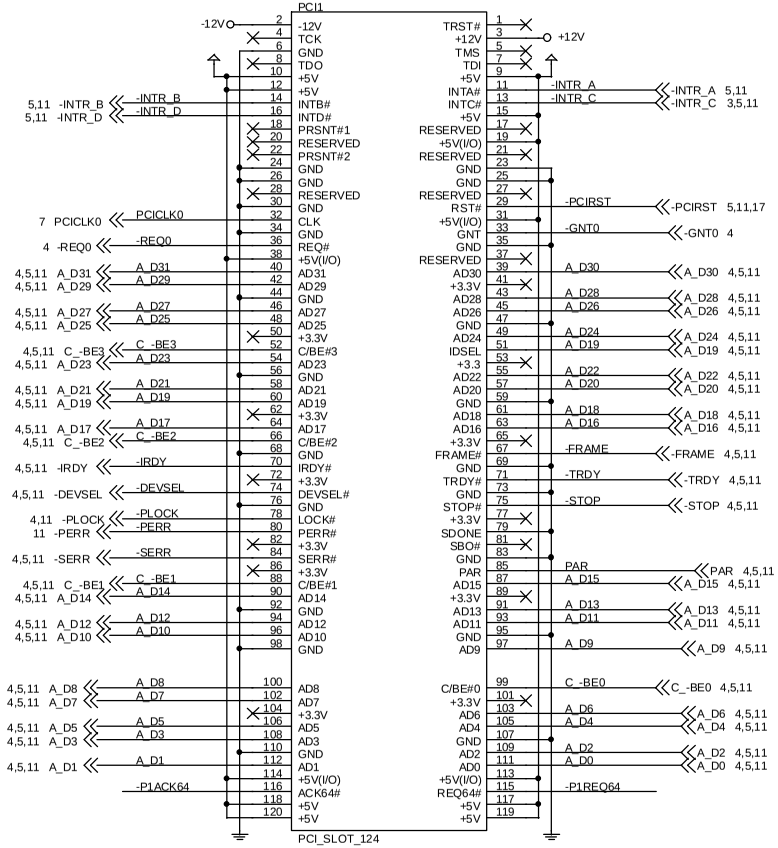

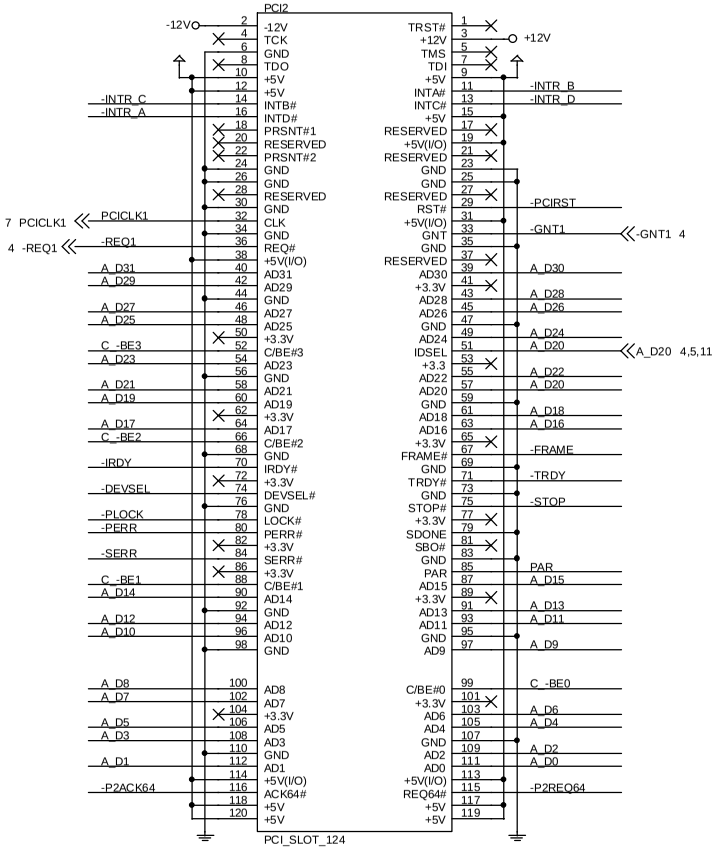

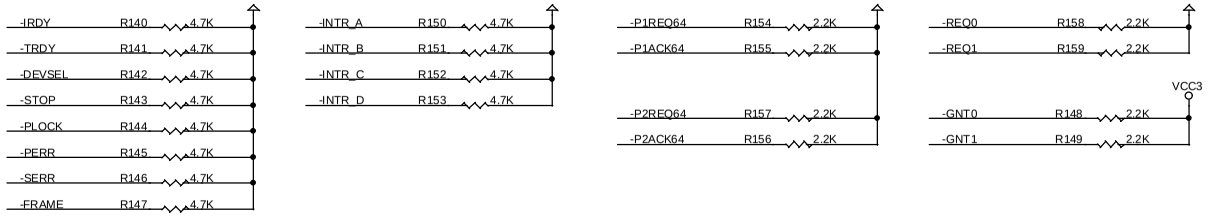

VIA TECHNOLOGIES, INC.

Title: PCI1 & PCI2 SLOTS

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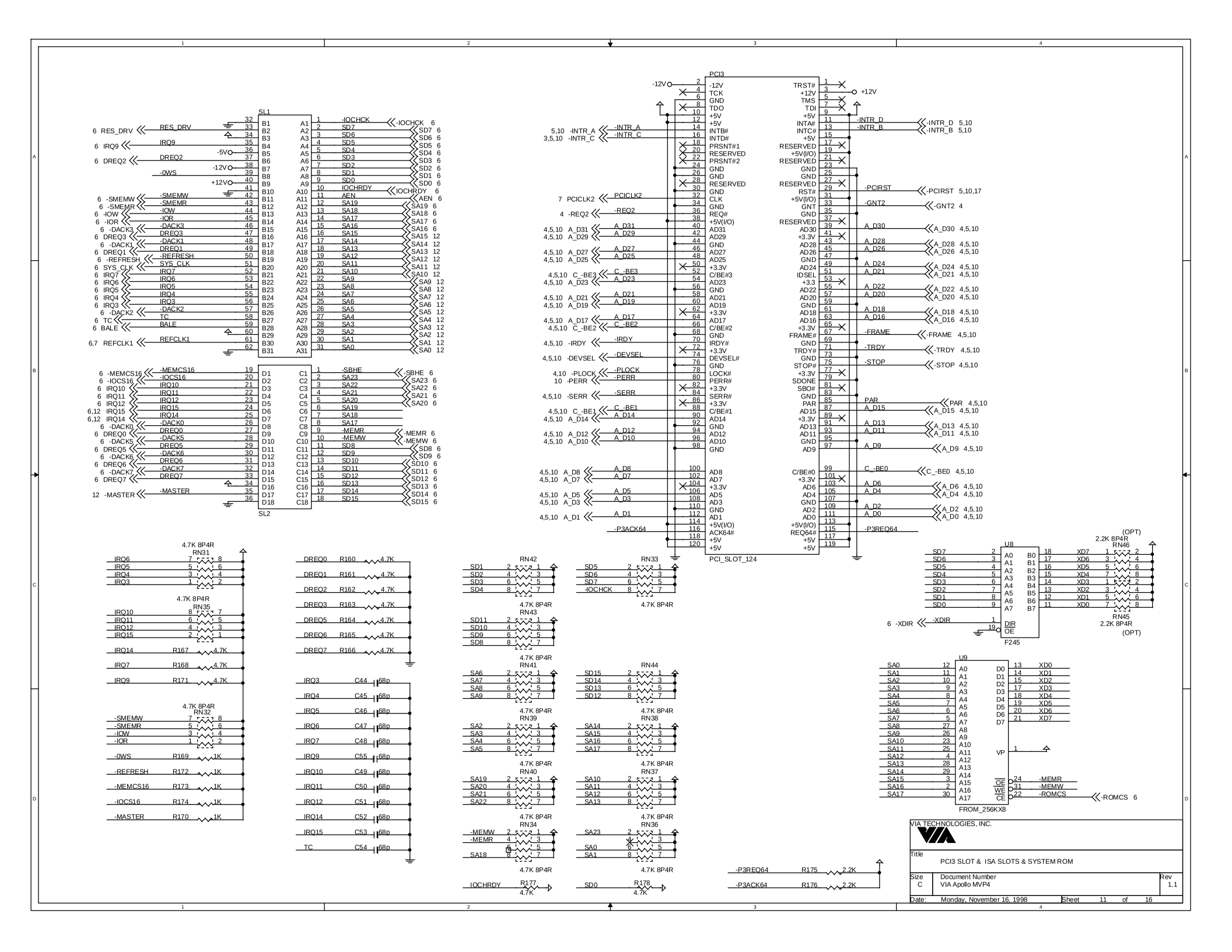
SL1
SL2
PCI3
PCI_SLOT_124
RES_DRV
IRQ9
DREQ2
-0WS
-SMEMW
-SMEMR
-IOW
-IOR
-DACK3
DREQ3
-DACK1
DREQ1
-REFRESH
SYS_CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
-DACK2
TC
BALE
REFCLK1
-IOCHCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IOCHRDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
-MEMCS16
-IOCS16
IRQ10
IRQ11
IRQ12
IRQ15
IRQ14
-DACK0
DREQ0
-DACK5
DREQ5
-DACK6
DREQ6
-DACK7
DREQ7
-MASTER
-SBHE
SA23
SA22
SA21
SA20
SA19
SA18
SA17
-MEMR
-MEMW
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
-12V
TCK
GND
TDO
+5V
INTB#
INTD#
PRSNT#1
RESERVED
PRSNT#2
RESERVED
GND
CLK
REQ#
+5V(I/O)
AD31
AD29
AD27
AD25
+3.3V
C/BE#3
AD23
AD21
AD19
AD17
C/BE#2
IRDY#
DEVSEL#
LOCK#
PERR#
SERR#
C/BE#1
AD14
AD12
AD10
AD8
AD7
AD5
AD3
AD1
ACK64#
TRST#
+12V
TMS
TDI
INTA#
INTC#
RST#
GNT
AD30
AD28
AD26
AD24
IDSEL
AD22
AD20
AD18
AD16
FRAME#
TRDY#
STOP#
SDONE
SBO#
PAR
AD15
AD13
AD11
AD9
C/BE#0
AD6
AD4
AD2
AD0
REQ64#
-INTR_A
-INTR_C
-INTR_D
-INTR_B
-PCIRST
-GNT2
A_D31
A_D29
A_D27
A_D25
C_-BE3
A_D23
A_D21
A_D19
A_D17
C_-BE2
-IRDY
-DEVSEL
-PLOCK
-PERR
-SERR
C_-BE1
A_D14
A_D12
A_D10
A_D8
A_D7
A_D5
A_D3
A_D1
-P3ACK64
-FRAME
-TRDY
-STOP
PAR
C_-BE0
A_D6
A_D4
A_D2
A_D0
-P3REQ64
PCICLK2
-REQ2
RN31
RN32
RN33
RN34
RN35
RN36
RN37
RN38
RN39
RN40
RN41
RN42
RN43
RN44
RN45
RN46
4.7K 8P4R
2.2K 8P4R
(OPT)
R167
R168
R171
R169
R172
R173
R174
R170
R177
R178
R175
R176
4.7K
1K
2.2K
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
R160
R161
R162
R163
R164
R165
R166
C44
C45
C46
C47
C48
C55
C49
C50
C51
C52
C53
C54
68p
U8
F245
U9
FROM_256KX8
-XDIR
DIR
OE
VP
-MEMR
-MEMW
-ROMCS
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
VIA TECHNOLOGIES, INC.
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PCI3 SLOT & ISA SLOTS & SYSTEM ROM
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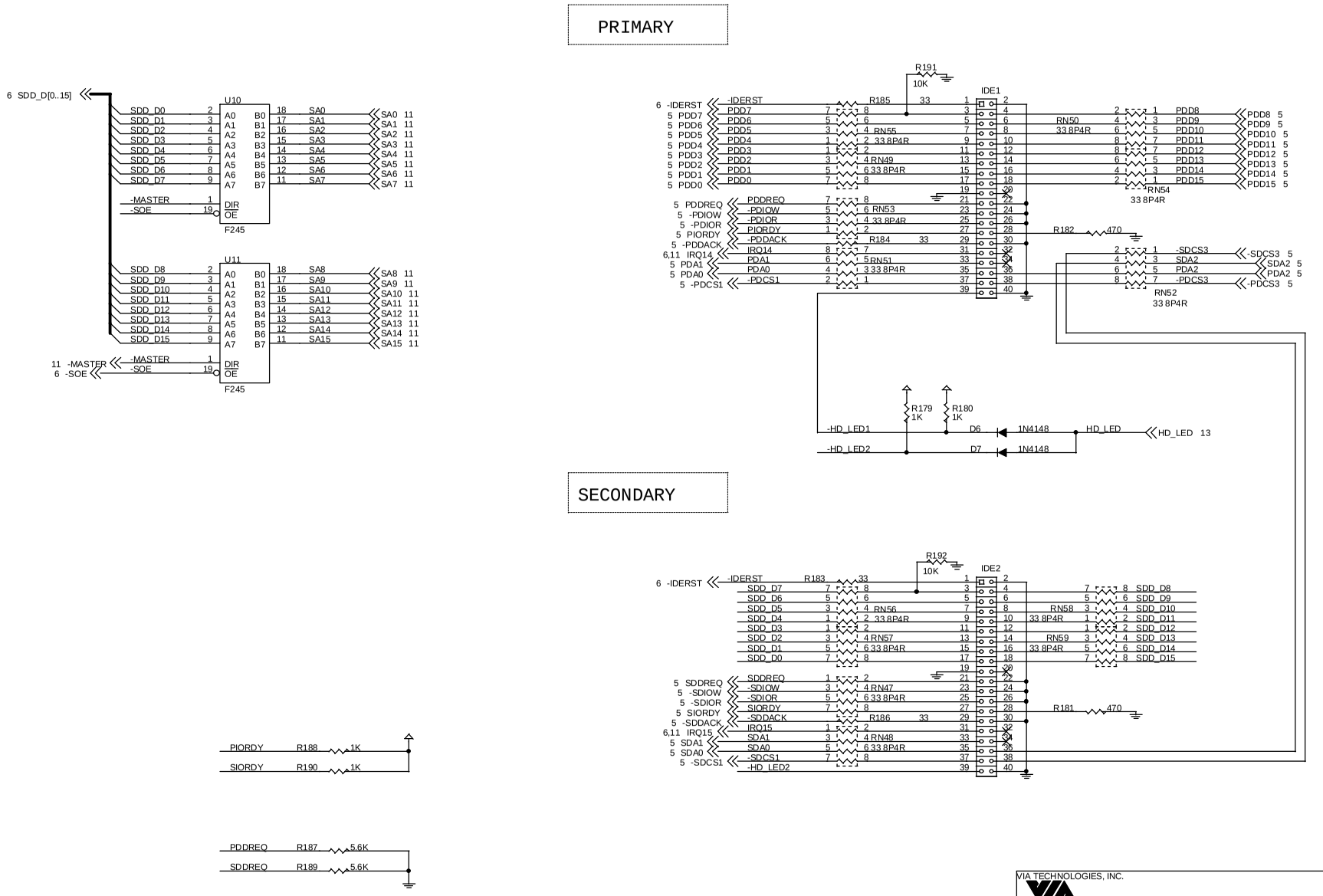
PRIMARY
SECONDARY
6 SDD_D[0..15]
U10
U11
F245
-MASTER
-SOE
DIR
OE
IDE1
IDE2
R191
10K
R192
10K
R185
R184
R182
R183
R186
470
33
RN55
RN56
RN57
RN58
RN59
RN54
RN52
33 8P4R
R179
R180
1K
-HD_LED1
-HD_LED2
D6
D7
1N4148
HD_LED
HD_LED 13
R188
R190
PIORDY
SIORDY
R187
R189
PDDREQ
SDDREQ
5.6K
VIA TECHNOLOGIES, INC.
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IDE1 & IDE2
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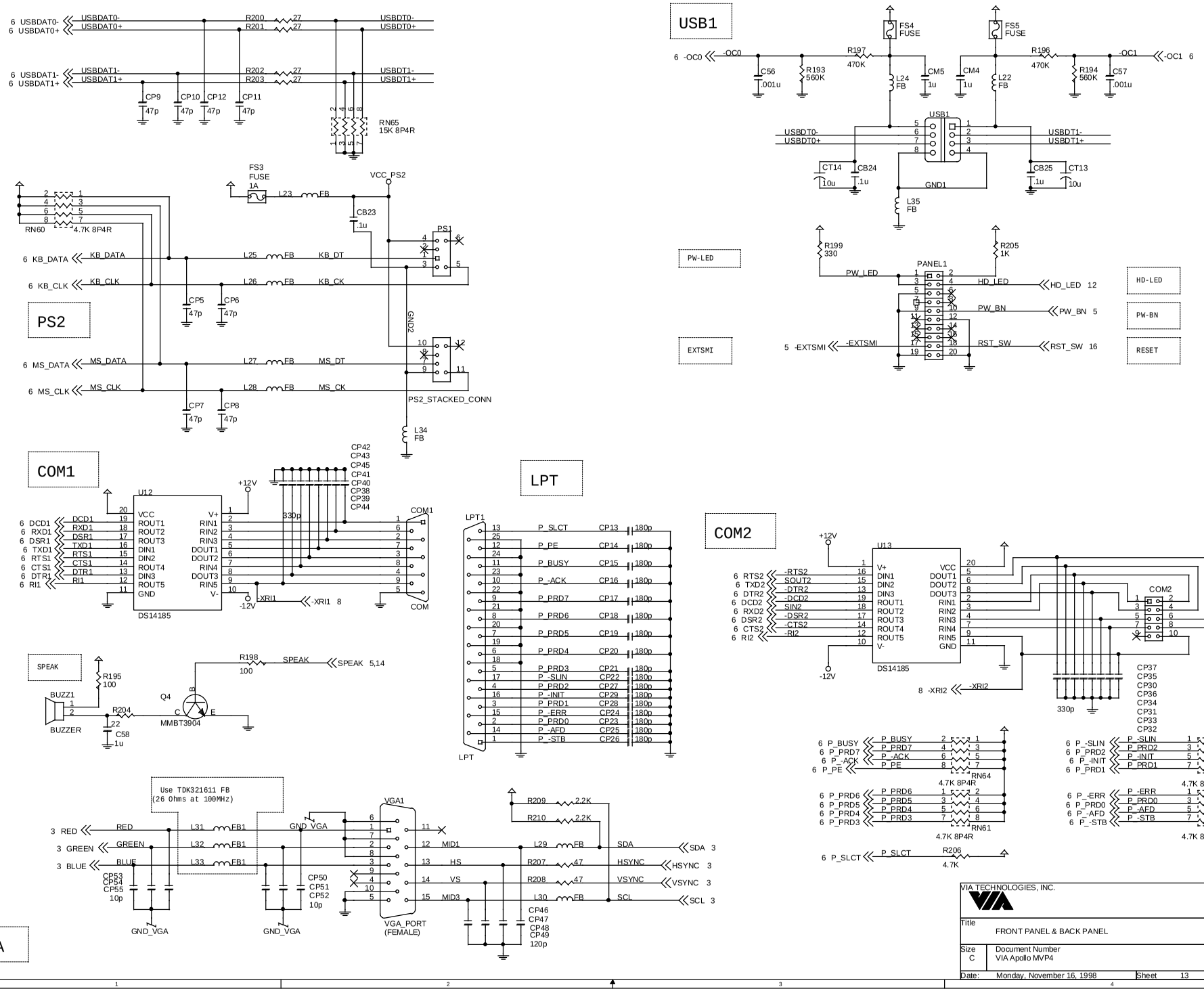
USB1
PS2
COM1
LPT
COM2
VGA
PW-LED
EXTSMI
HD-LED
PW-BN
RESET
USBDAT0-
USBDAT0+
USBDAT1-
USBDAT1+
USBDT0-
USBDT0+
USBDT1-
USBDT1+
RN65
15K 8P4R
RN60
4.7K 8P4R
KB_DATA
KB_CLK
MS_DATA
MS_CLK
PS2_STACKED_CONN
-OC0
-OC1
FS4
FUSE
FS5
FUSE
FS3
FUSE
1A
VCC_PS2
PANEL1
PW_LED
HD_LED
PW_BN
RST_SW
-EXTSMI
DS14185
MMBT3904
BUZZER
SPEAK
LPT1
VGA_PORT
(FEMALE)
Use TDK321611 FB
(26 Ohms at 100MHz)
RED
GREEN
BLUE
HSYNC
VSYNC
SDA
SCL
GND_VGA
P_SLCT
P_PE
P_BUSY
P_-ACK
P_-ERR
P_SLIN
P_-INIT
P_-AFD
P_-STB
P_PRD0
P_PRD1
P_PRD2
P_PRD3
P_PRD4
P_PRD5
P_PRD6
P_PRD7
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FRONT PANEL & BACK PANEL
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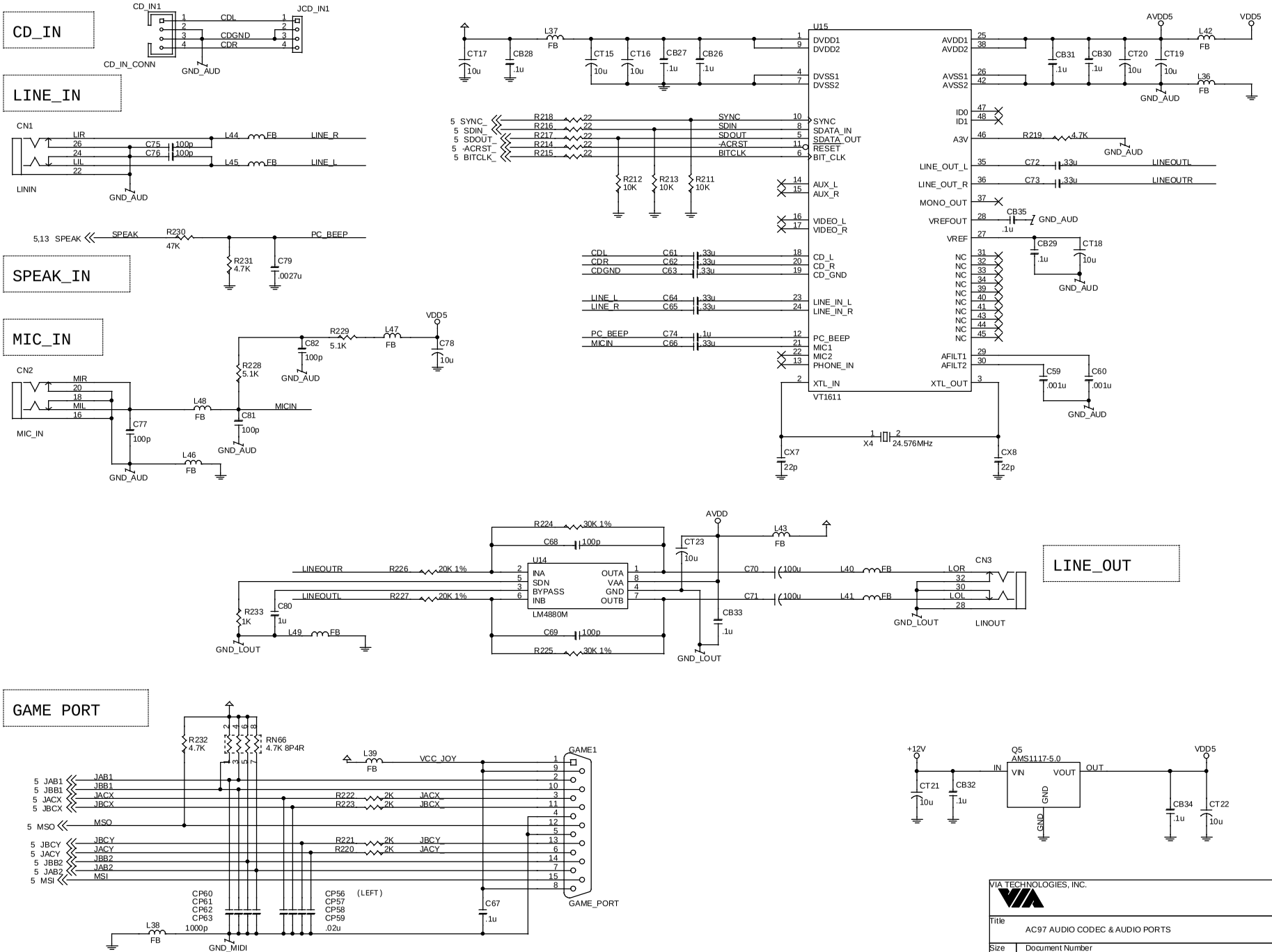
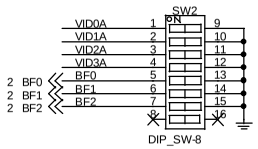
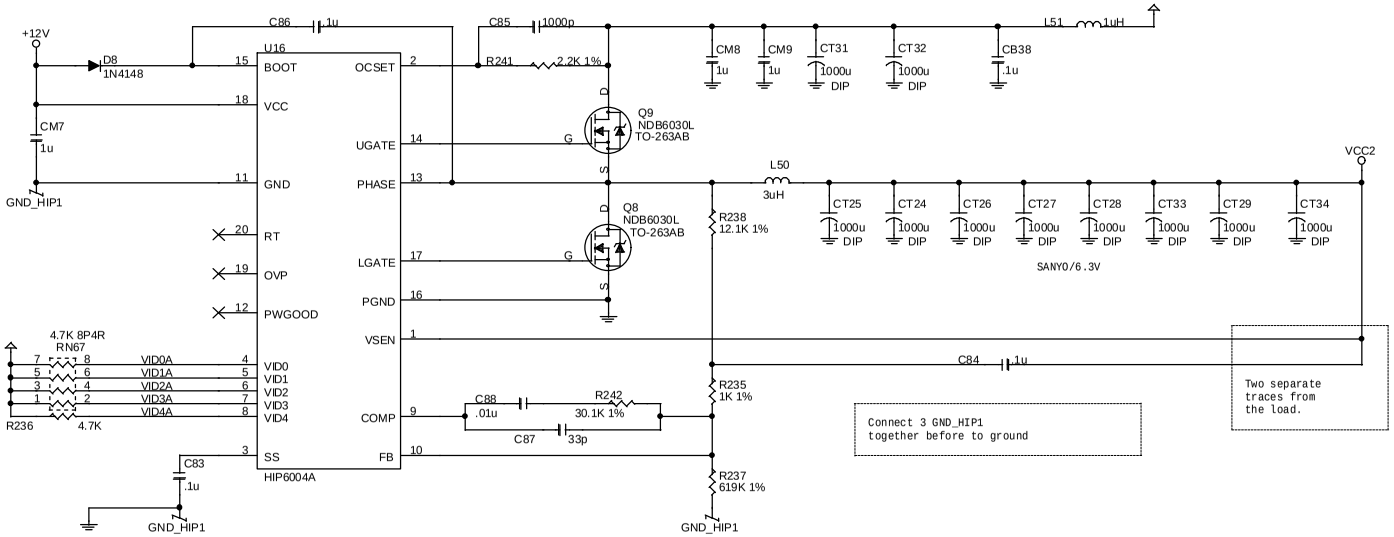
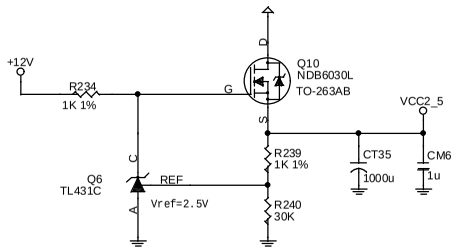
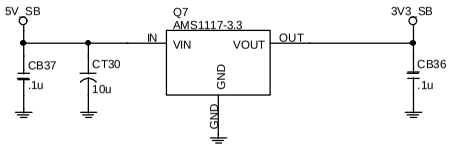

CD_IN
LINE_IN
SPEAK_IN
MIC_IN
LINE_OUT
GAME PORT
CD_IN1
JCD_IN1
CD_IN_CONN
CDL
CDGND
CDR
GND_AUD
CN1
LIR
LIL
LINE_R
LINE_L
LININ
5,13 SPEAK
SPEAK
R230
47K
R231
4.7K
C79
.0027u
PC_BEEP
CN2
MIR
MIL
MIC_IN
MICIN
R228
5.1K
R229
5.1K
L47
FB
C82
100p
C78
10u
VDD5
L48
C81
C77
L46
U15
VT1611
DVDD1
DVDD2
DVSS1
DVSS2
SYNC
SDIN
SDOUT
-ACRST
BITCLK
RESET
BIT_CLK
SDATA_IN
SDATA_OUT
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_R
CD_GND
LINE_IN_L
LINE_IN_R
PC_BEEP
MIC1
MIC2
PHONE_IN
XTL_IN
XTL_OUT
X4
24.576MHz
CX7
CX8
22p
AVDD1
AVDD2
AVSS1
AVSS2
AVDD5
VDD5
ID0
ID1
A3V
4.7K
LINE_OUT_L
LINE_OUT_R
LINEOUTL
LINEOUTR
MONO_OUT
VREFOUT
VREF
NC
AFILT1
AFILT2
C59
.001u
C60
.001u
U14
LM4880M
INA
SDN
BYPASS
INB
OUTA
VAA
GND
OUTB
LINEOUTR
LINEOUTL
R226
20K 1%
R227
20K 1%
R224
30K 1%
R225
30K 1%
C68
C69
100p
R233
1K
C80
1u
L49
C70
C71
100u
L40
L41
L43
C23
C33
.1u
CN3
LOR
LOL
LINOUT
GND_LOUT
R232
4.7K
RN66
4.7K 8P4R
L39
VCC_JOY
GAME1
GAME_PORT
JAB1
JBB1
JACX
JBCX
MSO
JBCY
JACY
JBB2
JAB2
MSI
R222
R223
R221
R220
2K
CP60
CP61
CP62
CP63
1000p
CP56
CP57
CP58
CP59
.02u
(LEFT)
C67
L38
GND_MIDI
+12V
Q5
AMS1117-5.0
VIN
VOUT
GND
IN
OUT
C21
C32
C34
C22
10u
.1u
VIA TECHNOLOGIES, INC.
Title
AC97 AUDIO CODEC & AUDIO PORTS
Size
C
Document Number
VIA Apollo MVP4
Rev
1.1
Date:
Monday, November 16, 1998
Sheet
14
of
16

SW1				
4	3	2	1	VCC2
OFF	OFF	OFF	OFF	0
OFF	OFF	OFF	ON	2.1
OFF	OFF	ON	OFF	2.2
OFF	OFF	ON	ON	2.3
OFF	ON	OFF	OFF	2.4
OFF	ON	OFF	ON	2.5
OFF	ON	ON	OFF	2.6
OFF	ON	ON	ON	2.7
ON	OFF	OFF	OFF	2.8
ON	OFF	OFF	ON	2.9
ON	OFF	ON	OFF	3.0
ON	OFF	ON	ON	3.1
ON	ON	OFF	OFF	3.2
ON	ON	OFF	ON	3.3
ON	ON	ON	OFF	3.4
ON	ON	ON	ON	3.5

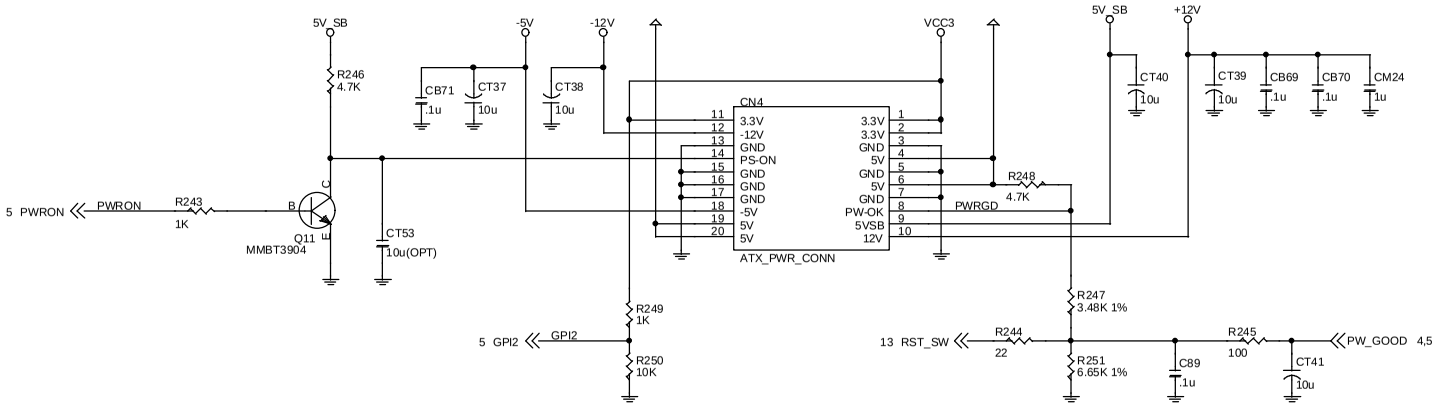




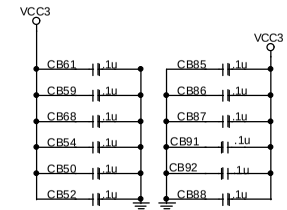




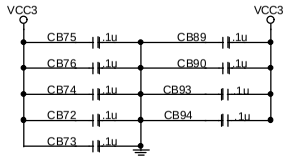
VIA TECHNOLOGIES, INC.		
Title: DC-DC CONVERTERS		
Size: C	Document Number: VIA Apollo MVP4	Rev: 1.1
Date: Monday, November 16, 1998	Sheet 15 of 16	

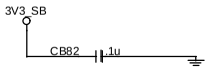


Around NB

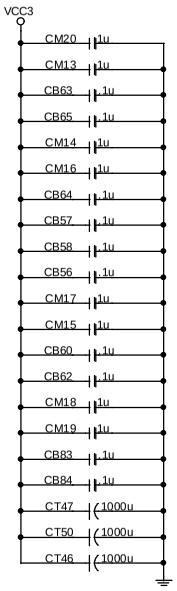


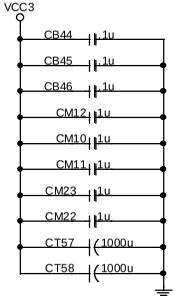
Around SB

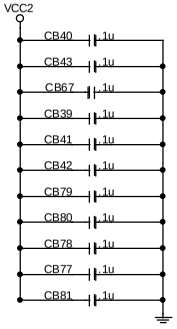


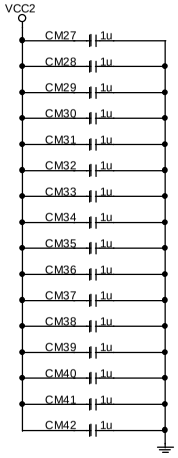


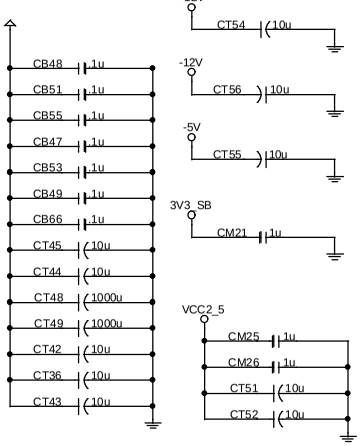
Around SB











VIA TECHNOLOGIEA, INC.

Title	ATX POWER/BYPASS CAPACITORS	
Size C	Document Number VIA Apollo MVP4	Rev 1.1
Date: Monday, November 16, 1998	Sheet 16 of 16	

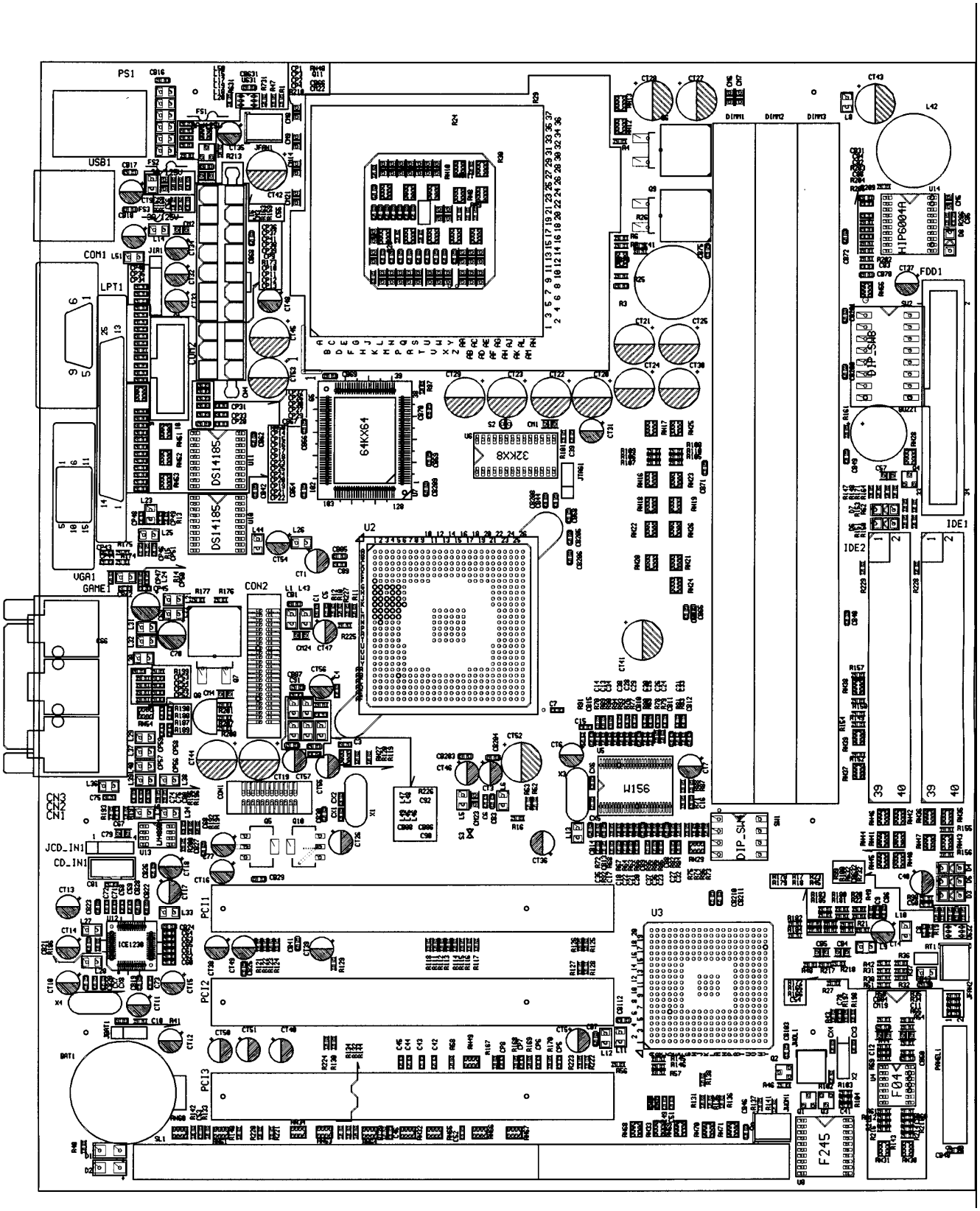
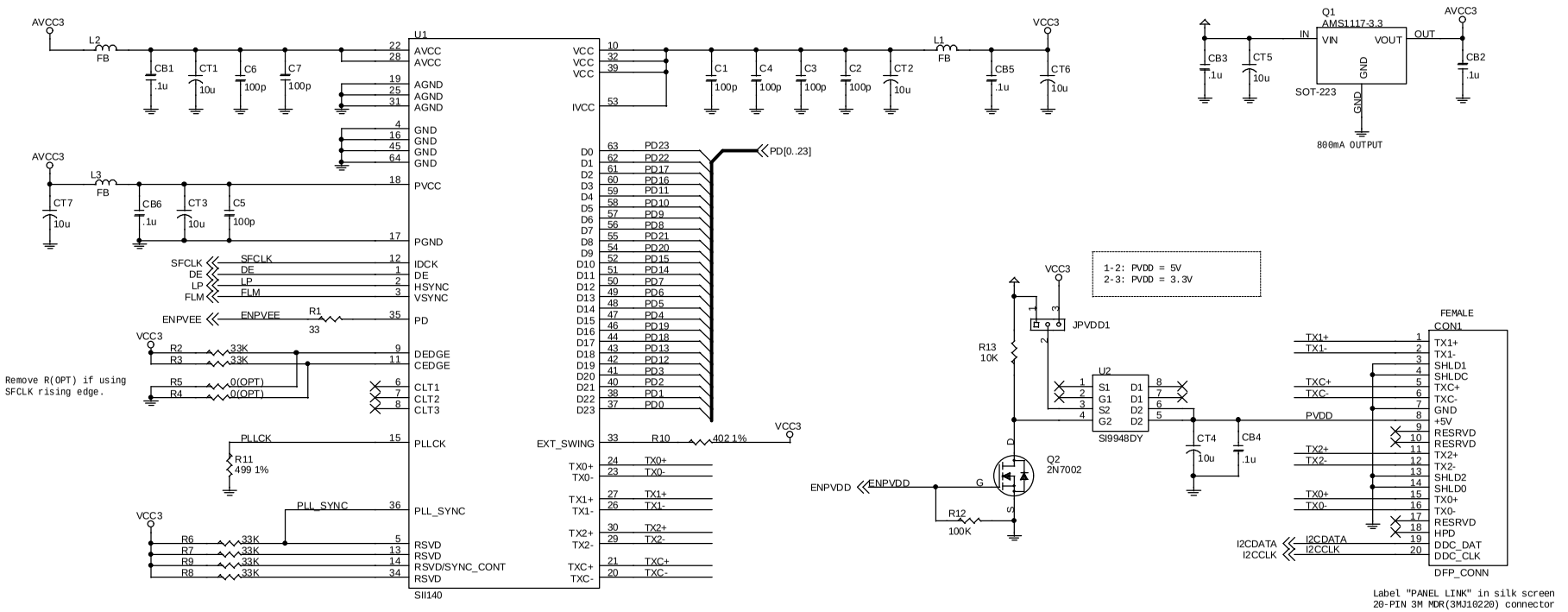


Figure A-1. Apollo MVP4 Reference Design Component Placement

Appendix B - TMDS Transmitter Reference Design Schematic



REFERENCE ONLY

VIA TECH. bears no resposibity for
any error in this schematic. Subject
to change without any notice.
Please refer to Silicon Image datasheet
and application note for more details.

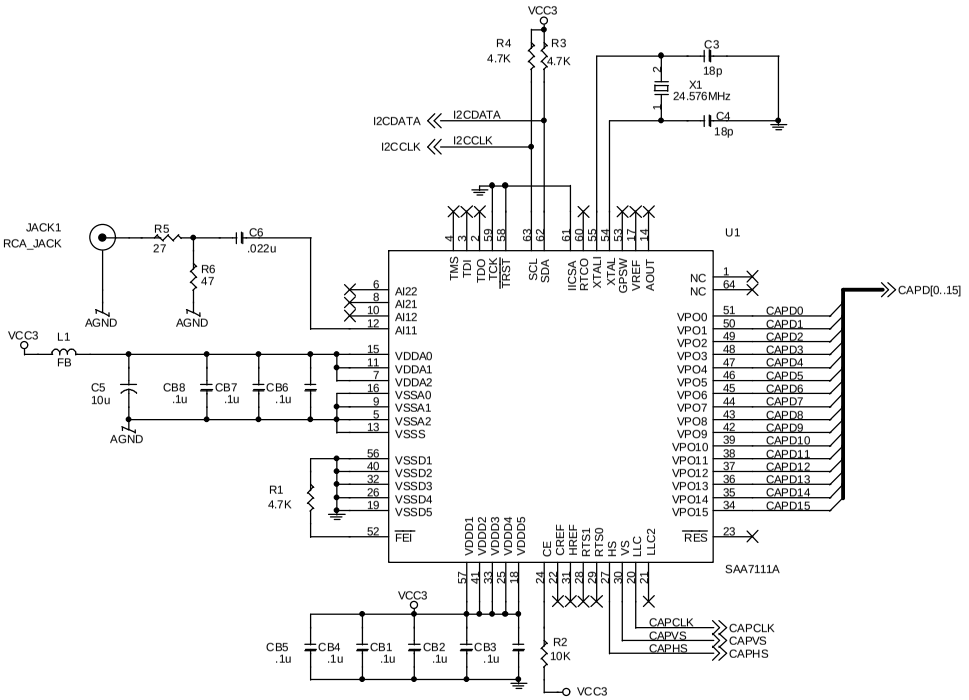
NOTE:

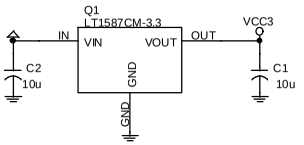
1.I2CCLK and I2CDATA are
connected to SB (VT82C686A)

2.ENPVDD, ENPVEE, SFCLK, DE, LP
and FLM are connected to VT8501

VIA TECHNOLOGIES, INC.		
Title: PANEL LINK TRANSMITTER (SI SII140)		
Size: C	Document Number: PANEL LINK TRANSMITTER FOR MVP4	Rev: 1.0
Date: Monday, November 16, 1998	Sheet 1 of 1	

Appendix C - TV Decoder Reference Design Schematic





REFERENCE ONLY

VIA TECH. bears no resposibity for
any error in this schematic. Subject
to change without any notice.
Please refer to Philips datasheet
and application note for more details.

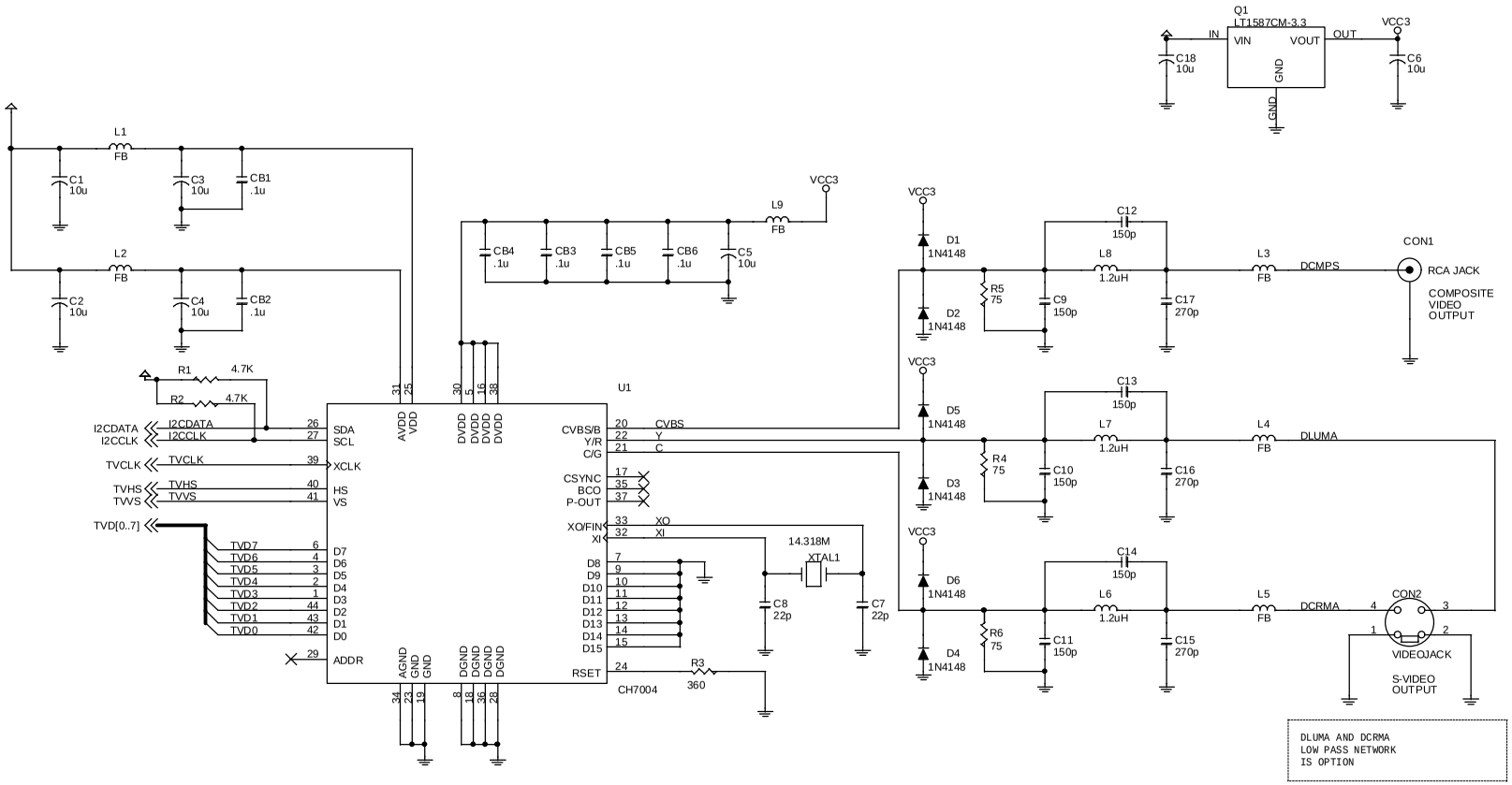
NOTE:

1.CAPD[0..15], CAPCLK, CAPHS and CAPVS are connected to VT8501

2.I2CCLK and I2CDATA are connected TO SB (VT82C686A)

VIA TECHNOLOGIES, INC.		
Title: TV DECODER (Philips SAA7111A)		
Size: C	Document Number: TV DECODER FOR MVP4	Rev: 1.0
Date: Friday, October 02, 1998	Sheet 1 of 1	

Appendix D - TV Encoder Reference Design Schematic



REFERENCE ONLY

VIA TECH. bears no resposibity for
any error in this schematic. Subject
to change without any notice.
Please refer to Chrontel's datasheet
and application note for more details.

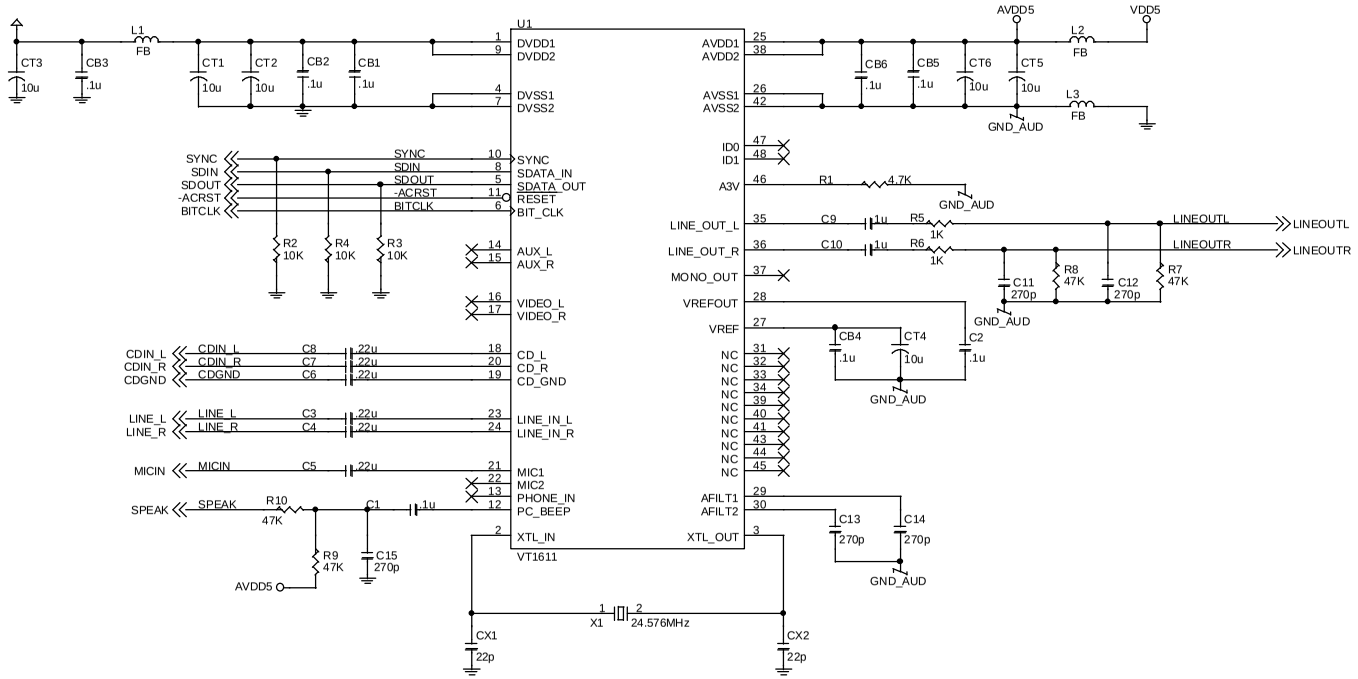
NOTE:

1.TVD[0..7], TVCLK, TVHS and
TVVS are connected to VT8501

2.I2CCLK and I2CDATA are
connected TO SB (VT82C686A)

VIA TECHINOLOGIES, INC.		
Title: TV ENCODER (Chrontel CH7004)		
Size: C	Document Number: TV ENCODER FOR MVP4	Rev: 1.0
Date: Friday, October 02, 1998	Sheet 1 of 1	

Appendix E - VIA AC'97 CODEC Reference Design Schematic



REFERENCE ONLY

VIA TECH. bears no resposibity for
any error in this schematic. Subject
to change without any notice.
Please refer to VIAl's datasheet
and application note for more details.

NOTE:

1.LINEOUTL and LINEOUTR are connected to LINE-OUT phone jack

2.LINE_L and LINE_R are connected to LINE-IN phone jack

3.CDIN_L, CDIN_R and CDGND are connected CDIN connector

4.MICIN is connected to MICIN phone jack

5.SYNC, SDIN, SDOUT, -ACRST BITCLK and SPEAK are connected to SB (VT82C686A)

VIA TECHNOLOGIES, INC.		
Title: AUDIO CODEC (VIA VT1611)		
Size: C	Document Number: AC'97 CODEC FOR MVP4	Rev: 1.0
Date: Friday, October 02, 1998	Sheet 1 of 1	

Appendix F - SPKR Strapping Application Circuits

Power-up strapping for the VT82C686A SPKR pin (pin V5) determines the function of the Secondary IDE disk data bus pins (SDD[15..0]) to be either SDD[15..0] (SPKR strapped low) or Audio/Game port functions (SPKR strapped high).

The speaker drive circuit commonly used in PC motherboards uses a fairly small base resister (on the order of 22 ohms) into the base of a transistor driver. This circuit, however, results in too low a voltage on the SPKR pin for the strap pull-up resistor to overcome. In this case, power up reset will always detect a low signal. Therefore, either of the two application circuits shown below in figures F-1 or F-2 should be used to insure that both high and low strap levels are detected properly.

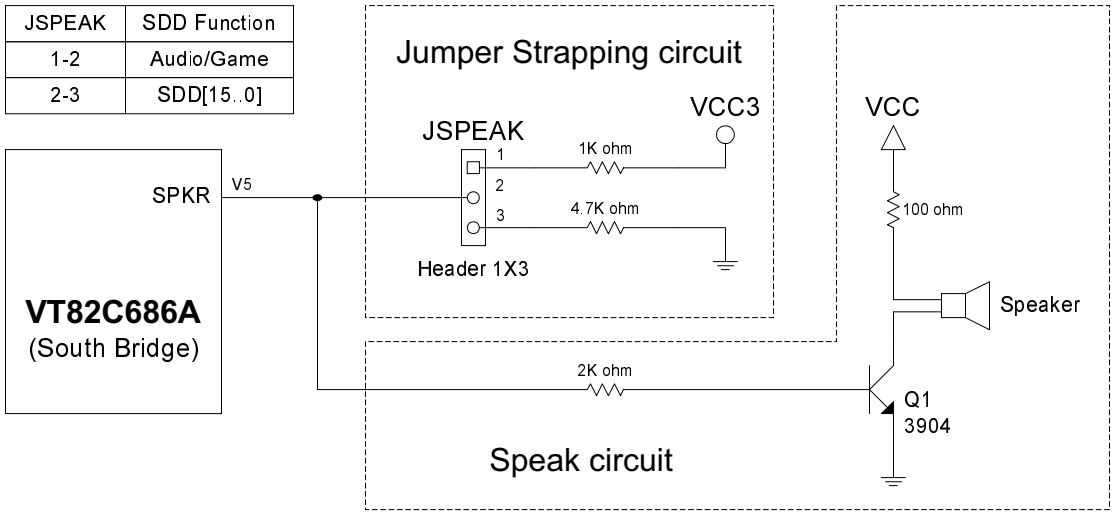


Figure F-1. VT82C686A SPKR Pin Transistor Driver Solution

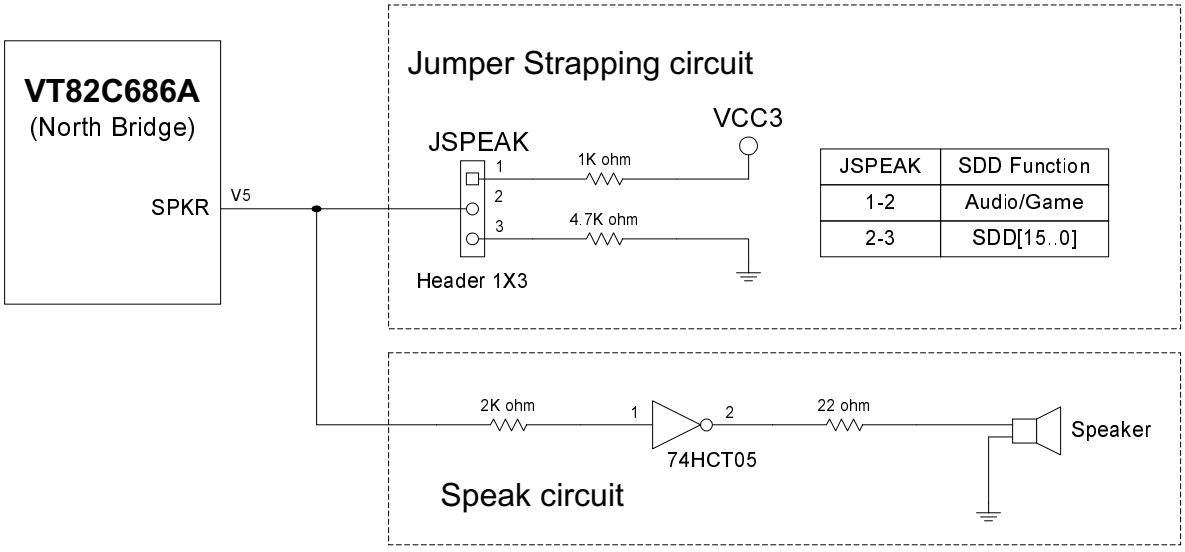


Figure F-2. VT82C686A SPKR Pin Inverter Driver Solution