



PDC20319 series

PCI Bus Mastering SATA/ SATA RAID Accelerator

Development guide

Revision 1.0

Powered by PROMISE ATA RAID



CHANGE HISTORY	5
INTRODUCTION	6
FEATURES	6
1.GENERAL	6
2.PCI INTERFACE	6
3.RAID ENGINE	7
4.SATA interface	-
5.Flash MEMORY INTERFACE	7
6.MISCELLANEOUS	7
FUNCTIONAL BLOCK	8
PAD/PIN ASSIGNMENT	9
1. PCI INTERFACE (50 pins)	10
2.FLASH INTERFACE (34 pins)	11
3.Serial bus Interface	12
4.MISCELLANEOUS	12
5.DFT test pins (2 pins)	13
6.POWER/GROUND	13
7. PIN NUMBER INDEX for PDC20319	15
8. ALPHANUMERIC INDEX of PDC20319	19
TEST MODE FOR PDC20319 SERIES	21
1.Pin scan mode	21
SERIAL BUS	22
REGISTERS DESCRIPTION	24
1.PCI configuration register	24
2.Power Management Register Block Definition	26
<i>Capability Identifier – Cap_ID (Offset = 60h)</i>	26
<i>Next Item Pointer – Next_Item_Ptr (Offset = 61h)</i>	26

<i>PMC – Power Management Capabilities (Offset = 62h)</i>	26
<i>PMCSR – Power Management Control/Status (Offset = 64h)</i>	27
<i>PMCSR_BSE – PMCSR PCI to PCI Bridge Support Extensions (Offset = 66h)</i>	28
<i>Data (Offset = 67h)</i>	28
3.Message Signaled Interrupts	29
<i>Capability ID (offset = 70h)</i>	29
<i>Next Pointer (offset 71h)</i>	29
<i>Message Control (offset 72h)</i>	29
<i>Message Address (offset 74h)</i>	31
<i>Message Data (offset 78h)</i>	31
4.Extended register	31
<i>HOST Module Control Register</i>	32
<i>XOR Module Control Register</i>	41
<i>ATA Timing & Control Register</i>	48
LIST OF EXTENDED REGISTERS	71
1.ATA Control Register (BA#0)	71
<i>Command Packet Control Register (BA#0/ BA #3)</i>	71
<i>IDE Channel 0 Timing & Control Register (Index_IDE0/ BA#3)</i>	72
<i>IDE Channel 1 Timing & Control Register (Index_IDE1/ BA#3)</i>	74
<i>IDE Channel 2 Timing & Control Register (Index_IDE2/ BA#3)</i>	75
<i>IDE Channel 3 Timing & Control Register (Index_IDE3/ BA#3)</i>	77
2.XOR Control Register	78
<i>XOR command package control register (BA#1/index_XOR/BA#3)</i>	78
<i>XOR register(index_XOR/ BA#3)</i>	79
3.Host Control register (BA#2/ BA3)	80
ATA/ HOST DMA PACKET AND SG FORMAT	82
1.ATA Packet (Variable size)	82
<i>Delay Sequence ID</i>	83
<i>Synchronization Sequence ID</i>	83
<i>ATA Packet Control</i>	83
<i>Host Memory Scatter/Gather Point (PSG)</i>	84
<i>Next Command Point (NCA)</i>	84
2.XOR Packet	88
<i>Delay Sequence ID</i>	88
<i>Synchronization Sequence ID</i>	89

<i>XOR Packet Command Control</i>	89
<i>Host Memory Scatter/Gather Point (PSGn)</i>	89
<i>Next Command Point (NCA)</i>	89
3.SG format (8 bytes)	90
<i>SG Address</i>	90
<i>SG Byte Count</i>	90
<i>Control bit definition</i>	90
MECHANICAL SPECIFICATION	92
DC/AC SPECIFICATION	95
1.Power Requirement	95
2.Absolute Maximum Rating	95
3.Recommended operating conditions	95
4.PCI I/O DC Characteristics	96
5.PCI I/O AC Characteristics	96

CHANGE HISTORY

Rev. 1.0: ----- 12 April 2003

INTRODUCTION

The PROMISE Technology PDC20319 series ASICs are PCI to SATA/ SATA RAID controllers, which have PCI bus mastering RAID 0/1/10/5 engine that supports hardware commands for ATA operation to accelerate SATA-RAID system. PDC20319 series have 4 channels SATA interface in one controller. It communicates with the PCI bus using burst bus mastering and advanced packet command based scatter/gather engine to enhance overall system performance. They satisfy the SATA 1.0 spec also. In addition, PROMISE Technology provides a 32-bit software driver that supports 32-bit operating system functionality. PDC20319 series include PDC20319 and PDC20318.

FEATURES

1. GENERAL

- Highly system level integration that available in a 144-pin LQFP adopting high speed COMS technology.
- Single chip, high performance SATA/ SATA-RAID implementation for easy integrated on to motherboards and occupying less board space in add-on card application.
- Built in 4 channels SATA PHY, which satisfy SATA 1.0 specification and can transfer data with 1.5GHz speed.
- Capable to support multiple arrays and quad master mode for dedicated SATA channel, up to four physical drive can operated at master mode.
- Quad independent data paths with read ahead and write posting supported for quad SATA channels to have high performance.
- Bus mastering design takes full advantage of multi-tasking, multi-threading operating systems and greatly improves performance.
- Provides Memory Mapped-I/O programming interface to improve command setting up performance, and that can be applied to some platforms even which without I/O space addressing capability.

2. PCI INTERFACE

- PCI interface that complies with PCI Local Bus Specification Revision 2.3.

- Provides PCI Power Management 1.1 capability.
- Support PCI MEMORY WRITE INVAIDATE, READ CASHE LINE and READ MULTIPULE command to rising PCI efficiency.
- Support PCI MSI(Message signal interrupt) feature, which save time of interrupt handling.
- Supports 32-bit PCI bus master with zero wait burst protocol, bus speed up to 66 MHz and provides 267 MB/sec sustained transfer rate.
- Supports full set of configuration headers for easy implementation of plug and play BIOS features.
- Sub-system vendor ID & sub-system device ID are preloaded, which will be automatic, fetched from local flash memory after system RESET#.

3. RAID ENGINE

- Provides advance chained packet commands for XOR and four independent SATA operations.
- Allows software mechanism to implement ATA elevator sorting algorithm.

□

4. SATA interface

- Integrated four 1.5 GHz PHY which satisfy SATA 1st generation specification.
- High signal quality, excellent compatibility with SATA hard drive.
- Support SATA power save mode.
- Support plug/play operation and can generate interrupt for software handling.

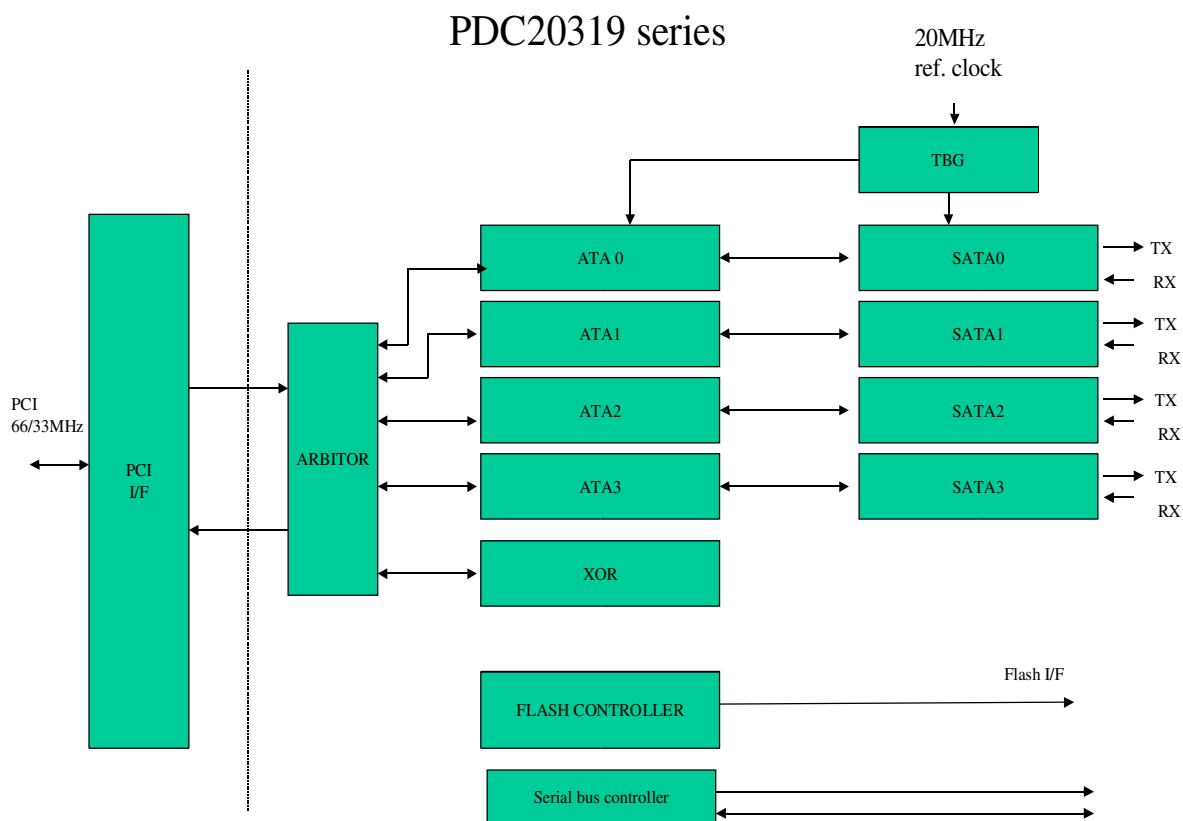
5. Flash MEMORY INTERFACE

Interface to external flash memory up to 8M byte.

6. MISCELLANEOUS

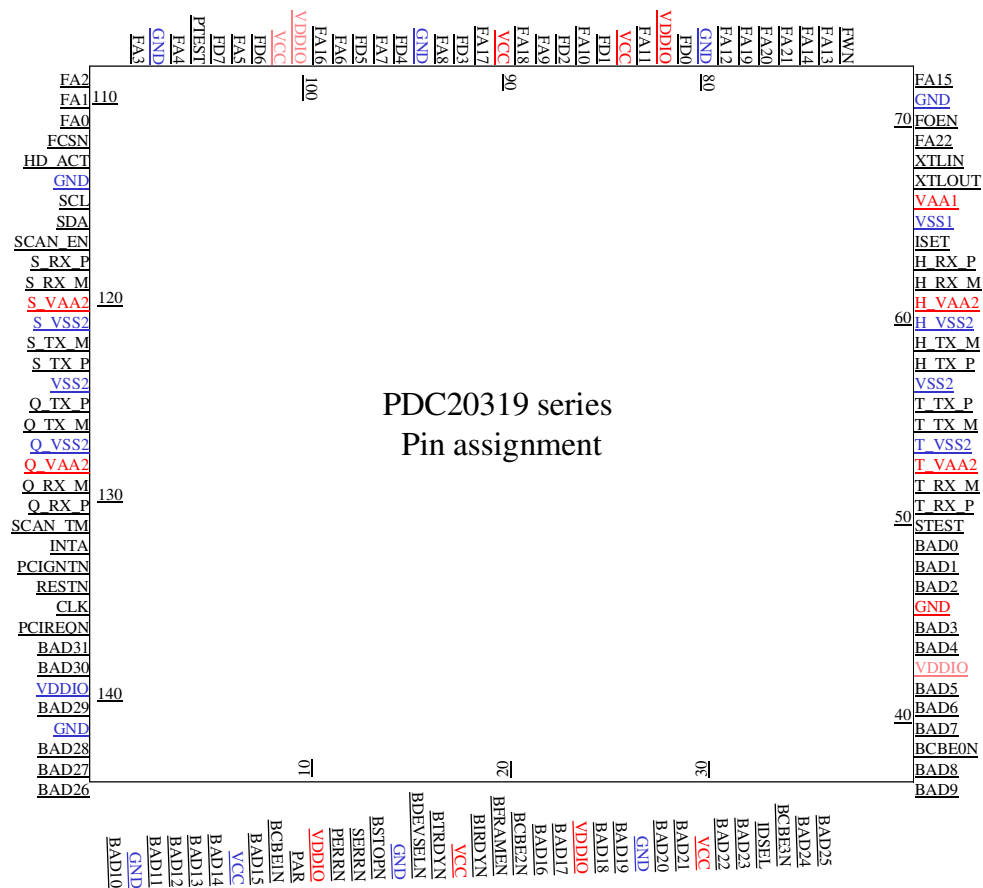
- Building one serial bus for enclosure control.
- Compliance with the PC2000, WHQL hardware requirements.
- Direct control to optional external BIOS that allows it to support 48-bit LBA format drives larger than 128GB.
- Build in pin scan function for PCB testing easily and DFT circuit to guarantee ASIC quality.

Functional Block



Pad/pin assignment

Type	Abbreviation
Input	I
Output	O
Tri-state or bi-directional	T/S
Sustained Tri-state	S/T/S
Open Drain	O/D
Power	VCC
Ground	GND



1. PCI INTERFACE (50 pins)

Name	Type	Description
BAD[31:0]	T/S	Address and Data: PCI AD bus.
CLK	I	PCI Clock: All other PCI signals, except RESETN and INTAN, are sampled on the rising edge of CLK, and all other timing parameters are defined with respect to this edge. Operate up to 66 MHz.
INTAN	O/D	Interrupt A: This signal is used to request an interrupt to host. This signal is tri-stated when no interrupt asserted.
RESETN	I	System Reset: This signal is system power-on reset signal, active low, used to set the internal registers, sequencers, and signals of the PDC20319 to an initial state.
PCIGNTN	I	PCI Bus Grant: '0' indicates that access to the bus has been granted.
PCIREQN	T/S	PCI Bus Request: This signal indicates to the system arbiter that this PDC20319 controller desires use of the bus while PCIREQN asserted to '0'.
BCBE[3:0]N	T/S	Bus Command and Byte Enable: PCI C/BE bus, Indicate command in address phase and byte enable in data phase
IDSEL	I	Initialization Device Select: This signal is used as a chip select during configuration read and writes transaction.
BFRAMEN	S/t/s	Cycle Frame: This signal is driven by the current master to indicate the beginning and duration of an access. BFRAMEN is asserted, data transfers continue. When BFRAMEN is de-asserted, the transaction is in the final data phase.

BIRDYN	S/T/S	Initiator Ready: This signal indicates the initiating bus master ability to complete the current data phase of the transaction.
BTRDYN	S/T/S	Target Ready: This signal indicates the initiating selected device ability to complete the current data phase of the transaction.
BDEVSELN	S/T/S	Device Select: Driving low indicates the driving device has decoded its address as the target of the current access. As input, it indicates to a master whether any device on the bus has been selected.
BSTOPN	S/T/S	Stop: This signal indicates the current selected target is requesting the master to stop the current transaction.
PAR	T/S	Parity: This signal is even parity across BAD[31:0] and BCBE[3:0]N PDC20319 drives PAR for address and write data phase as master.
PERRN	S/T/S	Parity Error: this signal reports data parity errors during all PCI transactions except a Special Cycle.
SERRN	O/D	System Error: this signal reports address parity errors, data parity errors on the Special Cycle command, command, or any other system error where the result will be catastrophic.

2. FLASH INTERFACE (34 pins)

Name	Type	Description
FWN	O	Write Enable: It is the write enable of Flash memory.
FOEN	O	Output Enable: It is the output enable of Flash memory.

FCSN	O	Chip Select: This signal is used to select a Flash memory chip when host access to external BIOS.
FA22 – FA0	T/S	Address pin of flash memory.
FD7 – FA0	T/S	Data pins of flash memory.

3. Serial bus Interface

Name	Type	Description
SCL	O/D	Serial bus clock: clock of serial bus interface.
SDA	O/D	Serial bus data: data pin of serial bus interface

4. MISCELLANEOUS

Name	Type	Description
HD_ACT	O/D	Hard drive active: signal to indicate the hard drive is accessed.
XTLIN	I	Reference clock: reference clock input or crystal input (20MHz)
XTLOUT	O	Crystal output: output of crystal
ISSET	I	Bias current Resister: A 12.1K ohm resister is connected between this pin and the nearest digital GND pin

STEST	I	Test mode: set this pin to “1” make the chip enter test mode
PTEST	I	Test mode: set this pin to “1” make the chip enter test mode

5. DFT test pins (2 pins)

Name	Type	Description
DFT_TM	I/PD	DFT test mode: force chip to DFT test mode.
DFT_SE	I/PD	DFT scan enable: scan enable signal in DFT test mode.

6. POWER/GROUND

Name	Type	Description
VDDIO	PWR	Power for input pad and core logic: connected to 3.3 volts
VCC	PWR	Power for core logic: connected to 1.8 volts
GND	GND	Ground for logic output pad
VAA1	PWR	TBG Analog power : connected to 3.3 volts
VSS1	GND	TBG analog ground.: connected to analog ground power plane
VAA2	PWR	PHY analog power: connected to 3.3 volts

VSS2	GND	PHY analog ground: connected to analog ground plane
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7. PIN NUMBER INDEX for PDC20319

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	BAD25	37	BAD9	73	FWN	109	FA2
2	BAD24	38	BAD8	74	FA13	110	FA1
3	BCBE3N	39	BCBE0N	75	FA14	111	FA0
4	IDSEL	40	BAD7	76	FA21	112	FCSN
5	BAD23	41	BAD6	77	FA20	113	HD_ACT
6	BAD22	42	BAD5	78	FA19	114	GND
7	VCC	43	VDDIO	79	FA12	115	SCL
8	BAD21	44	BAD4	80	GND	116	SDA
9	BAD20	45	BAD3	81	FD0	117	SCAN_EN
10	GND	46	GND	82	VDDIO	118	S_RX_P
11	BAD19	47	BAD2	83	FA11	119	S_RX_M
12	BAD18	48	BAD1	84	VCC	120	S_VAA2
13	VDDIO	49	BAD0	85	FD1	121	S_VSS2
14	BAD17	50	STEST	86	FA10	122	S_TX_M
15	BAD16	51	T_RX_P	87	FD2	123	S_TX_P
16	BCBE2N	52	T_RX_M	88	FA9	124	S_VSS2
17	BFRAMEN	53	T_VAA2	89	FA18	125	Q_TX_P
18	BIRDYN	54	T_VSS2	90	VCC	126	Q_TX_M
19	VCC	55	T_TX_M	91	FA17	127	Q_VSS2

20	BTRDYN	56	T_TX_P	92	FD3	128	Q_VAA2
21	BDEVSELN	57	VSS2	93	FA8	129	Q_RX_M
22	GND	58	H_TX_P	94	GND	130	Q_RX_P
23	BSTOPN	59	H_TX_M	95	FD4	131	SCAN_TM
24	SERRN	60	VSS2	96	FA7	132	INTA
25	PERRN	61	VAA2	97	FD5	133	PCIGNTN
26	VDDIO	62	H_RX_M	98	FA6	134	RESTN
27	PAR	63	H_RX_P	99	FA16	135	CLK
28	BCBE1N	64	ISSET	100	VDDIO	136	PCIREQN
29	BAD15	65	VSS1	101	VCC	137	BAD31
30	VCC	66	VAA1	102	FD6	138	BAD30
31	BAD14	67	XTLOUT	103	FA5	139	VDDIO
32	BAD13	68	XTLIN	104	FD7	140	BAD29
33	BAD12	69	FA22	105	PTEST	141	GND
34	BAD11	70	FOEN	106	FA4	142	BAD28
35	GND	71	GND	107	GND	143	BAD27
36	BAD10	72	FA15	108	FA3	144	BAD26



8. ALPHANUMERIC INDEX of PDC20319

49	BAD0	21	BDEVSELN	102	FD6	122	S_TX_M
48	BAD1	17	BFRAMEN	104	FD7	123	S_TX_P
36	BAD10	18	BIRDYN	70	FOEN	120	S_VAA2
34	BAD11	23	BSTOPN	73	FWN	121	S_VSS2
33	BAD12	20	BTRDYN	10	GND	124	S_VSS2
32	BAD13	135	CLK	22	GND	117	SCAN_EN
31	BAD14	111	FA0	35	GND	131	SCAN_TM
29	BAD15	110	FA1	46	GND	115	SCL
15	BAD16	86	FA10	71	GND	116	SDA
14	BAD17	83	FA11	80	GND	24	SERRN
12	BAD18	79	FA12	94	GND	50	STEST
11	BAD19	74	FA13	107	GND	52	T_RX_M
47	BAD2	75	FA14	114	GND	51	T_RX_P
9	BAD20	72	FA15	141	GND	55	T_TX_M
8	BAD21	99	FA16	62	H_RX_M	56	T_TX_P
6	BAD22	91	FA17	63	H_RX_P	53	T_VAA2
5	BAD23	89	FA18	59	H_TX_M	54	T_VSS2
2	BAD24	78	FA19	58	H_TX_P	66	VAA1
1	BAD25	109	FA2	113	HD_ACT	61	H_VAA2
144	BAD26	77	FA20	4	IDSEL	7	VCC

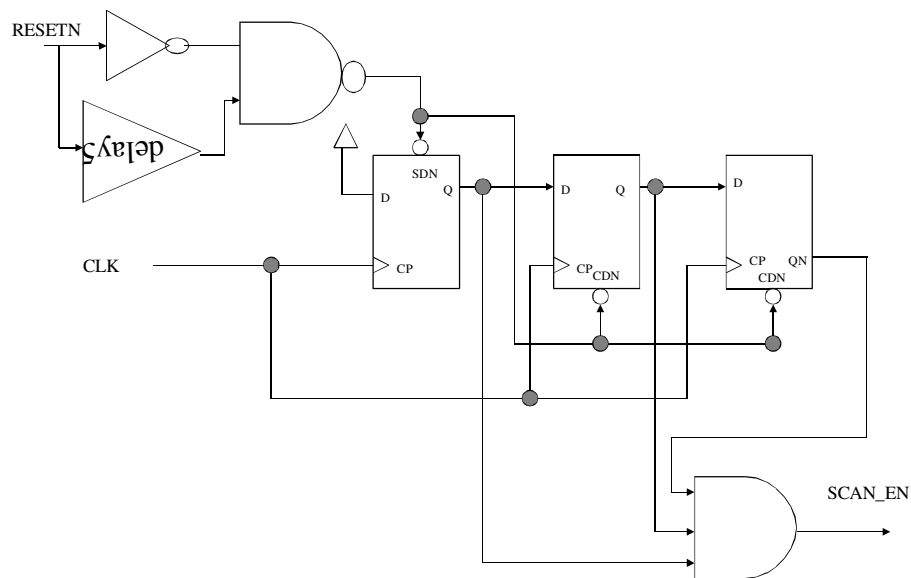
143	BAD27	76	FA21	132	INTA	19	VCC
142	BAD28	69	FA22	64	ISSET	30	VCC
140	BAD29	108	FA3	27	PAR	84	VCC
45	BAD3	106	FA4	105	PTEST	90	VCC
138	BAD30	103	FA5	133	PCIGNTN	101	VCC
137	BAD31	98	FA6	136	PCIREQN	82	VDDIO
44	BAD4	96	FA7	25	PERRN	100	VDDIO
42	BAD5	93	FA8	129	Q_RX_M	13	VDDIO
41	BAD6	88	FA9	130	Q_RX_P	26	VDDIO
40	BAD7	112	FCSN	126	Q_TX_M	43	VDDIO
38	BAD8	81	FD0	125	Q_TX_P	139	VDDIO
37	BAD9	85	FD1	128	Q_VAA2	65	VSS1
39	BCBE0N	87	FD2	127	Q_VSS2	57	VSS2
28	BCBE1N	92	FD3	134	RESTN	60	H_VSS2
16	BCBE2N	95	FD4	118	S_RX_P	68	XTLIN
3	BCBE3N	97	FD5	119	S_RX_M	67	XTLOUT



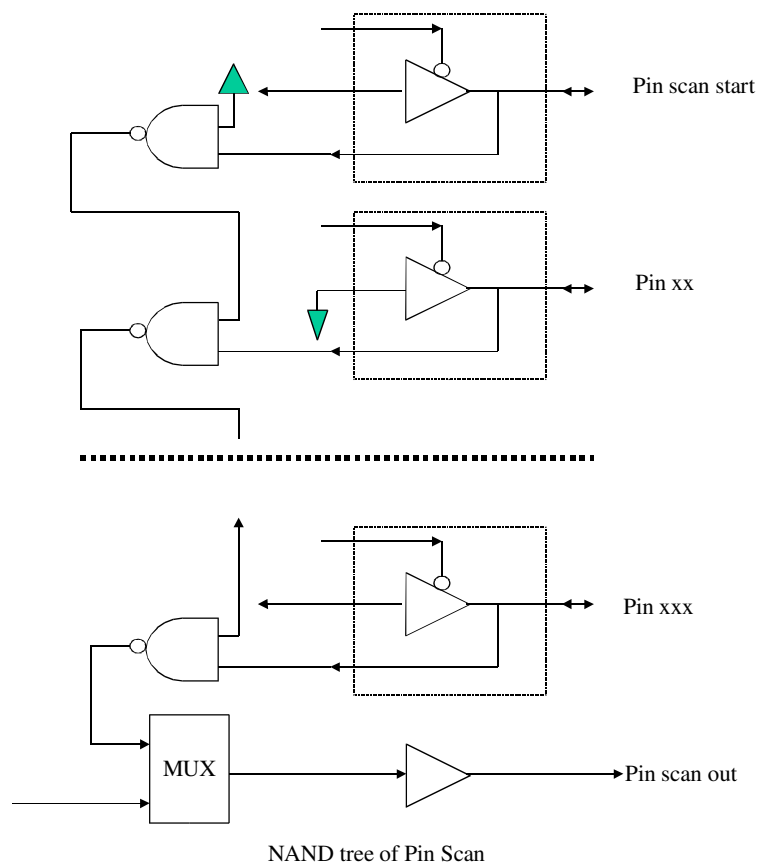
Test mode for PDC20319 series

1. Pin scan mode

PDC20319 series has pin scan mode. The functional diagram of pin scan enable is as following diagram.
After PCI RESTB assert, the ASIC enter pin scan mode after the first PCI clock rising edge, and quit from the mode after the secondary PCI clock rising edge.



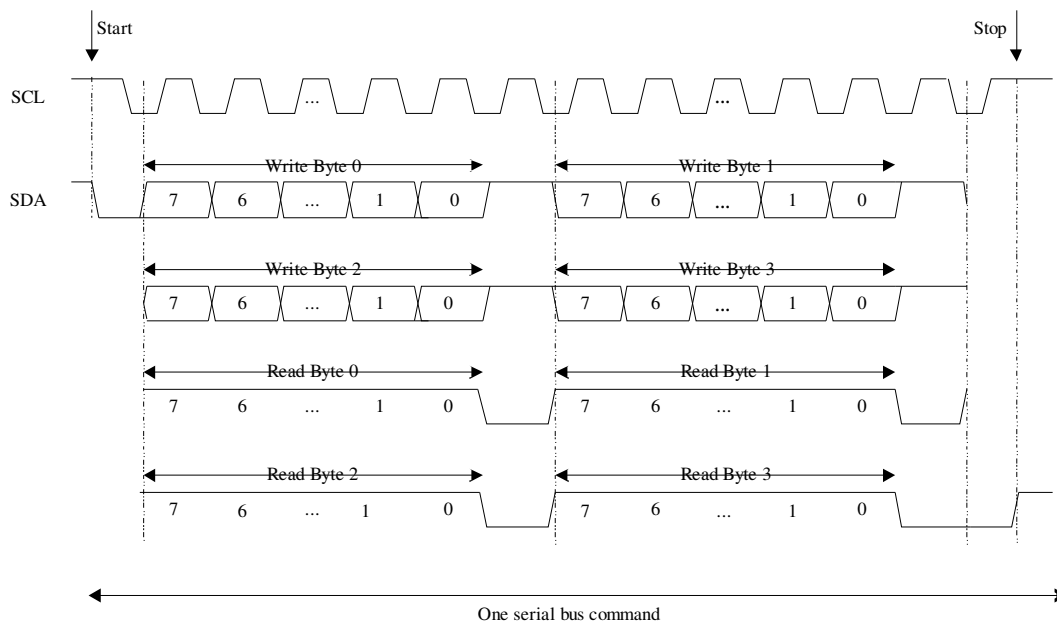
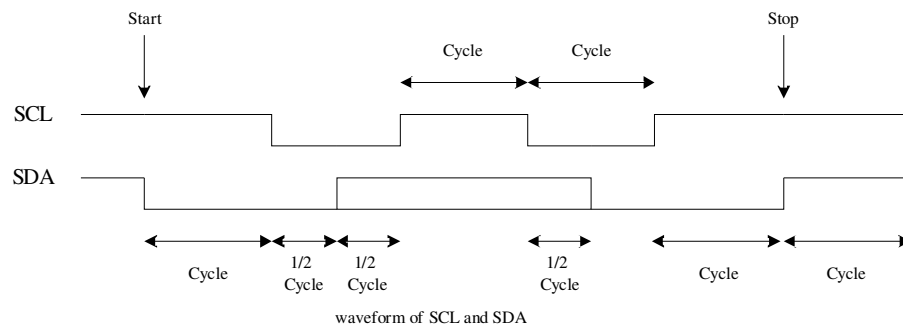
Function diagram of pin scan enable



In pin scan mode, only one pad is output pad. See the function diagram. The pin scan start from RESTB and output to HD_ACT

Serial bus

PDC20319 series support serial bus interface to communicate with external device for enclosure control (temperature, fan etc.). The base clock of Serial bus (SER_CLK) is PLL output clock drive 2^6 . In normal operation, it is $150\text{MHz}/2^6$. The SER_CYC(BA#2:50h | BA3# + 0x50h bit 3-0) defines how many SER_CLK to be a serial bus cycle. A high/low pulse of SCL is equal a SER_CYCLE. The waveform of SCL and SDA is as following diagram. The start bit and stop bit are generated by serial bus controller. The SER_WC and SER_RC(BA#2:50h | BA3# + 0x50h) define how many data will be sent and received from the serial bus. The maximum write/read size is 4 bytes. The SER_TDATA(BA#2: 54h|BA#3 + 54h) defines the data to be transferred and SER_RDATA(BA#2: 58h | BA#3 + 54h) define the received data. After writing the byte 0 of SER_TDATA, the serial bus controller start to transfer/receive data. It transfers data first then receive data if SER_RC isn't equal zero. The diagram is as following. SCL and SDA are open-drain I/O pins. They need pull high resistor externally.



REGISTERS DESCRIPTION

The following illustrated programmable registers defined in PDC20319.

1. PCI configuration register

Offset	[31:24]	[23:16]	[15:8]	[7:0]
00h	Device ID (33xxx)		Vendor ID (105Ah)	
04h	Status (0230h)		Command (0000h)	
08h	Class Code (01xx00h)			Revision ID (02h)
0Ch	Reserved	Header Type (00h)	Latency Timer (00h)	CacheLine Size (00h)
10h	Base Address register #0, for ATA BA#0 (8001h) 64 byte			
14h	Base Address register #1, for XOR BA#1 (8101h) 16 byte			
18h	Base Address register #2, for HOST BA#2(8201h) 128 byte			
1Ch	Base Address register #3, for memory resources (Memory mapped I/O) BA#3(800000h) 4K byte			
20h	Base Address register #4, for FLASH BA#4(900000h) 128k byte Base Address register #5 (Reserved)			
24h				

2Ch	Sub-System Device ID (33xxxh)		Sub-System Vendor ID (105Ah)	
30h	Expansion ROM Register (00080000h)			
34h	Reserved			Cap_Ptr (60h)
3Ch	Max_LAT (12h)	Min_GNT (04h)	Interrupt Pin (01h)	Interrupt Line (0Eh)
60h	Power Management Capabilities (0222h)		Next Item Ptr (70h)	Capability ID (01h)
64h	Data (00h)	PMCSR_BSE Bridge Support Extensions (00h)	Power Management Control/Status Register	
70h	Message control (0004h)		Next Item Ptr (00h)	Capability ID (05h)
74h	Message address			
78h			Message data	
Others	Reserved			

Device ID	Class Code	ASIC name
3318	018000	PDC20318
3319	010400	PDC20319

- Latency Timer “00h” that implied burst disabled, so software have to check this register when chip initialization.
- *Italic that indicates Read Only field.* Highlight with pink color is RESET# default value.
- .
- There is INT disable bit in command register bit 10. This bit is defined by PCI 2.3 spec. write 1 to this bit will disable interrupt.

2. Power Management Register Block Definition

The definition of following register can refer PCI Bus Power Management Interface Specification

Capability Identifier – Cap_ID (Offset = 60h)

Bits	Value	Type	Description
7:0	01h	R	<i>ID – This field, when “01h” identifies the linked list item as being the PCI Power Management registers.</i>

Next Item Pointer – Next_Item_Ptr (Offset = 61h)

Bits	Value	Type	Description
7:0	x0h	R	<i>Next Item Pointer – This field provides an offset into the function’s PCI Configuration Space pointing to the location of next item in the function’s capability list. If the MSI function is enable, the value is 70h, otherwise, it is 00h.</i>

PMC – Power Management Capabilities (Offset = 62h)

Bits	Value	Type	Description
15:11	00000 b	R	<i>PME_Support –No PME# supported.</i>

10	0b	R	D2_Support – Do not support D2.
9	1b	R	D1_Support – supports the D1 Power Management State.
8:6	000b	R	Reserved
5	1b	R	DSI – requires a device specific initialization sequence following transition to the D0 uninitialized state.
4	0b	R	Reserved
3	0b	R	PME Clock – No PME# supported.
2:0	010b	R	Version – Complies with Revision 1.1 of the PCI Power Management Interface Specification.

PMCSR – Power Management Control/Status (Offset = 64h)

Bits	Value	Type	Description
15	0b	Read Only	PME_Status – No PME# supported, always return 0.
14:13	00b	Read Only	Data_Scale – not implement.
12:9	0000b	Read Only	Data_Select – not implement
8	0b	Read Only	PME_En – PME# assertion is not implemented.
7:2	000000b	Read Only	Reserved

1:0	RRb "R" for Register Value	Read/ Write	<p>PowerState – This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below.</p> <p>00b – D0 01b – D1 10b – D2 11b – D3 hot</p> <p>If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.</p> <p>Any state other than D0 will stop the internal clock of PDC20319.</p>
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PMCSR_BSE – PMCSR PCI to PCI Bridge Support Extensions (Offset = 66h)

PMCSR_BSE supports PCI bridge specific functionality and is required for all PCI-to-PCI bridges.

Bits	Value	Type	Description
7	0b	R	BPCC_En (Bus Power/Clock Control Enable) – not implement.
6	0b	R	B2_B3# (B2/B3 support for D3 _{hot}) – not implement.
5:0	000000b	R	Reserved

Data (Offset = 67h)

Bits	Value	Type	Description
7:0	00h	R	Data – not implement.

3. Message Signaled Interrupts

Capability ID (offset = 70h)

Bit	Value	Type	Description
7:0	CAP_ID (05h)	R	The value of 05h in this field identifies the function as message signaled interrupt capable. This field is read only.

Next Pointer (offset 71h)

Bit	Value	Type	Description
7:0	NXT_PTR (00h)	R	Pointer to the next item in the capabilities list. Must be NULL for the final item in the list.

Message Control (offset 72h)

Bit	Value	Type	Description
15:8	Reserved (00h)	R	Always returns 0 on a read operation.
7	64 bit address capable (0b)	R	0, no 64 bit message address.

6:4	Multiple Message Enable	R/W	<p>System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. If a function requests four messages (indicated by a Multiple Message Capable encoding of “010”), system software can allocate either four, two, or one message by writing a “010”, “001, or “000” to this field, respectively. When MSI is enabled, a device will be allocated at least 1 message. The encoding is defined as: Encoding # of messages allocated</p> <p>000 1 001 2 010 4 011 8 100 16 101 32 110 Reserved 111 Reserved</p> <p>This field’s state after reset is “000”.</p>
3:1	Multiple Message Capable	R	<p>System software reads this field to determine the number of requested messages. The number of requested messages must be aligned to a power of two (if a function requires three messages, it requests four by initializing this field to “010”). The encoding is defined as:</p> <p>Encoding # of messages requested</p> <p>The value is</p> <p>010 4</p> <p>PDC20319 requests 4 messages.</p>
0	MSI Enable	R/W	<p>If 1, the function is permitted to use MSI to request service and is prohibited from using its INTx# pin (if implemented). System configuration software sets this bit to enable MSI. A device driver is prohibited from writing this bit to mask a function’s service request. If 0, the function is prohibited from using MSI to request service. This bit’s state after reset is 0 (MSI is disabled).</p>

Message Address (offset 74h)

Bit	Value	Type	Description
31:2	Message Address	R/W	System-specified message address. If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register specify the DWORD aligned address

Message Data (offset 78h)

Bit	Value	Type	Description
15:0	Message Data	R/W	<p>If the Message Enable bit (bit 0 of the Message Control register) is set, if the Multiple Message Enable field (bits 6-4 of the Message Control register) Is 010, then the message data means</p> <p>Data :interrupt from packet command.</p> <p>Data +1: interrupt from Serial bus</p> <p>Data +2: interrupt from Force interrupt register.</p> <p>Data +3: interrupt from plug and control register</p>

4. Extended register

There are extended registers for control and timing adjustment. All of these register can be accessed by Memory mapped I/O or index I/O (addressing by index register and data register contents data). The base address of memory mapped I/O is at PCI configuration register, offset 0x1Ch, BA#3. When these registers are accessed by index I/O, users must program index register first then R/W the data register and program these registers by double word. **Only double word command is allowed.** The location of index address port and index data port is as following

Base address	Offset	
BA#0	08h	Index_IDE0 : index address port of IDE0

BA#0	0Ch	Index data port of IDE0
BA#0	18h	Index_IDE1: index address port of IDE1
BA#0	1Ch	Index data port of IDE1
BA#0	28h	Index_IDE2: index address port of IDE2
BA#0	2Ch	Index data port of IDE2
BA#0	38h	Index_IDE3: index address port of IDE3
BA#0	3Ch	Index data port of IDE3
BA#1	08h	Index_XOR: index address port of XOR
BA#1	0Ch	Index data port of XOR

HOST Module Control Register**Sequence Counter Control Register #0 - #F (BA#2: 0h – 3Ch| BA#3 + 000h – 03Ch)**

7	6	5	4	3	2	1	0
Reserved	Reserved	SEQ INT Mask (1b)	SEQ CNT				

15	14	13	12	11	10	9	8
Reserved							

23	22	21	20	19	18	17	16
Reserved			X Error	A3 Error	A2 Error	A1 Error	A0 Error

31	30	29	28	27	26	25	24
Reserved							

There are 16 sequence counter control registers.

Bit[31:21]: Reserved

Bit[20]: X Error. It indicates an error condition is generated in XOR engine.

Bit[19]: A3 Error. It indicates an error condition is generated in ATA3.

Bit[18]: A2 Error. It indicates an error condition is generated in ATA2.

Bit[17]: A1 Error. It indicates an error condition is generated in ATA1.

Bit[16]: A0 Error. It indicates an error condition is generated in ATA0.

Bit[15:6]: Reserved.

Bit[5]: Sequence Interrupt Mask. When this bit is set, it will mask an interrupt generated by the sequence counter.

Bit[4:0]: Sequence Counter. It indicates how many engines run in this RAID sequence. It will collect all interrupts generated by those engines that run in this sequence ID. The sequence counter will count down for each interrupt, which belongs to this sequence ID arrives. If it counts to zero, all interrupts generated by those engines will pass through to PCI bus.

Sequence Interrupt Status register (BA#2: 40h | BA#3 + 040h)

7 (r)	6 (r)	5 (r)	4 (r)	3(r)	2(r)	1(r)	0(r)
SEQ#7 INT	SEQ#6 INT	SEQ#5 INT	SEQ#4 INT	SEQ#3 INT	SEQ#2 INT	SEQ#1 INT	SEQ#0 INT
15 (r)	14 (r/w)	13 (r/w)	12 (r/w)	11 (r/w)	10 (r/w)	9 (r/w)	8 (r/w)
SEQ#F INT	SEQ#E INT	SEQ#D INT	SEQ#C INT	SEQ#B INT	SEQ#A INT	SEQ#9 INT	SEQ#8 INT
23 (r)	22 (r)	21 (r)	20 (r)	19 (r)	18 (r)	17 (r)	16 (r)
Reserved							
31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)

Reserved

Bit[31:16]: Reserved.

Bit[15]: SEQ#F Interrupt. It indicates whether the SEQ#F interrupt is generated.

Bit[14]: SEQ#E Interrupt. It indicates whether the SEQ#E interrupt is generated.

Bit[13]: SEQ#D Interrupt. It indicates whether the SEQ#D interrupt is generated.

Bit[12]: SEQ#C Interrupt. It indicates whether the SEQ#C interrupt is generated.

Bit[11]: SEQ#B Interrupt. It indicates whether the SEQ#B interrupt is generated.

Bit[10]: SEQ#A Interrupt. It indicates whether the SEQ#A interrupt is generated.

Bit[9]: SEQ#9 Interrupt. It indicates whether the SEQ#9 interrupt is generated.

Bit[8]: SEQ#8 Interrupt. It indicates whether the SEQ#8 interrupt is generated.

Bit[7]: SEQ#7 Interrupt. It indicates whether the SEQ#7 interrupt is generated.

Bit[6]: SEQ#6 Interrupt. It indicates whether the SEQ#6 interrupt is generated.

Bit[5]: SEQ#5 Interrupt. It indicates whether the SEQ#5 interrupt is generated.

Bit[4]: SEQ#4 Interrupt. It indicates whether the SEQ#4 interrupt is generated.

Bit[3]: SEQ#3 Interrupt. It indicates whether the SEQ#3 interrupt is generated.

Bit[2]: SEQ#2 Interrupt. It indicates whether the SEQ#2 interrupt is generated.

Bit[1]: SEQ#1 Interrupt. It indicates whether the SEQ#1 interrupt is generated.

Bit[0]: SEQ#0 Interrupt. It indicates whether the SEQ#0 interrupt is generated.

The Interrupt will be cleared when Bit[15:0] is read

Flash Control Register (BA#2: 44h | BA#3 + 044h)

15:8(r/w)	7:0 (r/w)
reserved	Reserved

31: 30 (r/w)	29:26 (r/w)	25:24 (r/w)	23:18 (r/w)	17 (r/w)	16 (r/w)
TFAS (11b)	TFPW (1111b)	TFAH (11b)	FPAGE (000000b)	Reserved	FIFO_SHD (0b)

Bit[31:30]: FLASH Address setup time. It defines the minimum time from address valid and FCSN low to FOEN or FWN low.

Bit[29:26]: FLASH Minimum pulse width. It is the minimum pulse width of FOEN and FWN.

Bit[25:24]: FLASH Address hold time. It defines the minimum time from FOEN or FWN high to address transition and FCSN high.

Bit[23:18]: FLASH PAGE control. It helps to access FLASH memory space beyond 128Kbytes and up to 8Mbytes. These bit affect FA[22:17] directly.

Bit[17] : Reserved

Bit[16]: FIFO THRESHOLD register. It indicates the threshold depth of ATA data FIFO during UDMA WRITE.

”0”: Request to transfer data while FIFO depth is less than 16 DW.

”1”: Request to transfer data while FIFO depth is less than 8 DW.

Bit[15:0]: reserved

PCI Control & Status register (BA#2: 48h | BA#3 + 048h)

7 (r)	6(r)	5 (r)	4 (r)	3:2 (r)	1:0 (r/w)
reserved	Sub-system ID Read Only	FLASH MEMORY BIOS ENABLE	Initial state for IO /memory /PCI master /BIOS	BIOS size	reserved

15(r/w)	14(r/w)	13(r/w)	12(r/w)	11 :8
4 th Software Reset (1)	3 rd Software Reset (1)	Secondary Software Reset (1)	Primary Software Reset (1)	reserved

31:16
Reserved

Bit[31:16]: reserved

Bit[15]: 4th ATA channel Software Reset. Writing ‘0’ to this bit will reset the 4th channel devices.

Bit[14]: 3rd ATA channel Software Reset. Writing ‘0’ to this bit will reset the 3rd channel devices.

Bit[13]: Secondary ATA channel Software Reset. Writing ‘0’ to this bit will reset the secondary channel devices.

Bit[12]: Primary ATA channel Software Reset. Writing ‘0’ to this bit will reset the primary channel

- devices.
- Bit[11:8]: reserved.
- Bit[7]: reserved.
- Bit[6]: This bit indicates whether the Sub-system ID and Sub-system Vender ID are Read Only
- Bit[5]: this bit indicate flash memory is disable.
1: Enable FLASH MEMORY BIOS and flash memory can be accessed.
0: Disable flash memory.
This bit will override the definition of bit4.
- Bit[4]: the initial state of PCI device's IO/Memory/bus master (PCI command register bit0,1,2) / BIOS (expansion ROM base address register bit0).
1:enable
0:disable
- Bit[3:2]: BIOS size.
00: 16K
01: 32K
10: 64k
11: 128k
- Bit[1:0]: reserved

Serial bus control Register (BA#2: 50h | BA#3 +050h)

7 :4	3:0(r/w)
reserved	SER_CYC[3:0] (0xFh)

15:13	12 (r/w)	11(r/w)	10(r/w)	9(r/w)	8(r/w)
R	Mask ERR	Mask Finish	ERR (0)	FINISH (0)	SER_RST (0)

31:27(r/w)	26:24(r/w)	23:19(r/w)	18:16(r/w)
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Reserved	SER_WCNT[2:0] (0)	Reserved	SER_RCNT[2:0] (0)
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- Bit[31:27]: reserved
- Bit[26:24]: SER_WCNT: serial bus transfer count. The register defines the number of data to be transferred. The maximum number is 0x4h.
- Bit[23:19]: reserved
- Bit[18:16]: SER_RCNT: serial bus receive count. The register defines the number of data to be received by serial bus. The maximum value is 0x4h.
- Bit[15:13]: reserved.
- Bit[12]: Mask ERR interrupt. “1”: no interrupt is generated by ERR flag, but the value of ERR is still set if error happened
- Bit[11]: MASK Finish interrupt. “1”, No interrupt is generated by FINISH flag, but the value of FINISH still set if serial bus finish transfer.
- Bit[10]: ERR: serial bus transfer/receive error. If there are error during the serial bus transfer, the ERR bit will set to “1” and an interrupt will be generated to PCI bus. Write “1” to the bit will clear the flag.
- Bit[9]: FINISH. Serial bus transfer/receive data finish. After serial bus transfer/receive finish, it generates an interrupt to PCI bus. Write “1” to the bit will reset the finish flag, and clear the interrupt.
- Bit[8]: SER_RST: write “1” to reset the serial bus state machine.
- Bit [7:4]: reverse
- Bit[3:0]: SER_CYC: serial bus cycle time. The clock of serial bus(SER_CLK) is PLL output clock divides 2^6 . The SER_CYC defines how many of SER_CLK to be a SCL cycle time.

Serial bus transfer data Register (BA#2: 54h | BA#3 +054h)

31:0 (r/w)
SER_TDATA

- Bit[31:0]: the data to be transferred by serial bus. The transfer sequence is MSB first, low byte first. When the SER_RCNT and SER_WCNT are not zero, the serial bus state machine will transfer data first then received data.
- In application, BYTE0 can be treated as COMMAND/ADDRESS register and the other 3 bytes are parameter/data registers.
- Write the BYTE0 will start a serial bus command with up to 3 parameter/data to be transferred.

Serial bus receive data Register (BA#2: 58h | BA#3 +058h)

31:0 (r/w)
SER_RDATA

Bit[31:0]: the data to be received by serial bus. The received sequence is MSB first, low byte first.

Extra data Register #0 (BA#2: 5Ch | BA#3 +05Ch)

31(r/w)	30:0 (r/w)
INT_FORCE	EXT_REG0

Bit[31]: INT_FORCE bit. Write a “1” to make an Interrupt Request to PCI HOST and write a “0” to clear it.

Bit[30:0]: Extra data Register #0.

Extra data Register #1 (BA#2:60Ch | BA#3 +060h)

31:0 (r/w)
EXT_REG1

Bit[31:0]: Extra data Register #1.

Extra data Register #2 (BA#2: 64h | BA#3 +064h)

31:0 (r/w)
EXT_REG2

Bit[31:0]: Extra data Register #2.

MSI control register (BA#2: 68h | BA#3 +068h)

31:2	1(r/w)	0(r/w)
Reserved	Enable MSI hold (0)	Clear hold flag (0)

Bit[31:2]: reserved.

Bit1: enable MSI hold.

0: if MSI is enable, the message will be sent to host independently.

1: if MSI is enable, the message will be sent to host only if the clear hold flag is 0.

Bit 0 : clear hold flag. If the MSI is enable and Enable MSI hold is “1”, PDC20319 sends message immediately after interrupt happening and set this bit to 1 automatically. Software must write “1” to the register to clear the flag, then PDC20319 can send another message to host if there are another interrupt request.

SATA plug control and status register(BA#2: 6Ch | BA#3 + 06Ch)

15:12	11:8(r)	7:4 (r/w)	3:0(r/w)
Reserved	SATA connect well	Plug flag	Unplug flag

31:28	27:24	23:20(r/w)	19:16(r/w)
Reserved	reserved	Mask unplug INT (Fh)	Mask plug INT (Fh)

Bit[31:24]: reserved.

Bit [23:20]: mask unplug INT. when the bit is “1”, the corresponding plug interrupt will be masked, but the flag still work.

Bit [19:16] : mask plug INT. when the bit is “1”, the corresponding plug interrupt will be masked, but the flag still work.

Bit [11:8] xxx1 : SATA0 is well connected

Xx1x: SATA1 is well connected

X1xx: SATA2 is well connected.

1xxx: SATA3 is well connected.

Bit [7:4] xxx1: SATA0 is plugged again

xx1x: SATA1 is plugged again

x1xx: SATA2 is plugged again

1xxx: SATA3 is plugged again

when SATA cable is plugged again, the corresponding flag will be “1”. Write “1” to the bit can clear the flag. A interrupt will pass to host when any of the bits change to “1” if the corresponding mask plug INT is “0”

Bit [3:0] xxx1: SATA0 is disconnected.

 Xx1x: SATA1 is disconnected

 X1xx: SATA2 is disconnected

 1xxx: SATA3 is disconnected.

When SATA cable is disconnected, the corresponding flag will be “1”. Write “1” to the bit can clear the flag. A interrupt will pass to host when any of the bits change to “1” if the corresponding mask plug INT is “0”

XOR Module Control Register

XOR Command Packet Pointer Register (BA#1:0h | index_XOR: 00h | BA#3 + 180h)

31:2 (r/w)	1:0 (r/w)
Base address of Command Packet	Reserved(00)

Bit[31:2]: the register points the location of current XOR Command Packet. The XOR Command Packet Pointer must be DWORD aligned. When packet command is executed, this register can be updated by current NCA automatically when current XOR packet finishes. The XOR packet format can refer Section 9

Bit[1:0]: Reserved.

XOR Global Control & Status Register (BA#1:4h | index_XOR: 04h | BA#3 + 184h)

7(r/w)	6(r/w)	5(r)	4(r)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
Reserved							NCA Pause

15	14	13(r)	12	11	10(r)	9(r)	8(r)
Reserved	PSGx Active			Reserved	DH_ER R	SH_ERR	PH_ERR

23(r)	22 (r)	21(r)	20:18(r)	17(r)	16 (r)
reserved	PCI System Error	Compare Error	Reserved	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27:24 (r)
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Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved (0)
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Bit[31:30]: Reserved.

Bit[29]: Packet Command Cycle status.

Bit[28]: Delay Transaction Status. This command packet is executed on delay transaction.

Bit[27:23]: Reserved

Bit[22]: PCI System Error. PCI target abort or master abort protocol is happened. This bit can be clear by write 1 to XOR software Reset (index_XOR: 3Chl BA#3 + 1BCh, bit 11)

Bit[21]: Compare Error. It is the compare result of two data streams. If the data is not the same, this flag will be "1". This bit can be clear by write 1 to XOR software Reset (index_XOR: 3Chl BA#3 + 1BCh, bit 11)

Bit[20:18]: Reserved.

Bit[17]: Direct Command complete status.

Bit[16]: Packet Command complete status.

Bit[15]: Reserved.

Bit[14:12]: PSGx Active.

000: PSG0 Active.

001: PSG1 Active.

010: PSG2 Active.

011: PSG3 Active.

111: IDEL.

Others : Reserved.

Bit[11]: Reserved.

Bit[10]: DH_ERROR. "1" Indicates the PCI SYSTEM ERROR occurs while loading DATA. This bit can be clear by write 1 to XOR software Reset (index_XOR: 3Chl BA#3 + 1BCh, bit 11)

Bit[9]: SH_ERROR. "1" Indicates the PCI SYSTEM ERROR occurs while loading a S/G table. This bit can be clear by write 1 to XOR software Reset (index_XOR: 3Chl BA#3 + 1BCh, bit 11)

Bit[8]: PH_ERROR. "1" Indicates the PCI SYSTEM ERROR occurs while loading a packet command
This bit can be clear by write 1 to XOR software Reset (index_XOR: 3Chl BA#3 + 1BCh, bit 11)

Bit[7:1]: Reserved.

Bit[0]: NCA Pause. When this bit is set, the XOR engine will not execute the next command packet.

XOR Descriptor Table Pointer Register0 (index_XOR: 08h | BA#3 + 188h)

31:2 (r/w)	1:0 (r)
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Base address of Descriptor table. Corresponds to A[31:2]	00b
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The Descriptor Table must be DWORD aligned. When command packet is executed, this value can be loaded from PSG0 pointer of XOR command packet. It indicates the location of 1st S/G table of current XOR operation.

XOR Descriptor Table Pointer Register1 (index_XOR: 0Ch | BA#3 + 18Ch)

31:2 (r/w)	1:0 (r)
Base address of Descriptor table. Corresponds to A[31:2]	00b

The Descriptor Table must be DWORD aligned. When command packet is executed, this value can be loaded from PSG1 pointer of XOR command packet. It indicates the location of 2nd S/G table of current XOR operation

XOR Descriptor Table Pointer Register2 (index_XOR: 10h | BA#3 + 190h)

31:2 (r/w)	1:0 (r)
Base address of Descriptor table. Corresponds to A[31:2]	00b

The Descriptor Table must be DWORD aligned. When command packet is executed, this value can be loaded from PSG2 pointer of XOR command packet. It indicates the location of 3rd S/G table of current XOR operation

XOR Descriptor Table Pointer Register3 (index_XOR: 14h | BA#3 + 194h)

31:2 (r/w)	1:0 (r)
Base address of Descriptor table. Corresponds to A[31:2]	00b

The Descriptor Table must be DWORD aligned. When command packet is executed, this value is loaded from PSG3 pointer of XOR command packet. It indicates the location of 4th S/G table of current XOR operation

XOR #0 S/G Engine Address counter Register (index_XOR: 18h | BA#3 + 198h)

31:0 (r)

Value of S/G engine address counter

Bit[31:0]: The value of channel #0's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #0 S/G Engine byte count counter Register (index_XOR:1Ch | BA#3 + 19Ch)

31:16 (r)	15:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:16]: Reserved.

Bit[15:0]: The value of channel #0's S/G engine byte count counter . When test mode is set, the counter is broken to two 8bit counter and its value can be read from this register.

XOR #1 S/G Engine Address counter Register (index_XOR:20h | BA#3 + 1A0h)

31:0 (r)
Value of S/G engine address counter

Bit[31:0]: The value of channel #1's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #1 S/G Engine byte count counter Register (index_XOR:24h | BA#3 + 1A4h)

31:16 (r)	15:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:16]: Reserved.

Bit[15:0]: The value of channel #1's S/G engine byte count counter . When test mode is set, the counter is broken to two 8bit counter and its value can be read from this register.

XOR #2 S/G Engine Address counter Register (index_XOR: 28h | BA#3 + 1A8h)

31:0 (r)
Value of S/G engine address counter

Bit[31:0]: The value of channel #2's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #2 S/G Engine byte count counter Register (index_XOR:2Ch | BA#3 + 1Ach)

31:16 (r)	15:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:16]: Reserved.

Bit[15:0]: The value of channel #2's S/G engine byte count counter . When test mode is set, the counter is broken to two 8bit counter and its value can be read from this register.

XOR #3 S/G Engine Address counter Register (index_XOR: 30h | BA#3 + 1B0h)

31:0 (r)
Value of S/G engine address counter

Bit[31:0]: The value of channel #3's S/G engine address counter. When test mode is set, the counter is cut to four 8bit counters and its value can be read from this register.

XOR #3 S/G Engine byte count counter Register (index_XOR:34h | BA#3 + 1B4h)

31:16 (r)	15:0 (r)
Reserved	Value of S/G engine byte count counter

Bit[31:16]: Reserved.

Bit[15:0]: The value of channel #3's S/G engine byte count counter. When test mode is set, the counter is broken to two 8bit counter and its value can be read from this register.

XOR Next Command Packet Pointer Register (index_XOR: 38h | BA#3 + 1B8h)

31:2 (r/w)	1:0 (r/w)
Base address of Next Command Packet	Reserved(00)

Bit[31:2]: The XOR Next Command Packet Pointer must be DWORD aligned. The value is loaded from NCA pointer of XOR command packet. It indicates the location of next command packet address.

Bit[1:0]: Reserved.

XOR Control & Status Register (index_ XOR: 3Ch | BA#3 + 1BCh)

7(r/w)	6(r/w)	5 (r)	4 (r)	3(r/w)	2(r/w)	1(r/w)	0(r/w)
XOR Start/Stop	XOR Type	Reserved		Interrupt Sequence ID			

15:12 (r)	11	10	9	8
Reserved	XOR Software Reset	Mask INT (0)	Test Mode (0)	Reserved

23:16 (r)
Reserved

31 (r)	30 (r)	29:24 (r)
Data FIFO Empty	Control FIFO Empty	Reserved

- Bit[31]: Data FIFO empty. The data FIFO of XOR is empty
- Bit[30]: Control FIFO empty. The task FIFO of XOR is empty
- Bit[29:12]: Reserved.
- Bit[11]: This bit controls the XOR module software reset. Write '1' to this will reset XOR module.
- Bit[10]: Mask INT. When this bit is set, the interrupt from XOR controller will not pass to PCI.
- Bit[9]: XOR Controller Test Mode.
- Bit[8]: Reserved.
- Bit[7]: XOR start/stop. Setting '1' to this bit will enable XOR operation of the controller. Writing '0' to this bit will halt XOR operation. All state machine information is lost when a '0' is written. XOR operation cannot be stopped and then resumed. If this bit is reset while XOR operation is still active, the XOR command is aborted. This bit is reset after the XOR command is completed.
- Bit[6]: XOR Type.

'1' = execute XOR command.

'0' = execute Compare Command.

Bit[5:4]: Reserved.

Bit[3:0]: assign current XOR Interrupt Sequence ID.

ATA Timing & Control Register

Data Register:

Channel #0: index_IDE0: 00h | BA#3 + 200h

Channel #1: index_IDE1: 00h | BA#3 + 280h

Channel #2: index_IDE2: 00h | BA#3 + 300h

Channel #3: index_IDE3: 00h | BA#3 + 380h

31:16 (r)	15:0(r/w)
Reserved(0)	Data Register

The register contains the same information as the Data register defined in ATA specification.

Feature/Error Register:

Channel #0: index_IDE0: 04h | BA#3 + 204h

Channel #1: index_IDE1: 04h | BA#3 + 284h

Channel #2: index_IDE2: 04h | BA#3 + 304h

Channel #3: index_IDE3: 04h | BA#3 + 384h

31:8 (r)	7:0 (r/w)
Reserved(0)	Feature or Error Register

The register contains the same information as the Feature-Status register defined in ATA specification.

Sector Count Register:

Channel #0: index_IDE0: 08h | BA#3 + 208h

Channel #1: index_IDE1: 08h | BA#3 + 288h

Channel #2: index_IDE2: 08h | BA#3 + 308h

Channel #3: index_IDE3: 08h | BA#3 + 388h

31:8 (r)	7:0 (r/w)
Reserved(0)	Sector Count Register

The register contains the same information as the Sector-Count register defined in ATA specification.

Sector Number Register:

Channel #0: index_IDE0: 0Ch | BA#3 + 20Ch

Channel #1: index_IDE1: 0Ch | BA#3 + 28Ch

Channel #2: index_IDE2: 0Ch | BA#3 + 30Ch

Channel #3: index_IDE3: 0Ch | BA#3 + 38Ch

31:8 (r)	7:0 (r/w)
Reserved(0)	Sector Number Register

The register contains the same information as the Sector-Number register defined in ATA specification.

Cylinder Low Register:

Channel #0: index_IDE0: 10h | BA#3 + 210h

Channel #1: index_IDE1: 10h | BA#3 + 290h

Channel #2: index_IDE2: 10h | BA#3 + 310h

Channel #3: index_IDE3: 10h | BA#3 + 390h

31:8 (r)	7:0 (r/w)
Reserve(0)	Cylinder Low Register

The register contains the same information as the Cylinder-Low register defined in ATA specification.

Channel #0 Cylinder High Register:

Channel #0: index_IDE0: 14h | BA#3 + 214h

Channel #1: index_IDE1: 14h | BA#3 + 294h

Channel #2: index_IDE2: 14h | BA#3 + 314h

Channel #3: index_IDE3: 14h | BA#3 + 394h

31:8 (r)	7:0 (r/w)
Reserved(0)	Cylinder High Register

The register contains the same information as the Cylinder-High register defined in ATA specification.

Device / Head Register:

Channel #0: index_IDE0: 18h | BA#3 + 218h

Channel #1: index_IDE1: 18h | BA#3 + 298h

Channel #2: index_IDE2: 18h | BA#3 + 318h

Channel #3: index_IDE3: 18h | BA#3 + 398h

31:8 (r)	7:0 (r/w)
Reserved(0)	Device/Head Register

The register contains the same information as the Device-Head register defined in ATA specification.

Command/Status Register:

Channel #0: index_IDE0: 1Ch | BA#3 + 21Ch

Channel #1: index_IDE1: 1Ch | BA#3 + 29Ch

Channel #2: index_IDE2: 1Ch | BA#3 + 31Ch

Channel #3: index_IDE3: 1Ch | BA#3 + 39Ch

31:8 (r)	7:0 (r/w)
Reserved (0)	Command or Status Register

The register contains the same information as the Command-Status register defined in ATA specification.

Alternate Status / Device Control Register:

Channel #0: index_IDE0: 38h | BA#3 + 238h

Channel #1: index_IDE1: 38h | BA#3 + 2B8h

Channel #2: index_IDE2: 38h | BA#3 + 338h

Channel #3: index_IDE3: 38h | BA#3 + 3B8h

31:8 (r)	7:0 (r/w)
Reserved (0)	Alternate Status or Device Control Register

The register contains the same information as the Alternate-Status or Device-Control register defined in ATA specification.

IDE Command Packet Pointer Register:

Channel #0: BA#0: 0h | index_IDE0: 40h | BA#3 + 240h

Channel #1: BA#0: 10h | index_IDE1: 40h | BA#3 + 2C0h

Channel #2: BA#0: 20h | index_IDE2: 40h | BA#3 + 340h

Channel #3: BA#0: 30h | index_IDE3: 40h | BA#3 + 3C0h

31:2 (r/w)	1:0 (r/w)
Base address of Command Packet	Reserved(00)

Bit[31:2]: The ATA Command Packet Pointer must be DWORD aligned. This register points the location of ATA command-packet.

Bit[1:0]: Reserved.

Descriptor Table Pointer Register:

Channel #0: index_IDE0: 44h | BA#3 + 244h

Channel #1: index_IDE1: 44h | BA#3 + 2C4h

Channel #2: index_IDE2: 44h | BA#3 + 344h

Channel #3: index_IDE3: 44h | BA#3 + 3C4h

31:2 (r/w)	1:0 (r)
Base address of Descriptor table. Corresponds to A[31:5]	Reserved(00)

The Descriptor Table must be DWORD aligned. This register points the location of S/G table. For packet-command operation, the value will be updated by PSG pointer of ATA command-packet.

Global Control & Status Register:

Channel #0: BA#0: 4h | index_IDE0: 48h | BA#3 + 248h

Channel #1: BA#0: 14h | index_IDE1: 48h | BA#3 + 2C8h

Channel #2: BA#0: 24h | index_IDE2: 48h | BA#3 + 348h

Channel #3: BA#0: 34h | index_IDE3: 48h | BA#3 + 3C8h

7 (r)	6 (r/w)	5 (r/w)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	NCA Pause

15	14	13	12	11	10(r)	9(r)	8 (r)
Reserved	Reserved	Reserved	Reserved	Reserved	DH_ERR	SH_ERR	PH_ERR

23(r)	22(r)	21(r)	20(r)	19 (r)	18	17	16
reserved	PCI System Error	Drive Error	Under Run Error	Over Run Error	Reserved	Direct Command Complete	Packet Command Complete

31 (r)	30 (r)	29 (r)	28 (r)	27 (r)	26 (r)	25 (r)	24 (r)
Reserved	Reserved	Packet Command Cycle	Delay Transaction	Reserved			

Bit[31:30]: Reserved.

Bit[29]: Packet Command Cycle.

Bit[28]: Delay Transaction Status. This command packet is executed on delay transaction.

Bit[27:23]: Reserved.

Bit[22]: PCI System Error. Master abort or target abort protocol is happened. This bit will be reset by

- write “1” to ATA software reset(index_IDE0/1/2/3: 60h BA#3 + 260h/2C0h/360h/3C0h, bit 11).
- Bit[21]: Drive Error. Shadow register of HD’s error flag. This bit will be reset by write “1” to ATA software reset(index_IDE0/1/2/3: 60h BA#3 + 260h/2C0h/360h/3C0h, bit 11).
- Bit[20]: Underrun Error. S/G total byte count is less than HD requires. The check pint is when HD’s INTRQ asserts and only error in DMA read operation could be detected. This bit will be reset by write “1” to ATA software reset(index_IDE0/1/2/3: 60h BA#3 + 260h/2C0h/360h/3C0h, bit 11).
- Bit[19]: Overrun Error. S/G total byte count is large than HD requires. The checkpoint is when HD’s INTRQ asserts. This bit will be reset by write “1” to ATA software reset(index_IDE0/1/2/3: 60h BA#3 + 260h/2C0h/360h/3C0h, bit 11).
- Bit[18]: Reserved.
- Bit[17]: direct command complete status
- Bit[16]: packet command complete status.
- Bit[15:11]: Reserved.
- Bit[10]: DH_ERROR. “1” Indicates the PCI SYSTEM ERROR occurs while loading DATA. This bit will be reset by write “1” to ATA software reset(index_IDE0/1/2/3: 60h BA#3 + 260h/2C0h/360h/3C0h, bit 11).
- Bit[9]: SH_ERROR. “1” Indicates the PCI SYSTEM ERROR occurs while loading a S/G table. This bit will be reset by write “1” to ATA software reset (index_IDE0/1/2/3: 60h BA#3 + 260h/2C0h/360h/3C0h, bit 11)..
- Bit[8]: PH_ERROR. “1” Indicates the PCI SYSTEM ERROR occurs while loading a packet command. This bit will be reset by write “1” to ATA software reset(index_IDE0/1/2/3: 60h BA#3 + 260h/2C0h/360h/3C0h, bit 11).
- Bit[7:1]: Reserved.
- Bit[0]: NCA Pause. When this bit is set, the ATA engine will not execute the next command packet.

Configuration and Timing Control Register 0:

DRV #0: index_IDE0: 4Ch | BA#3 + 24Ch

DRV #1: index_IDE1: 4Ch | BA#3 + 2CCh

DRV #2: index_IDE2: 4Ch | BA#3 + 34Ch

DRV #3: index_IDE3: 4Ch | BA#3 + 3CCh

31 (r/w)	30:29 (r/w)	28:24 (r/w)	23:21 (r/w)	20:16 (r/w)	15:14 (r/w)	13:8 (r/w)	7:5 (r/w)	4:0 (r/w)
Reserve	TDN (2h)	TDCYCH (1fh)	TDENV (6h)	TDCYCL (1fh)	Reserve	TPRCYC (2bh)	TPRCV (7h)	TPENV (1bh)

Bit 31: reserved.

- Bit[30:29]: tDN. CS0_, CS1_ hold time in DMA mode. It is the number of clock from DIOR_/DIOW_ to CS0_, CS1_.
- Bit[28:24]: tDCYCH: cycle number of high pulse of DIOR_/DIOW_ in DMA mode. It is the pulse width when DIOR_/DIOW_ is high in DMA transformation.
- Bit[23:21]: tDENV. Cycle time of DMA envelope. It is the number of clock from DACK_ to DIOR_/DIOW_.
- Bit[20:16]: tDCYCL: cycle time of low pulse of DIOR_/DIOW_ in DMA mode. It is the pulse width when DIOR_/DIOW_ is low in DMA transformation.
- Bit[13:8]: tPRCYC. Cycle time of DIOR_/DIOW_. It is the pulse width of DIOR_/DIOW_ in PIO register (8bit) transformation.
- Bit[7:5]: tPRCV. PIO recovery time. It is the number of clock between two PIO transformations.
- Bit[4:0]: tPENV. PIO envelope. It is the number of clock to initialize PIO transformation

Configuration and Timing Control Register 1:

DRV #0: index_IDE0: 50h | BA#3 + 250h

DRV #1: index_IDE1: 50h | BA#3 + 2D0h

DRV #2: index_IDE2: 50h | BA#3 + 350h

DRV #3: index_IDE3: 50h | BA#3 + 3D0h

15:14 (r/w)	13 (r/w)	12:8 (r/w)	7:4 (r/w)	3:2 (r/w)	1:0 (r/w)
Reserve	tHOLD (1b)	Tcyc (fh)	TMLI (bh)	TENV (2h)	TACK (2h)

31:26 (r/w)	25 (r/w)	24 (r/w)	23:21 (r/w)	20:16 (r/w)
TPDCYC (2bh)	Reserved	PIO mode IORDY enable (1b)	TSS (6h)	TRP (15h)

Bit[31:26]: tPRCYC. Cycle time of DIOR_/DIOW_. It is the pulse width of DIOR_/DIOW_ in PIO data (16bit) transformation.

Bit[25]: Reserved.

Bit[24]: PIO mode IORDY enable.

‘1’: the PIO mode transformation will be finished after IORDY being high.

‘0’: the PIO mode transformation will be finished regardless status of IORDY.

Bit[23:21]: TSS. Timing from last STROBE edge to STOP

Bit[20:16]: ready-to-pause time.

Bit[15:14]: reserved.

Bit[13]: tHOLD. ‘1’ : add half clock for DATA hold time.

Bit[12:8]: tCYC. Cycle time of UDMA.

Bit[7:4]: tMLI. Inter-lock time with minimum.

Bit[3:2]: tENV. Envelope time.

Bit[1:0] : tACK. Setup and hold time from DACK_ in UDMA mode.

S/G Engine Address counter Register:

Channel #0: index_IDE0: 54h | BA#3 + 254h

Channel #1: index_IDE1: 54h | BA#3 + 2D4h

Channel #2: index_IDE2: 54h | BA#3 + 354h

Channel #3: index_IDE3: 54h | BA#3 + 3D4h

31:0 (r)
Value of S/G engine address counter

Bit[31:0]: The value of S/G engine address counter. When test mode is set, the counter is cut to four 8bit counter and its value can be read from this register.

S/G Engine byte count counter Register :

Channel #0 : index_IDE0: 58h | BA#3 + 258h

Channel #1 : index_IDE1: 58h | BA#3 + 2D8h

Channel #2 : index_IDE2: 58h | BA#3 + 358h

Channel #3 : index_IDE3: 58h | BA#3 + 3D8h

31:16 (r)	15:0 (r)
Reserved	Value of S/G engine byte count counter 0

Bit[31:16]: Reserved.

Bit[15:0] : The value of S/G engine byte count counter 0. When test mode is set, the counter is broken to two 8bit counter and its value can be read from this register.

ATA Next Command Packet Pointer Register:

Channel #0: index_IDE0: 5Ch | BA#3 + 25Ch

Channel #1: index_IDE1: 5Ch | BA#3 + 2DCh

Channel #2: index_IDE2: 5Ch | BA#3 + 35Ch

Channel #3: index_IDE3: 5Ch | BA#3 + 3DCh

31:6 (r/w)	1:0 (r/w)
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Base address of Next Command Packet	Reserved(00)
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Bit[31:2]: The ATA Next Command Packet Pointer must be DWORD aligned. The register indicates the location of next command packet.

Bit[1:0]: Reserved.

IDE Control & Status Register:

Channel #0: index_IDE0: 60h | BA#3 + 260h

Channel #1: index_IDE1: 60h | BA#3 + 2E0h

Channel #2: index_IDE2: 60h | BA#3 + 360h

Channel #3: index_IDE3: 60h | BA#3 + 3E0h

7 (r/w)	6 (r/w)	5 (r)	4 (r/w)	3 (r/w)	2 (r/w)	1 (r/w)	0 (r/w)
DMA Start/Stop	DMA R/W Direction	Reserved.		Interrupt Sequence ID			

15:14(r/w)	13 (r/w)	12 (r/w)	11(r/w)	10 (r/w)	9(r/w)	8(r/w)
Reserved	reserved	reserved	ATA Software Reset (0)	Mask INT (0)	Test Mode (0)	reserved

23	22	21	20	19	18	17	16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

31 (r)	30 (r)	29 (r)	28 (r)	27(r)	26	25(r)	24(r)
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Data FIFO Empty	Control FIFO Empty	Reserved	Drive DMARQ Status	Drive INT Status	Reserved	reserved
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Bit[31]: Data FIFO empty. The data FIFO of channel 0/1/2/3 is empty

Bit[30]: Control FIFO empty. The Control FIFO of channel 0/1/2/3 is empty

Bit[29]: Reserved.

Bit[28]: Drive DMARQ status. The status of internal DMARQ can be monitored directly from here.

Bit[27]: Drive INT status. The status of internal ATA's INTRQ.

Bit[26:12]: reserved

Bit[11]: This bit controls the ATA module software reset. Write '1' to this will reset ATA module.

Bit[10]: Mask INT. When this bit is set, the interrupt from ATA module will not pass to PCI.

Bit[9]: ATA Module Test mode.

Bit[8]: reserved

Bit[7]: DMA start/stop. Setting '1' to this bit will enable DMA operation of the controller. Writing '0' to this bit will halt DMA operation. All state machine information is lost when a '0' is written. DMA operation cannot be stopped and then resumed. If this bit is reset while DMA operation is still active, the DMA command is aborted. This bit is reset after the DMA command is completed.

Bit[6]: Host set the Direction of DMA data. 1: chip to HD. 0: HD to chip

Bit[5:4]: Reserved.

Bit[3:0]: Interrupt Sequence ID. It indicates the sequence ID of the interrupt generated by this engine.

SATA status Register:

Channel #0: index_IDE0: 80h | BA#3 + 400h

Channel #1: index_IDE1: 80h | BA#3 + 500h

Channel #2: index_IDE2: 80h | BA#3 + 600h

Channel #3: index_IDE3: 80h | BA#3 + 700h

31:12	11:8	7:4	3:0
Reserved	IPM	SPD	DET

Bit[31:12]: reserved.

Bit[11:8]: The current interface power management state.

0000: Device not present or communication not established.

0001: Interface in active state.

0010: Interface in PARTIAL power management state.

0110: Interface in SLUMBER power management state.

All other values are reserved.

Bit[7:4] : The negotiated interface communication speed established.

0: No negotiated speed. The device is not present or communication is not established.

1: Interface is in active state.

All other values are reserved.

Bit[3:0] : The interface device detection and PHY state.

0000: No device detected and PHY communication is not established.

0001: Device presence detected but PHY communication is not established.

0011: Device presence detected and PHY communication is established.

0100: PHY in offline mode.

All other values are reserved.

SATA Error Register:

Channel #0: index_IDE0: 84h | BA#3 + 404h

Channel #1: index_IDE1: 84h | BA#3 + 504h

Channel #2: index_IDE2: 84h | BA#3 + 604h

Channel #3: index_IDE3: 84h | BA#3 + 704h

7:2	1	0
Reserved	COMM_ERR_FIXED	DATA_ERROR_FIXED

11	10	9	8
Reserved	PROTOCOL_ERR	PRESISTENT_ERR	DATA_ERR

23	22	21	20	19	18	17:16
LINK_SEQ_ERR	reserved	CRC_ERR	DISPARITY_ERR	10B_TO_8B ERR	COMWAKE	reserved

31:26	25	24
reserved	FIS_TYP	reserved

The register can be accessed by DW command only.

Bit[31:26] : reserved.

Bit 25: FIS type not recognized.

0: FIS type recognized.

1: Transport layer with a good CRC received one or more FIS since this not was last cleared,
but had a type field that was not recognized.

Bit 24: reserved.

- Bit 23: Link sequence error. The Link layer state machine defines the conditions under which the link layer detects and erroneous transition.
- 0: No link sequence error.
 - 1: One or more Link state machine error conditions was encountered since the last time this bit was cleared.
- Bit 22: reserved.
- Bit 21: CRC error.
- 0: No CRC error.
 - 1: One or more CRC errors occurred with the Link layer since this bit was last cleared.
- Bit 20: Disparity error.
- 0: No disparity error.
 - 1: One or more disparity errors were detected since this bit was last cleared.
- Bit 19: 10B-to-8B decoding error.
- 0: No 10B-to-8B decoding error.
 - 1: One or more 10B-to-8B decoding error since this bit was last cleared.
- Bit 18: COMWAKE.
- 0: No COMWAKE.
 - 1: COMWAKE signal was detected by the PHY since this bit was last cleared.
- Bit[17:11]: reserved.
- Bit 10: Protocol error. The host software should reset the interface and retry the corresponding operation. If such an error persists, the attached device might have a design issue, rendering it incompatible with the host bus adapter.
- 0: No protocol error.
 - 1: A violation of the SATA procool was detected. This can arise from an invalid or poorly-formed FIS, from an invalid state transition, or from other causes.
- Bit 9: Non-recoverable persistent communication or data-integrity error. Persistent communication errors can arise from a faulty interconnect with the device, from a device that has been removed or has failed, or many other causes.
- 0: No error.
 - 1: A communication error that was not recovered occurred and is expected to be persistent. Therefore it is not necessary to retry the operation.
- Bit 8: Non-recoverable transient data integrity error.
- 0: No error.
 - 1: A data integrity error occurred that was not recovered by the interface. The host software should retry the operation.
- Bit [7:2] : reserved.
- Bit1: Communication error recovered. Communications between the host and the device can be temporarily lost by a device that was temporarily removed, from a temporary loss of PHY synchronization, or from other causes. It could be derived from the PHYRDY signal between the PHY and Link layers. No

action is required by the host software. However, the host software could elect to track such recovered errors in order to gauge overall communications integrity.

Bit0: Data integrity error recovered. A data integrity error can arise from a noise burst in the transmission, a voltage supply variation, or from other causes. No action is required by the host software. However, the host software could not elect to track such recovered errors in order to gauge overall communications integrity.

0: No error recovered.

1: A data integrity error was recovered by the interface through a retry operation or other recovery action.

SATA Scontrol Register:

Channel #0: index_IDE0: 88h | BA#3 + 408h

Channel #1: index_IDE1: 88h | BA#3 + 508h

Channel #2: index_IDE2: 88h | BA#3 + 608h

Channel #3: index_IDE3: 88h | BA#3 + 708h

7:4	3:0
SPD (0000h)	DET (0000h)

15:12	11:8
Reserved	IPM (0000h)

23:16
reserved

31:24
reserved

The register can be accessed by DW command only.

Bit[31:12] :reserved.

Bit [11:8]: The states of the enabled interface power management that can be invoked via the Serial ATA interface power management capabilities.

0000: No interface power management state restrictions.

0001: Transitions to the PARTIAL power management state disabled.

0010: Transitions to the SLUMBER power management state disabled.

0011: Transitions to both the PARTIAL and SLUMBER power management states disabled.

All other values are reserved.

Bit[7:4]: The highest communication speed the interface is allowed to negotiated when the interface communication speed is established.

0: No speed negotiation restrictions.

1: Limit speed negotiation to a rate not greater than Generation 1 communication rate.

All other values are reserved.

Bit[3:0]: Host adapter device detection and interface initialization controller.

0000: No device detection or initialization action requested.

0001: Perform interface communication initialization sequence to establish communications. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized.

0100: Disable the Serial ATA interface and put PHY in offline mode.

All other values are reserved.

SATA control Register:

Channel #0: index_IDE0: 8Ch | BA#3 + 40Ch

Channel #1: index_IDE1: 8Ch | BA#3 + 50Ch

Channel #2: index_IDE2: 8Ch | BA#3 + 60Ch

Channel #3: index_IDE3: 8Ch | BA#3 + 70Ch

31:24	23	22:2	1:0(r/w)
Reserved	SSC_EN (0)	reserved	SQ (00b)

Bit [31:24] : reserved.

Bit23: SATA Spread Spectrum Clocking enable. 1: Enable. 0: Disable.

Bit [22:2]: reserved.

Bit[1:0] Squelch detector threshold. 00: 100mVdiff p-p. 01: 150mVdiff p-p. 10: 200mVdiff p-p. 11: reserved. **01b is suggested.**

SATA BIST Activate FIS DW0 Register:

Channel #0: index_IDE0: 90h | BA#3 + 410h

Channel #1: index_IDE1: 90h | BA#3 + 510h

Channel #2: index_IDE2: 90h | BA#3 + 610h

Channel #3: index_IDE3: 90h | BA#3 + 710h

31:24	23(r /w)	22(r /w)	21(r /w)	20(r /w)	19(r /w)	18(r /w)	17	16(r /w)	15:0
Reserved	T	A	S	L	F	P	reserved	V	reserved

Bit[31:24] reserved

Bit[23] T: Transmit only

Bit[22] A: ALIGN Bypass

Bit[21] S: Scrambling Bypass

Bit[20] L: Far-end Retimed Loopback

Bit[19] F: Far-end Analog Loopback

Bit[18] P: Primitive Bits

Bit[17] reserved

Bit[16] V: Vendor Unique

Bit[15:0] reserved

SATA BIST Activate FIS DW1 Register:

Channel #0: index_IDE0: 94h | BA#3 + 414h

Channel #1: index_IDE1: 94h | BA#3 + 514h

Channel #2: index_IDE2: 94h | BA#3 + 614h

Channel #3: index_IDE3: 94h | BA#3 + 714h

31:0
DW1 content of the BIST Activate FIS

SATA BIST Activate FIS DW2 Register:

Channel #0: index_IDE0: 98h | BA#3 + 418h

Channel #1: index_IDE1: 98h | BA#3 + 518h

Channel #2: index_IDE2: 98h | BA#3 + 618h

Channel #3: index_IDE3: 98h | BA#3 + 718h

31:0
DW2 content of the BIST Activate FIS

Example of far-end retimed loopback,

write 410 00100000

write 414 b5b5b5b5

write 418 b5b5b5b5

write 43c 00200000

after some time

read 43c and get 00340000 or 00350000 meaning good results.

TBG mode register (index_IDE0:9Ch | BA#3 + 41Ch)

7:0
PROG_N (49h)

15	14	13:8
HIKVCOA	PROG_EN (0)	PROG_M (03h)

23:19	18	17:16
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Reserved	NPA	CNFG (10h)
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31:24
reserved

The register can be accessed by DW command only.

Bit [31:19]: reserved.

Bit 18: NPA Set VCO speed. 0: Full rate. 1: Half rate.

Bit [17:16] : TBG clock frequency selection.

00: 100Mhz.

01: 133Mhz.

10: 150Mhz.

11: RSVD.

Bit 15: HIKVCOA. Set VCO frequency range. 0: Slow corner. 1: Fast corner.

Bit 14: TBG clock programmability via PROG_M and PROG_N registers enabled.

0: Disabled.

1: Enabled PROG_M and PROG_N, and disable CNFG registers. When enabled, TBG clock frequency is then calculated as $10\text{Mhz} * (\text{PROG_N} + 2) / (\text{PROG_M} + 2)$.

Bit[13:8] : TBG M parameter.

Bit[7:0] : TBG N parameter.

TBG clock frequency is then calculated as

$10\text{Mhz} * (\text{PROG_N} + 2) / (\text{PROG_M} + 2)$.

Power mode trigger register

index_IDE0: B0h|BA#3 + 430h

index_IDE1: B0h|BA#3 + 530h

index_IDE2: B0h|BA#3 + 630h

index_IDE3: B0h|BA#3 + 730h

31:30	29(r/w))	28(r/w)	27(r/w)	26(r/w)	25:20	19(r/w)	18(r/w)	17(r/w)	16(r/w)
Reserved	CONT	T_SCR B	R_SCR B	SCRC_ENB (0)	reserved	PMEN B (0)	R_ERR_EN B	UDMA_SEL	DRQ_NG

The register can be accessed by DW command only.

- Bit [31:30] : reserved
- Bit [29] : Transmitting CONT primitive. 0: Enable. 1: Disable.
- Bit [28] : Transmitter Scrambler. 0: On. 1: Off.
- Bit [27] : Receiver Scrambler. 0: On. 1: Off.
- Bit[26] Serial CRC check. 0: Enable. 1: Disable.
- Bit [25:20] : reserved
- Bit 19: Power Mode Trigger. 0: Enable.
1: Disable.

When enabled, standard IDLE IMMEDIATE and STANDBY IMMEDIATE commands will be converted into Serial ATA power down handshaking sequence, PMREQ and PMACK, and trigger Partial and Slumber modes respectively.

- Bit[18]: Response to bad CRC. 0: R_ERR. 1: R_OK
- Bit[17]: UDMA mode selection.
1: Fix UDMA speed at CNFG clock rate.
0: Track UDMA mode to Set Features command setting.
- Bit[16]: Command register written when DRQ is set.
0: Previous command is not aborted.
1: Previous command is aborted.
- Bit[15:13]: reserved.
- Bit[12:8]: When FIFO space becomes less than this value, HOLD primitives will be sent.
- Bit[7:0]: reserved.

Power mode register

index_IDE0: BChl BA#3 + 43Ch

index_IDE1: BChl BA#3 + 53Ch

index_IDE2: BChl BA#3 + 63Ch

index_IDE3: BChl BA#3 + 73Ch

31:22	21(r/w)	20(r/w)	19	18:16(r)	15:14(r/w)	13:8	7:0
reserved	BIST_START	BIST_RECV	Rvd	BIST_OK	PM (00)	reserved	reserved

The register can be accessed by DW command only.

- Bit[31:22] reserved
- Bit[21] 0: BIST Idle. 1: BIST Start.

Bit[20]	0: BIST Activate FIS is not received. 1: BIST Activate FIS is received.
Bit[19]	reserved
Bit[18:16]	10x: BIST result is OK. All others: BIST result is bad
Bit[15:14]	Power Mode control. When reading these bits, current power state is read. 10: Partial mode. X1: Slumber mode. Writing '1' to one of the bits will trigger power down handshaking sequence and make PHY into Partial or Slumber state.
Bit[13:0]	reserved

Slew rate control register (index_IDE0:F0h | BA#3 + 470h)

31:20	19:16(r/w)	15:12(r/w)	11:9	8:6	5:3	2:0
reserved	PCIZP (8h)	PCIZN (8h)	reserved	reserved	reserved	reserved

The register can be accessed by DW command only.

Bit[31:20]: reserved

Bit[19:16]: Set PCI I/O's rising slew rate, from the slowest (0) to the fastest (15).

Bit[15:12]: Set PCI I/O's falling slew rate, from the slowest (0) to the fastest (15).

Bit[11:0]: reserved..

SATA mode Register :

Channel #0 : index_IDE0:F4h | BA#3 + 474h

Channel #1 : index_IDE1:F4h | BA#3 + 574h

Channel #2 : index_IDE2:F4h | BA#3 + 674h

Channel #3 : index_IDE3:F4h | BA#3 + 774h

31(r/w)	30:27	26:25(r/w)	24:23(r/w)	22:13	12:11(r/w)	10:9(r/w)	8	7:5(r/w)	4:0
FORCE	Reserved	SEL_MUPF (10b)	SEL_MUF F (11b)	rwd	PRE (01)	PLL BW (00)	reserve d	AMP (100h)	reserved

Bit[31]: Force Phy to move to ready state.

bit[30:27]: reserved.

Bit[26:25] select phase counter

Bit[24:23] Select frequency multiplier.

Bit[22:13] reserved

Bit[12:11]: PRE, Transmitter Pre-emphasis.

00: Coefficient=0.0.

01: Coefficient=0.1.

10: Coefficient=0.2.

11: Coefficient=0.3.

Bit[10:9]: PLL Bandwidth. Adjusts PLL bandwidth.
00: BW=1.
01: BW=0.667.
10: BW=0.667.
11: BW=0.5.
adjust these bit if the clock source is not good enough.

Bit[8] reserved

Bit [7:5]: AMP; Signal Amplitude.
000: 10mA+0%.
001: +5%.
010: +10%.
011: +15%.
100: +20%.
101: +25%.
110: +30%.
111: +35%.

Bit [4:0]: reserved

List of extended registers

BA#0 : PCI configuration base address register 0

BA#1: PCI configuration base address register 1

BA#2: PCI configuration base address register 2

BA#3: PCI configuration base address register 3

1. ATA Control Register (BA#0)

Command Packet Control Register (BA#0/ BA #3)

	Byte3	Byte2	Byte1	Byte0
00h/240h/index_IDE0: 40h	Channel #0 Command Packet Pointer Register:			
04h/248h/index_IDE0: 48h	Channel #0 Control & Status register			
08h	Reserved			Index_IDE0
0Ch	IDE#0 Data Port			
10h/2C0h/index_IDE1:40h	Channel #1 Command Packet Pointer Register:			
14h/2C8h/index_IDE1:48	Channel #1 Control & Status register			
18h	Reserved			Index_IDE1
1Ch	IDE#1 Data Port			
20h/340h/index_IDE2:40h	Channel #2 Command Packet Pointer Register:			
24h/348h/index_IDE2: 48h	Channel #2 Control & Status register			

28h	Reserved	Index_IDE2
2Ch/	IDE#2 Data Port	
30h/3C0h/index_IDE3: 40h	Channel #3 Command Packet Pointer Register:	
34h/3C8h/index_IDE3: 48h	Channel #3 Control & Status register	
38h	Reserved	Index_IDE3
3Ch	IDE#3 Data Port	

IDE Channel 0 Timing & Control Register (Index_IDE0/ BA#3)

offset	
0h/ 200h	Channel #0 Data Register
4h/ 204h	Channel #0 Feature/Error Register
8h/208h	Channel #0 Sector Count Register
Ch/ 20Ch	Channel #0 Sector Number Register
10h/ 210h	Channel #0 Cylinder Low Register
14h/ 214h	Channel #0 Cylinder High Register
18h/ 218h	Channel #0 Device / Head Register
1Ch/ 21Ch	Channel #0 Command/Status Register
38h/ 238h	Channel #0 Alternate Status / Device
40h/ 240h	Channel #0 IDE Command Packet Pointer Register
44h/ 244h	Channel #0 Descriptor Table Pointer Register

48h/248h	Channel #0 Global Control & Status Register:
4Ch/ 24Ch	DRV #0 Configuration and Timing Control Register 0
50h/ 250h	DRV #0 Configuration and Timing Control Register 1
54h/ 254h	Channel #0 S/G Engine Address counter Register
58h/ 258h	Channel #0 S/G Engine byte count counter Register
5Ch/ 25Ch	Channel #0 ATA Next Command Packet Pointer Register
60h/ 260h	Channel #0 IDE Control & Status Register
80h/400h	SATA #0 status register
84h/404h	SATA #0 error register
88h/408h	SATA #0 Scontrol register
8Ch/40Ch	SATA #0 control register
90h/410h	SATA #0 BIST Activate FIS DW0
94h/414h	SATA #0 BIST Activate FIS DW1
98h/418h	SATA #0 BIST Activate FIS DW2
9Ch/41Ch	TBG mode register
B0h/430h	SATA #0 Power mode trigger register
BCh/43Ch	SATA #0 Power mode register
F0h/470h	Slew rate control register
F4h/474h	SATA #0 mode register

IDE Channel 1 Timing & Control Register (Index_IDE1/ BA#3)

offset	
0h/ 280h	Channel #1 Data Register
4h/ 284h	Channel #1 Feature/Error Register
8h/288h	Channel #1 Sector Count Register
Ch/ 28Ch	Channel #1 Sector Number Register
10h/ 290h	Channel #1 Cylinder Low Register
14h/ 294h	Channel #1 Cylinder High Register
18h/ 298h	Channel #1 Device / Head Register
1Ch/ 29Ch	Channel #1 Command/Status Register
38h/ 2B8h	Channel #1 Alternate Status / Device
40h/ 2C0h	Channel #1 IDE Command Packet Pointer Register
44h/ 2C4h	Channel #1 Descriptor Table Pointer Register
48h/ 2C8h	Channel #1 Global Control & Status Register:
4Ch/ 2CCh	DRV #1 Configuration and Timing Control Register 0
50h/ 2D0h	DRV #1 Configuration and Timing Control Register 1
54h/ 2D4h	Channel #1 S/G Engine Address counter Register
58h/ 2D8h	Channel #1 S/G Engine byte count counter Register
5Ch/ 2DCh	Channel #1 ATA Next Command Packet Pointer Register

60h/ 2E0h	Channel #1 IDE Control & Status Register
80h/500h	SATA #1 status register
84h/504h	SATA #1 error register
88h/508h	SATA #1 Scontrol register
8Ch/50Ch	SATA #1control register
90h/510h	SATA #1BIST Activate FIS DW0
94h/514h	SATA #1 BIST Activate FIS DW1
98h/518h	SATA #1 BIST Activate FIS DW2
B0h/530h	SATA #1 Power mode trigger register
BCh/53Ch	SATA #1 Power mode register
F4h/574h	SATA #1 mode register

IDE Channel 2 Timing & Control Register (Index_IDE2/ BA#3)

Offset	
0h/ 300h	Channel #2 Data Register
4h/ 304h	Channel #2 Feature/Error Register
8h/ 308h	Channel #2 Sector Count Register
Ch/ 30Ch	Channel #2 Sector Number Register
10h/ 310h	Channel #2 Cylinder Low Register
14h/ 314h	Channel #2 Cylinder High Register

18h/ 318h	Channel #2 Device / Head Register
1Ch/ 31Ch	Channel #2 Command/Status Register
38h/ 338h	Channel #2 Alternate Status / Device
40h/ 340h	Channel #2 IDE Command Packet Pointer Register
44h/ 344h	Channel #2 Descriptor Table Pointer Register
48h/ 348h	Channel #2 Global Control & Status Register:
4Ch/ 34Ch	DRV #2 Configuration and Timing Control Register 0
50h/ 350h	DRV #2 Configuration and Timing Control Register 1
54h/ 354h	Channel #2 S/G Engine Address counter Register
58h/ 358h	Channel #2 S/G Engine byte count counter Register
5Ch/ 35Ch	Channel #2 ATA Next Command Packet Pointer Register
60h/ 360h	Channel #2 IDE Control & Status Register
80h/600h	SATA #2 status register
84h/604h	SATA #2 error register
88h/608h	SATA #2 Scontrol register
8Ch/60Ch	SATA #2control register
90h/610h	SATA #2 BIST Activate FIS DW0
94h/614h	SATA #2 BIST Activate FIS DW1
98h/618h	SATA #2 BIST Activate FIS DW2

B0h/630h	SATA #2 Power mode trigger register
BCh/63Ch	SATA #2 Power mode register
F4h/674h	SATA #2 mode register

IDE Channel 3 Timing & Control Register (Index_IDE3/ BA#3)

offset	
0h/ 380h	Channe3 #2 Data Register
4h/ 384h	Channel #3 Feature/Error Register
8h/ 388h	Channel #3 Sector Count Register
Ch/ 38Ch	Channel #3 Sector Number Register
10h/ 390h	Channel #3 Cylinder Low Register
14h/ 394h	Channel #3 Cylinder High Register
18h/ 398h	Channel #3 Device / Head Register
1Ch/ 39Ch	Channel #3 Command/Status Register
38h/ 3B8h	Channel #3 Alternate Status / Device
40h/ 3C0h	Channel #3 IDE Command Packet Pointer Register
44h/ 3C4h	Channel #3 Descriptor Table Pointer Register
48h/ 3C8h	Channel #3 Global Control & Status Register:
4Ch/ 3CCh	DRV #3 Configuration and Timing Control Register 0
50h/ 3D0h	DRV #3 Configuration and Timing Control Register 1

54h/ 3D4h	Channel #3 S/G Engine Address counter Register
58h/ 3D8h	Channel #3 S/G Engine byte count counter Register
5Ch/ 3DCh	Channel #3 ATA Next Command Packet Pointer Register
60h/ 3E0h	Channel #3 IDE Control & Status Register
80h/700h	SATA #3 status register
84h/704h	SATA #3 error register
88h/708h	SATA #3 Scontrol register
8Ch/70Ch	SATA #3control register
90h/710h	SATA #3 BIST Activate FIS DW0
94h/714h	SATA #3 BIST Activate FIS DW1
98h/718h	SATA #3 BIST Activate FIS DW2
B0h/730h	SATA #3 Power mode trigger register
BCh/73Ch	SATA #3 Power mode register
F4h/774h	SATA #3 mode register

2. XOR Control Register

XOR command package control register (BA#1/index_XOR/BA#3)

Offset	Byte3	Byte2	Byte1	Byte0
0h/0h/180h	XOR Command Packet Pointer Register			

4h/4h/184h	XOR Global Control & Status Register	
8h/x/x	Reserved	Index_XOR
Ch/x/x	XOR Data Port	

XOR register(index_XOR/ BA#3)

Offset	
8h/ 188h	XOR Descriptor Table Pointer Register0
Ch/ 18Ch	XOR Descriptor Table Pointer Register1
10h/ 190h	XOR Descriptor Table Pointer Register2
14h/ 194h	XOR Descriptor Table Pointer Register3
18h/ 198h	XOR #0 S/G Engine Address counter Register
1Ch/ 19Ch	XOR #0 S/G Engine byte count counter Register
20C/ 1A0h	XOR #1 S/G Engine Address counter Register
24h/ 1A4h	XOR #1 S/G Engine byte count counter Register
28C/ 1A8h	XOR #2 S/G Engine Address counter Register
2Ch/ 1ACh	XOR #2 S/G Engine byte count counter Register
30h/ 1B0h	XOR #3 S/G Engine Address counter Register
34h/ 1B4h	XOR #2 S/G Engine byte count counter Register
38h/ 1B8h	XOR Next Command Packet Pointer Register
3Ch/ 1BCh	XOR Control & Status Register

3. Host Control register (BA#2/ BA3)

	Byte3	Byte2	Byte1	Byte0
00h/ 00h	Sequence Counter Control Register 0			
04h/ 04h	Sequence Counter Control Register 1			
08h/ 08h	Sequence Counter Control Register 2			
0Ch/ 0Ch	Sequence Counter Control Register 3			
10h/ 10h	Sequence Counter Control Register 4			
14h/ 14h	Sequence Counter Control Register 5			
18h/ 18h	Sequence Counter Control Register 6			
1Ch/ 1Ch	Sequence Counter Control Register 7			
20h/ 20h	Sequence Counter Control Register 8			
24h/ 24h	Sequence Counter Control Register 9			
28h/ 28h	Sequence Counter Control Register A			
2Ch/ 2Ch	Sequence Counter Control Register B			
30h/ 30h	Sequence Counter Control Register C			
34h/ 34h	Sequence Counter Control Register D			
38h/ 38h	Sequence Counter Control Register E			

3Ch/ 3Ch	Sequence Counter Control Register F
40h/ 40h	Sequence Interrupt Status Port
44h/ 44h	FLASH Control Register
48h/ 48h	PCI Control & Status Register
50h/ 50h	Serial bus control Register
54h/ 54h	Serial bus transfer data register
58h/ 58h	Serial bus receive data register
5Ch/ 5Ch	Extra data register #0
60h/ 60h	Extra data register #1
64h/ 64h	Extra data register #2
68h/68h	MSI control register
6Ch/6Ch	Plug and play control register

ATA/ HOST DMA packet and SG format

1. ATA Packet (Variable size)

PDC20319 series can use command packet to operate ATA command. The packet location is pointed by

Channel #0 ATA Command Packet Pointer Register

Channel #1 ATA Command Packet Pointer Register

Channel #2 ATA Command Packet Pointer Register

Channel #3 ATA Command Packet Pointer Register

The data structure of the packet is as following table.

BYTE 3	BYTE 2	BYTE 1	BYTE 0	
Delay Sequence ID	Sync. Sequence ID	Reserved	Control	00h
PSG[31:0]				04h
NCA[31:0]				08h
Data 1_0	CMD1	Data 0_0	CMD0	0Ch
Data 2_2	Data 2_1	Data 2_0	CMD2	10h
...	Data 3_0		CMD3	14h
...	18h
Data N_0	CMD N

About the information about CMD, please refer to examples that describe as later.

Delay Sequence ID

7	6	5	4	3	2	1	0
Reserved				Delay Sequence ID			

Bit[3:0]: Delay Sequence ID.

Bit[7:4]: Reserved.

Synchronization Sequence ID

7	6	5	4	3	2	1	0
Reserved				Synchronization Sequence ID			

Bit[3:0]: Synchronization Sequence ID.

Bit[7:4]: Reserved.

ATA Packet Control

7	6	5	4	3	2	1	0
Reserved	Reserved	NCA Pause	Delay Enable	None Data Command	DMA R/W	Reserved	

Bit[0:1]: Reserved

Bit[2]: 1 = ATA READ DMA command.

0 = ATA WRITE DMA command.

Bit[3]: 1 = ATA None Data Command.

0 = ATA DMA Command.

Bit[4]: 1= Packet command with delay transaction that depends on synchronization sequence ID.

0= Packet command without delay transaction.

Bit[5]: 1=Pause to execute next packet command after this packet command finished.

0=Continue to execute next packet command after this packet command finished.

Bit[6]: reserved

Bit[7]: Reserved.

Host Memory Scatter/Gather Point (PSG)

31:2	1:0
PSG[31:3]	Reserved(00)

Bit[1:0] Reserved.

Bit[31:2] PSG of Host Memory. This pointer indicates the location of S/G table.

Next Command Point (NCA)

31:2	1:0
NCA[31:2]	Reserved(00)

Bit[1:0] Reserved.

Bit[31:2] Next command address. If NCA is 0h, it indicates no next command.

CMD define the micro-code to execute ATA command. It defines command address, command type and number of command. The DATA following CMD is the corresponding data. Based on the packet definition we can describe 28-bit LBA ATA command, up to 64-bit LBA ATA command.

CMD

7:5	4:3	2:0
Size of Register Issued	Condition	DA

Bit [7:5]: number of unit data to be written. the unit is WORD if the address is 1f0h, otherwise the unit is BYTE.

000: Eight data units to be written,

001: one data unit to be written,

...

111: seven data unit to be written.

Bit [4:3] 00: Unconditional 1fXh write,

01: Combined with bit[2:0] to form extra defined, see bit[2:0].

10: write to 1fXh after status polling and HD's BSY flag =0,

11: write to 1fXh after status polling and HD's DRDY=1,

Bit [2:0]: Address bit 2:0 of PIO command .

The definition of {Bit [4:3], Bit [2:0]} is

01, 110 for 3F6h

01, xxx End of packet and the address is 1FXh (xxx != '110')

Data

7:0/(15:0)
Content /(content of 1f0h only)

Packet Command Set-up Example #1 (for Traditional 28-bit LBA ATA Command):

				offset
Content of 3f6h	001_01_110	Content of 1f6h	001_10_110	0Ch
Content of 1f2h	001_00_010	Content of 1f1h	001_00_001	10h
Content of 1f4h	001_00_100	Content of 1f3h	001_00_011	14h
Content of 1f7h	001_01_111	Content of 1f5h	001_00_101	18h

Description:

Content of 1f6h	001_10_110
-----------------	------------

ASIC have to polling status to make sure drive is not busy, and then select drive (Master/Slave) by write “content of 1f6h” to 1f6h register.

Content of 3f6	001_01_110
----------------	------------

Enable interrupt of HDD by write “content of 3f6h” to 3f6h register.

...	001_00_110
-----	------------

1f1h, 1f2h, 1f3h, 1f4h and 1f5h are unconditional 1fXh write.

Content of 1f7h	001_01_111
-----------------	------------

Program commands register by writing “content of 1f7h” to 1f7h register, and indicate end of this packet.

Example #2 (for Big LBA: 16 bits Sector-Count & 64 bits LBA):

Content of 1f1h	001_10_001	Content of 1f6h	001_10_110	0Ch
Content of 1f2h(1)	002_00_010	Content of 3f6h	001_01_110	10h
Content of 1f3h(2)	content of 1f3h(1)	100_00_011	content of 1f2h(2)	14h
Content of 1f7h	001_01_111	Content of 1f3h(4)	content of 1f3h(3)	18h

Description:

Content of 1f6h	001_10_110
-----------------	------------

Polling status and make sure drive is not busy and then select drive (Master/Slave)

Content of 1f1h	001_10_001
-----------------	------------

Polling status and make sure drive is not busy and then 1fXh write

Content of 3f6h	001_01_110
-----------------	------------

Set 64-bit LBA and enable interrupt of HDD (1000_00x0b)

Content of 1f2h(2)	002_00_010	
		content of 1f2h(2)

Write 1f2h twice, content of 1f2(1): Sector count 7:0, content of 1f2(2): Sector count 15:8

Content of 1f3(2)	Content of 1f3(1)	100_00_011	
		Content of 1f3(4)	content of 1f3(3)

Write 1f3h four times, content of 1f3h(1): LBA 7:0, content of 1f3h(2): LBA 15:8,

content of 1f3h(3): LBA 23:16, content of 1f3h(4): LBA 31:24.

Content of 1f7	001_01_111
----------------	------------

Programs command register, and indicate end of packet.

2. XOR Packet

BYTE 3	BYTE 2	BYTE 1	BYTE 0	
Delay ID	Sync. ID	Reserved	Control	00h
PSG0[31:0]				04h
PSG1[31:0]				08h
PSG2[31:0]				0Ch
PSG3[31:0]				10h
NCA[31:0]				14h

Delay Sequence ID

7	6	5	4	3	2	1	0
Reserved				Delay Sequence ID			

Bit[3:0]: Delay Sequence ID.

Bit[7:4]: Reserved.

Synchronization Sequence ID

7	6	5	4	3	2	1	0
Reserved				Synchronization Sequence ID			

Bit[3:0]: Synchronization Sequence ID.

Bit[7:4]: Reserved.

XOR Packet Command Control

7	6	5	4	3	2	1	0
Reserved		NCA Pause	Delay Enable	Reserved		XOR Type	

Bit[0]: 1 = execute XOR command.

0 = execute Compare Command.

Bit[3:1]: Reserved.

Bit[4]: 1= Packet command with delay transaction that depends on synchronization sequence ID.

0= Packet command without delay transaction.

Bit[5] 1=Pause to execute next packet command after this packet command finished.

0=Continue to execute next packet command after this packet command finished.

Bit[7:6]: Reserved.

Host Memory Scatter/Gather Point (PSGn)

31:2	1:0
PSGn[31:2]	Reserved(00)

Bit[1:0] Reserved.

Bit[31:2] PSG of Host Memory. If PSGn is 0, it indicates no PSGn.

Next Command Point (NCA)

31:2	1:0
------	-----

NCA[31:2]	Reserved(00)
-----------	--------------

Bit[1:0] Reserved.

Bit[31:2] Next command address. If NCA is 0, it indicates no next command.

3. SG format (8 bytes)

BYTE 3	BYTE 2	BYTE 1	BYTE 0
SG address			
8 bits control	Reserved	SG byte count	

SG Address

31:0
SG Address

Bit[31:0] SG Address. The 4 bytes specify the byte address of a physical memory region.

SG Byte Count

15:0
SG Byte Count

Bit[15:0] SG Byte Count. The 2 bytes specify the byte count of a physical memory region. A value of zero in these three bytes indicates 64K.

Control bit definition

7	6	5	4	3	2	1	0
Termination(1)	R	reserved	reserved	reserved	Reserved		

Bit[2:0] Reserved.

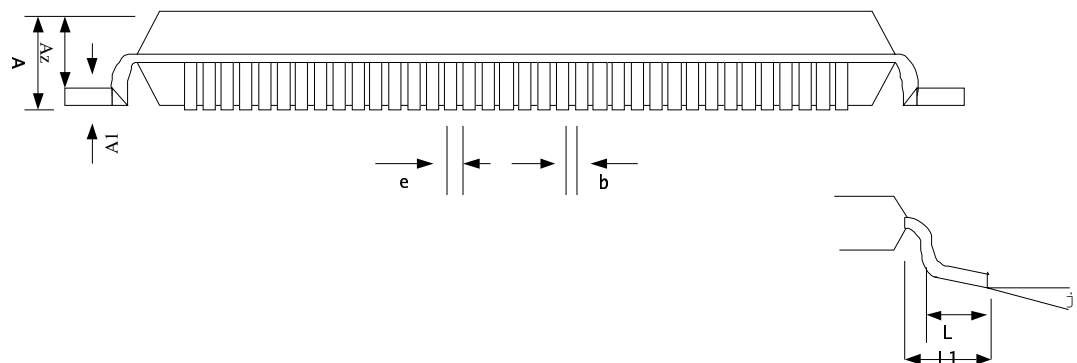
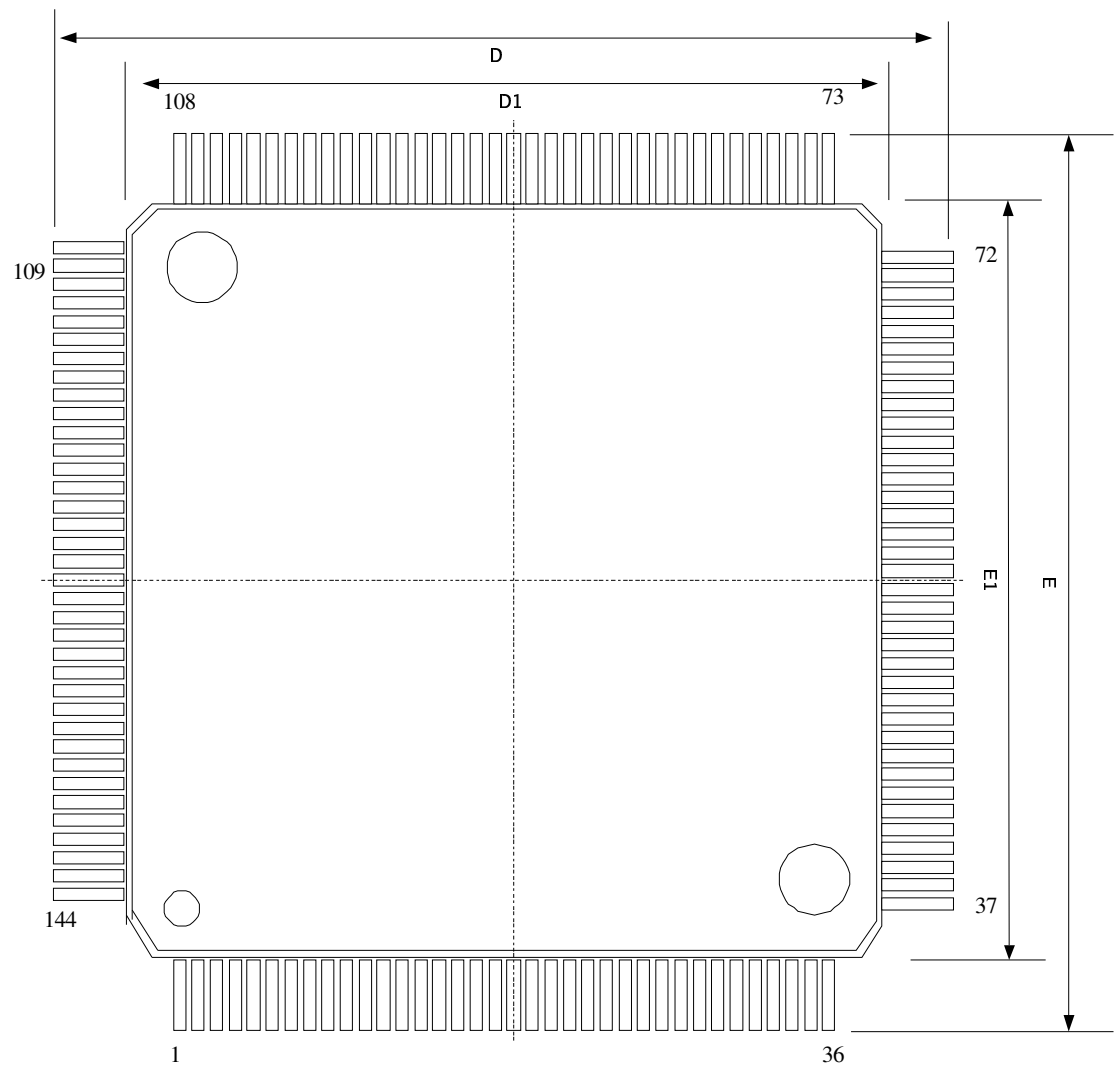
Bit[3] IDE Scatter/Gather Data Dump.

Bit[5:4] reserved

Bit[6] Reserved.
Bit[7] EOT. End of S/G table.

MECHANICAL SPECIFICATION

1.



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	-	0.002	-	-
Az	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D	21.83	22.00	22.15	0.860	0.866	0.872
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	21.83	22.00	22.15	0.860	0.866	0.872
E1	19.90	20.00	20.10	0.783	0.787	0.791
e	0.5BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039REF		
θ	0°	3.5°	7°	0°	3.5°	7°

DC/AC SPECIFICATION

1. Power Requirement

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute Digital I/O Pad Power Supply	VDDIO	CLK _{PCI} =33Mhz			30	mA
Absolute Digital Power Supply	VCC				270	mA
Absolute Analog Power Supply for TBG	VAA1	CLK _{TBG} =150Mhz			10	mA
Absolute Analog Power Supply for PHY	VAA2				240	mA

2. Absolute Maximum Rating

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute Digital Power Supply Voltage	VCC _{ABS}		-0.5		1.93	V
Absolute Digital I/O Pad Supply Voltage	VDDIO _{ABS}		-0.5		3.6	V
Absolute Analog Power Supply Voltage for TBG	VAA1 _{ABS}		-0.5		3.6	V
Absolute Analog Power Supply Voltage for PHY	VAA2 _{ABS}		-0.5		3.6	V
Absolute Input Voltage	V _{inABS}		-0.4		VDDIO+0.4	V
Absolute Storage Temperature	T _{storABS}		-55		85	°C
Absolute Junction Temperature	T _{juncABS}				125	°C

3. Recommended operating conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Ambient Operating Temperature			0		70	°C
Junction Operating Temperature			0		125	°C
Operating Digital Power Supply Voltage	VCC _{OP}		1.8-8%		1.8+8%	V
Operating Digital I/O Pad Supply Voltage	VDDIO _{OP}		3.3-8%		3.3+8%	V
Operating Analog Power Supply Voltage for TBG	VAA1 _{OP}		3.3-8%		3.3+8%	V
Operating Analog Power Supply Voltage for PHY	VAA2 _{OP}		3.3-8%		3.3+8%	V

4. PCI I/O DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input High Voltage	V _{IH}		2.0		5.5	V
Input Low Voltage	V _{IL}		-0.4		0.8	V
Output High Voltage	V _{OH}					V
Output Low Voltage	V _{OL}					V
Driver Sink Current	I _{OL}					mA
Driver Source Current	I _{OH}					uA

5. PCI I/O AC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Rising Slew Rate	S _{RISE}	Programmable	0.5		4.4	V/ns
Falling Slew Rate	S _{FALL}	Programmable	0.7		4.4	V/ns
Low to High Input Threshold	V ₊					V
High to Low Input Threshold	V ₋					V
Device Capacitance	C _{DEVICE}					pF
Output Impedance	R _{OUT}	Programmable	28	45	78	m Ohm
Maximum Toggling Rate	F _{MAX}				70	MHz