



MAN-0646U2-000  
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# PCI646U2

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Bus Master Ultra DMA  
PCI-IDE Chip Specification



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## Revision History

Revision	Date	Comments
1.0	4/7/98	First release
1.1	5/5/98	Changed signal DCHRDY1 on pin 61 from Primary Channel Drive Channel Ready to Secondary Channel Drive Channel Ready
1.2	6/15/98	PCI646U2 and PCI643U2 specifications merged into single document under direction of Semiconductor Marketing. Numerous corrections made.
1.3	3/3/99	Updated jumper table. (This revision is applicable to the PCI646U2-402 chip.) Removed all references to 643U2 in accordance with E-mail from Engineering. Made various text changes: added sections 1.19 and 1.20 and Appendix B.

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# 1 PCI646U2 Chip Specifications

The PCI646U2 chip is a PCI-to-IDE controller, designed for 5V systems. It is designed to comply with the PCI Local Bus Specification (Revision 2.1) and the PCI Power Management Interface Specification (Revision 1.0). It can support two channels (a total of four IDE devices) in any mode defined in the ATA-4 Specification<sup>1</sup>.

## 1.1 Pin Descriptions

The following is an alphabetical listing of signals and their pin assignments. Refer to paragraph 1.15 for a numerically-sorted pinout. Please refer to the pinout diagram for the locations of the pins.

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### NOTE

The recommended value of 1K $\Omega$  for pull-up/pull-down resistors is based on those disk drives on the market at this time. As more drives become available, it is recommended that the designer evaluate the best resistor value for each new disk drive.

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**TYPE IDENTIFICATION:** Each pin is assigned a type, which identifies the pin category as determined by the PCI specification. The types are as follows:

Type	Description
B/T	Bi-directional Tri-state Input/Output
I	Input
O	Output
O/D	Open Drain
S/T/S	Sustained Tri-states
T/O	Tri-state Output

Signal	Pin	Type
2NDIDEEN#/ DMACK0#	87	B/T

### Function

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This signal normally is used in response to DMARQ0 to either acknowledge that data has been accepted, or that data is available. At power-up reset, the state of this signal is used to enable or disable the secondary channel. A 1K $\Omega$  pull-down resistor is required to enable secondary channel access: otherwise, secondary channel access will be disabled. Refer to the bootstrap jumpers table in section 1.16 for additional details.

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<sup>1</sup> Multiword DMA mode 0 is not supported.

Signal	Pin	Type
2NDIOR#/ 2NDHDMARDY#/ 2NDHSTROBE	77	O

#### Function

Secondary Channel Disk I/O Read is an active low output which enables data to be read from the drive. The duration and repetition rate of DIOR# cycles is determined by PCI646U2 programming. DIOR# is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the secondary channel drive. This signal is also defined as secondary channel HDMARDY# in Ultra DMA read mode.

Signal	Pin	Type
2NDIOW#/ 2NDSTOP	78	O

#### Function

Secondary Channel Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition rate of DIOW# cycles is determined by PCI646U2 programming. DIOW# is driven high when inactive. This signal is defined as secondary channel STOP in Ultra DMA mode.

Signal	Pins	Type
AD[31..0]	7-14, 17-20, 23-26, 28-35, 42-49	B/T

#### Function

Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME # is asserted. During the address phase AD[31..0] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. During data phases AD[7..0] contain the least significant byte (lsb) and AD[31..24] contain the most significant byte (msb). Write data are stable and valid when IRDY# is asserted and read data are stable and valid when TRDY# is asserted. Data are transferred during those clocks where both IRDY# and TRDY# are asserted.

Signal	Pins	Type
C/BE[3..0]#	3-6	B/T

#### Function

Byte Enable bits 0 through 3 form the host CPU address bus. These inputs are active low and specify which bytes will be valid for master read/write data transfers.

Signal	Pin	Type
SID# / DMACK1#	88	B/T

#### Function

This signal normally is used in response to DMARQ1 to either acknowledge that data has been accepted, or that data is available. At power-up reset, the state of this signal and jumper number 10 will determine whether to load the CMD signatures into the subsystem ID and subsystem vendor ID configuration registers. Refer to the bootstrap jumpers table in section 1.16 for additional details.

Signal	Pin	Type
DCHRDY0/ DDMARDY0#/ DSTROBE0	76	I

#### Function

The Primary Channel Drive Channel Ready is an active high input. It indicates that the IDE disk drive has completed the current command cycle. A 1K $\Omega$  pull-up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the drive. This signal is also defined as DDMARDY# in Ultra DMA write mode.

Signal	Pins	Type
DCS0#	55	B/T

#### Function

This signal is normally the Drive Chip Select for Command Block Register access to the Primary Channel. At power-up reset the state of this signal is latched on a register located at PCI Configuration Register Index 4FH, bit 1. By default, a 1K $\Omega$  pulldown resistor is required.

Signal	Pins	Type
DCS1#	56	B/T

#### Function

This signal is normally the Drive Chip Select for Control Block Register access to the Primary Channel. At power-up reset the state of this signal determines whether the chip powers up as an IDE device or a RAID device. If power-up as a RAID device is desired, a 1K $\Omega$  pulldown resistor is required. Otherwise, the chip powers up as an IDE device. Configuring the device to RAID Mode can avoid conflicts arising from the motherboard's BIOS assignment of IDE addresses.

Signal	Pin	Type
DCS2#	80	B/T

#### Function

This signal is normally the Drive Chip Select for Command Block Register access to the Secondary Channel. At power-up reset the state of this signal determines whether or not the chip powers up in native mode. If DCS2# is pulled down with a 1K $\Omega$  resistor at reset, the chip would then power up in native mode.

Signal	Pin	Type
DCS3#	79	B/T

#### Function

This signal is normally the Drive Chip Select for Control Block Register access to the Secondary Channel. At power-up reset the state of this signal determines whether or not EPROM access is enabled. EPROM support will be enabled if a 1K $\Omega$  pulldown resistor is in place. EPROM support is for add-on card design in order to resolve any compatibility issue with motherboard BIOS.

Signal	Pin	Type
DEVSEL#	93	S/T/S

#### Function

Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.

Signal	Pin	Type
DCHRDY1/ DDMARDY1#/ DSTROBE1	61	I

#### Function

The Secondary Channel Drive Channel Ready is an active high input. It indicates that the IDE disk drive has completed the current command cycle. A 1K $\Omega$  pull-up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the drive. This signal is also defined as DDMARDY# in Ultra DMA write mode.

Signal	Pin	Type
DIOR#/ HDMARDY#/ HSTROBE	57	O

#### Function

Primary Channel Disk IO Read is an active low output which enables data to be read from the drive. The duration and repetition rate of DIOR# cycles is determined by PCI646U2 programming. DIOR# is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the primary channel drive. This signal is also defined as primary channel HDMARDY# in Ultra DMA read mode.

Signal	Pin	Type
DIOW#/STOP	58	O

#### Function

Primary Channel Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition rate of DIOW# cycles is determined by PCI646U2 programming. DIOW# is driven high when inactive. This signal is defined as primary channel STOP in Ultra DMA mode.



Signal	Pin	Type
DIRQ1	75	I

#### Function

Disk Interrupt is an input to the PCI646U2 used to generate the IRQ14 output when the primary IDE channel is in legacy mode. When the primary IDE channel is in native mode, this pin generates the INTA# output. DIRQ1 is asserted low then high by the drive at the beginning of a block transfer. This input should have a 1K $\Omega$  pull-down resistor connected to it.

Signal	Pin	Type
DIRQ2	86	I

#### Function

Disk Interrupt is an input to the PCI646U2 used to generate the IRQ15 output when the secondary IDE channel is in legacy mode. When the secondary IDE channel is in native mode, this pin generates the INTA# output. DIRQ2 is asserted low then high by the drive at the beginning of a block transfer. This input should have a 1K $\Omega$  pull-down resistor connected to it.

Signal	Pin	Type
DMARQ0	94	I

#### Function

This signal is used in a handshake manner with DMACK0#, and shall be asserted HIGH by the primary drive when it is ready to transfer data to or from the host.

Signal	Pin	Type
DMARQ1	60	I

#### Function

This signal is used in a handshake manner with DMACK1# and shall be asserted HIGH by the secondary drive when it is ready to transfer data to or from the host.

Signal	Pin	Type
DRST#	59	O

#### Function

Disk Reset is an active low output which signals the IDE drive(s) to initialize its control registers. DRST# is a buffered version of the RESET# input and connects directly to the ATA connector.

Signal	Pins	Type
DSA[0]	68	B/T
DSA[1]	69	B/T
DSA[2]	70	B/T

#### Function

Disk Address bits 0 through 2 are normally outputs to the ATA connector for register selection in the drive(s). These three signals are decoded from the AD[2] and C/BE[3..0] inputs. They are also sampled as inputs on the falling edge of RESET#. All of these pins have internal pull-up resistors. 1K $\Omega$  resistors are recommended where pull-32.)

Signal	Pins	Type
DSD[15..0]	36-39, 50-53, 62-65, 71-74	B/T

#### Function

Disk Data bits 0 through 15 are the 16-bit bi-directional data bus which connects to the IDE drive(s). DSD[7..0] define the lowest data byte while DSD[15..8] define the most significant data byte. The DSD bus is normally in a high-impedance state and is driven by the PCI646U2 only during the DIOW# command pulse or during the DIOR# toggling in Ultra DMA mode.

Signal	Pin	Type
ENIDE	21	I

#### Function

ENable IDE is an active high input that controls the PCI646U2's default disk operation mode following reset. When set low, the PCI646U2's IDE cycles are disabled following reset. This mode allows software to scan for system hardware and enable the PCI646U2 via the PCMD register (index 4). When left floating or pulled high, the PCI646U2 is enabled and cannot be disabled via software.

Signal	Pin	Type
FRAME #	98	S/T/S

#### Function

Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME # is asserted to indicate a bus transaction is beginning. While FRAME # is asserted, data transfers continue. When FRAME # is deasserted, the transaction is in the final data phase.

Signal	Pin	Type
IDSEL	100	I

#### Function

Initialization Device Select is used as a chip select during configuration read and write transactions.

Signal	Pin	Type
INTA#	84	O/D

#### Function

Interrupt A is used to request an interrupt in PCI IDE Native Mode. INTA# is open collector and is pulled up when both IDE ports are in Legacy Mode.

Signal	Pin	Type
IRDY#	99	S/T/S

#### Function

Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.

Signal	Pin	Type
IRQ14	22	T/O

#### Function

IRQ14 is used to request an interrupt in PCI IDE Legacy Mode. (For PC-AT compatibles.) IRQ14 is tri-stated when IDE port 0 is in Native Mode.

Signal	Pin	Type
IRQ15	83	T/O

#### Function

IRQ15 is used to request an interrupt for secondary IDE port in PCI IDE Legacy Mode. (PC-AT compatible.) IRQ15 is tri-stated when IDE port 1 is in Native Mode.

Signal	Pin	Type
PAR	96	B/T

#### Function

PAR is even parity across AD[31..0] and C/BE[3..0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31..0] but delayed by one clock.)

Signal	Pin	Type
PCICLK	89	I

#### Function

Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RESET and IRQ, are sampled on the rising edge of PCICLK, and all other timing parameters are defined

with respect to this edge.

Signal	Pin	Type
PCIGNT#	82	I

---

**Function**

This signal indicates to the agent that access to the PCI bus has been granted.

Signal	Pin	Type
PCIMODE	2	I

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**Function**

PCIMODE is set to high when chip is used in normal operation.

Signal	Pin	Type
PCIREQ#	81	T/O

---

**Function**

This signal indicates to the arbiter that this agent desires use of the PCI bus.

Signal	Pin	Type
PERR#	95	S/T/S

---

**Function**

Error may be pulsed active by an agent that detects a parity error. PERR# can be used by any agent to signal data corruptions. However, on detection of a PERR# pulse, the central resource may generate a nonmaskable interrupt to the host CPU, which often implies that the system will be unable to continue operation once error processing is complete.

Signal	Pin	Type
RESET#	1	I

---

**Function**

RESET# is an active low input that is used to set the internal registers of the PCI646U2 to their initial state. RESET# is typically the system power-on reset signal as distributed on the PCI bus.

Signal	Pin	Type
STOP#	97	S/T/S

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**Function**

STOP# indicates the current target is requesting the master to stop the current transaction.

Signal	Pin	Type
TEST0#	85	I

#### Function

This pin is used when PCIMODE = 0 to select different DC tests for this chip.

Signal	Pin	Type
TRDY#	92	S/T/S

#### Function

Target Ready indicates the target agent's ability to complete the current data phase of the transaction. TRDY# is used with IRDY#. A data phase is completed on any clock when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD(31..0). During a write, it indicates the target is prepared to accept data.

Signal	Pins	Type
VDD	16, 41, 67, 91	I

#### Function

Positive power supply input.

Signal	Pins	Type
VSS	15, 27, 40, 54, 66, 90	I

#### Function

Ground reference power supply input.

## 1.2 Register Definition

### (1) Standard Configuration Header

31	16	15	0	
Device ID*		Vendor ID = 1095h		00h
Status		Command		04h
Class-code*			Revision ID*	08h
BIST = 00000000b	Header Type = 00000000b	Latency Time = 00000000b	Cache Line Size = 00000000b	0Ch

\* Refer to the following table for appropriate values for Device ID, Revision ID and Class Code:

Device	Configuration	Device ID	Revision ID	Class Code
PCI646U2	Storage Mode	0646h	07h	01018xh

#### NOTE

Class code may vary depending on configuration pins. Refer to jumper number 7 in the jumper table in section 1.16; and PROGIF Index 09h in section 1.4 for more information.

## (2) Base Address Registers

Base-Address 0 29 valid bits IDE CS0 (I/O map) Default I/O Range = 000001F0h-000001F7h			Bit 2:0 = 001b	10h
Base-Address 1 30 valid bits IDE CS1 (I/O map) Default I/O Range = 000003F4h-000003F7h			Bit 1:0 = 01b	14h
Base-Address 2 29 valid bits IDE CS2 (I/O map) Default I/O Range = 00000170h-00000177h			Bit 2:0 = 001b	18h
Base-Address 3 30 valid bits IDE CS3 (I/O map) Default I/O Range = 00000374h-00000377h			Bit 1:0 = 01b	1Ch
Base-Address 4 28 valid bits PCI Bus Master/DMA Registers & IDE Timing CNT REGS			Bit 3:0 = 0001b	20h
Base Address 5 Not used — return zero				24h
Subsystem ID*		Subsystem Vendor ID		2Ch
ROM Expansion				30h
Reserved			Capability Pointer = 60h	34h
Reserved				38h
Max_lat = 00000100b	Min_Gnt = 000000010b	Interrupt Pin = 00000001b	Interrupt Line = 00001110b	3Ch

\* The subsystem ID and subsystem vendor ID are determined by jumper number 10 in section 1.16.

### 1.3 Status/Command Register (04h)

Bit	Read/Write	Description
0	R/W	Controls the response to the I/O space specified in the Base Address Register. Default value is determined by the ENIDE pin 21 1—chip enable 0—chip disable
1	R/W	Memory space access enable. Default value is determined by DCS #3. 0—disable
2	R/W	Bus Master enable. Default is disable. 1—enable 0—disable
3	R	Special cycle response 0—disable
4	R	Invalidate command 0—disable
5	R	VGA 0—
6	R/W	Parity error response 0—ignore the parity error
7	R	Address and DATA stepping 0—address/data stepping disable
8	R	PCI signal SERR# driver enable 0—disable
9	R	Fast back-to-back transfer 0—disable
10-19		Reserved
20	R	New capabilities 1—implemented
21-22		Reserved
23	R	Fast back-to-back capable 1—capable
24	R/W	Master Data Parity Error Detected 0—no action 1—reset
25-26	R	Devsel Timing 01—medium timing
27		Reserved
28	R/W	Received Target Abort 1—reset 0—no action
29	R/W	Received Master Abort 1—reset 0—no action
30		Reserved

31	R/W	Slave Data Parity Error Detected 1—reset 0—no action
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## 1.4 Configuration Registers

Name	Function	Index
PROGIF	<p>This programming interface is only applied to the chip when it is operated in IDE mode. For RAID mode, the value read from this register is 00h.</p> <p>The following values illustrate the different modes in which the IDE chip can be operated:</p> <ul style="list-style-type: none"> <li>= 80h (RO) when DSA1 is pulled down at reset (legacy mode only; non-programmable).</li> <li>= 8Ah (R/W) when DSA1 is not pulled down at reset (legacy mode, but chip can be programmed for native mode).</li> <li>= 8Fh (R/W) when DSA1 is not pulled down and DCS2# is pulled down at reset (native mode, but can be programmed to legacy mode).</li> </ul> <p>Refer to section 1.5, bit 6 of Index 50h, for more information about jumper DSA1. Refer to the PCI SIG's PCI IDE Controller Specification Rev. 1.0 for a detailed description.</p>	9

Name	Bits (R/W)	Description	Index
SUBCONF	0 (R/W)	Enable write to subsystem/subsystem vendor ID (Index 2Ch) 1—Enable 0—Disable (default)	04Fh
	1 (R)	Status of signal DCS0# at power-up reset.	
	2 (R/W)	Enable write to subclass code in the PCI Configuration Register at index 0Ah. 1—Enable 0—Disable (default)	



## 1.5 IDE Timing Control Registers

Name	Function	Index
CFR	Configuration (R)	50h

### Bits

6	DSA1 Jumper 0—Base address registers 0 thru 3 are read-only and values are 0. In IDE mode, the PCI Configuration Register index 9 will read 80. 1—In IDE mode, the PCI Configuration Register index 9 will read 8A or 8F. If enabled in native mode, the base address registers 0 thru 3 are configurable.
2	IDE drive 0/1 interrupt status Write 1 will clear this bit 0—no interrupt pending 1—interrupt pending

Name	Function	Index
CNTRL	Drive 0/1 Control Register (RW) (note 1)	51h

### Bits

7	Drive 1 read ahead control register 0—enable 1—disable
6	Drive 0 read ahead control register 0—enable 1—disable
3	Second channel control (default value determined by 2NDIDEEN# jumper) 0—disable 1—enable
2	Primary channel control (default value determined by DSA<0> jumper) 0—disable 1—enable

Name	Function	Index
CMDTIM	IDE Task File Timing Control Register (RW) All four devices on both channels use the same command timing.	52h

### Bits

7-4	IOR/IOW active count (note 2)
3-0	IOR/IOW recovery count (note 2)

### NOTES:

- 1) In accordance with ATA spec, drive 0/1 denotes the master/slave drive of the primary IDE disk channel.
- 2) Refer to sections 1.8 and 1.9 for active/recovery count.

<b>Name</b>	<b>Function</b>	<b>Index</b>
ARTTIM0	Drive 0 Address Setup Register (RW)	53h

#### **Bits**

7-6	Address setup time count 00—4 clocks 01—2 clocks 10—3 clocks 11—5 clocks
-----	--

#### **NOTE**

Whichever has the higher count between ARTTIM0 and ARTTIM1 will be selected for the primary channel.

<b>Name</b>	<b>Function</b>	<b>Index</b>
DRWTIM0	Drive 0 Data Read/Write or DACK Timing Register (RW)	54h

#### **Bits**

7-4	Active count
3-0	Recovery count

<b>Name</b>	<b>Function</b>	<b>Index</b>
ARTTIM1	Drive 1 Address Setup Register (RW)	55h

#### **Bits**

7-6	Address setup time count 00—4 clocks 01—2 clocks 10—3 clocks 11—5 clocks
-----	--

#### **NOTE**

Whichever has the higher count between ARTTIM0 and ARTTIM1 will be selected for the primary channel.

<b>Name</b>	<b>Function</b>	<b>Index</b>
DRWTIM1	Drive 1 Data Read/Write or DACK Timing Register (RW)	56h

#### **Bits**

7-4	Active count
3-0	Recovery count

<b>Name</b>	<b>Function</b>	<b>Index</b>
ARTTIM23	Drive 2/3 Control/Status Register (RW) (note 1)	57h

#### **Bits**

7-6	Drive 2/3 Address Setup Count Register
5	Reserved
4	IDE drive 2/3 interrupt status Write 1 will clear this bit 0—no interrupt pending 1—interrupt pending
3	Drive 3 read ahead 0—enable 1—disable (default)
2	Drive 2 read ahead 0—enable 1—disable (default)
1-0	Reserved

<b>Name</b>	<b>Function</b>	<b>Index</b>
DRWTIM2	Drive 2 Data Read/Write or DACK Timing Register (RW)	58h

#### **Bits**

7-4	Active count
3-0	Recovery count

<b>Name</b>	<b>Function</b>	<b>Index</b>
BRST	Read Ahead Count Register (R/W) Default = 40h  This value equals the read-ahead count in quad words. Example: 40h x 8 = 200h (512) bytes	59h

<b>Name</b>	<b>Function</b>	<b>Index</b>
DRWTIM3	Drive 3 Data Read/Write or DACK Timing Register (RW)	5Bh

#### **Bits**

7-4	Active count (note 2)
3-0	Recovery count (note 2)

#### **NOTES:**

- 1) In accordance with ATA spec, drive 2/3 denotes the master/slave drive of the secondary IDE disk channel.
- 2) Refer to sections 1.8 and 1.9 for active/recovery count.

## 1.6 PCI Power Management Registers

Refer to the PCI Power Management Interface Specification (Revision 1.0) for detailed descriptions.

Name	Function	Index
CAP_ID	Capability ID. "01h" identifies the linked list item as being the PCI Power Management Registers.	60h

### Bit

7-0	Value = 01h. Read only.
-----	-------------------------

Name	Function	Index
N_I_PTR	Next Item Pointer. "00h" indicates there are no additional items in the Capabilities List.	61h

### Bit

7-0	Value = 00h. Read only.
-----	-------------------------

Name	Function	Index
PMC	Power Management Capabilities Register. This is a 16-bit read-only register.	62h

### Bit

15-11	Value = 00h. This indicates that PME# signal is not supported in any power states.
10	Value = 1h. D2 Power Management State will be supported.
9	Value = 1h. D1 Power Management State will be supported.
8-6	Value = 0h. Reserved.
5	Value = 1h (default). Requests that the device initialization routine used to set registers have proper values (instead of default values) before the generic device driver uses it.
	Value = 0h. Indicates that the device initialization routine is not required before the generic class driver is able to use it.
4, 3	Value = 0h.
2-0	Value = 001b. Indicates that this function complies with Revision 1.0 of the PCI Power Management Interface specification.

Name	Function	Index
PMCSR	This 16-bit register is to manage the PCI functions power management state.	64h

### Bit (R/W)

15	Value = 0h.
----	-------------

Name		Function	Index
14, 13	R	Value = 11h. This two-bit Data_Scale field indicates that this function uses 001 as the scale factor to report Power Consumption.	
12-9 R/W		This four-bit Data_Select field is used to select which data is to be reported through the Data Register for Power Consumption. Values from 8h to 15h are reserved.	
8		Value = 0h.	
7-2	R	Reserved.	
1, 0 R/W		Default = 00b. This two-bit field is used to determine the current power state of a function, as follows:  00b = D0 01b = D1 10b = D2 11b = Not implemented	

Name	Function	Index
DR	This read-only Data Register is used to report the state-dependent data requested by the Data_Select field. The value of this register is scaled by the value reported by the Data_Scale field.	67h

Bit	Value
7-0	80H (D0 Power consumed, Data_Select field = 0h) 60H (D1 Power consumed, Data_Select field = 1h) 20H (D2 Power consumed, Data_Select field = 2h) 00H (D3 Power consumed, Data_Select field = 3h) 80H (D0 Power dissipated, Data_Select field = 4h) 60H (D1 Power dissipated, Data_Select field = 5h) 20H (D2 Power dissipated, Data_Select field = 6h) 00H (D3 Power dissipated, Data_Select field = 7h)

## 1.7 PCI Master Control Registers

These registers can be addressed through either the offset of Base Address #4 or the PCI configuration space.

Name	Function	Index
BMIDECR0	Bus Master IDE Command Register 0 for Primary IDE Channel. (R/W)	PCI Configuration Space 70h or Base Address #4 + 00h

### Bit

7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Read or Write Control 0—PCI bus master reads are performed 1—PCI bus master writes are performed
2	Reserved
1	Reserved
0	Start/Stop Bus Master 0—disable bus master operation 1—enable bus master operation

Name	Function	Index
MRDMODE	DMA Master Read Mode Select (R/W)	PCI Configuration Space 71h or Base Address #4 + 01h

### Bits

	Bit 1	Bit 0	Mode
(W)			
1, 0			Reserved
2			Primary IDE channel (Write 1 to clear this bit)
	0	0	no interrupt pending
	0	1	interrupt pending
3			Secondary IDE channel (Write 1 to clear this bit)
	0	0	no interrupt pending
	0	1	interrupt pending
4			Primary channel interrupt enable
	0	0	propagate primary channel IDE interrupts to IRQ14
	0	1	block primary channel IDE interrupts
5			Secondary channel interrupt enable
	0	0	propagate secondary channel IDE interrupts to IRQ15
	0	1	block secondary channel IDE interrupts
6	0	0	no reset on IDE bus

Name	Function	Index
	0      1      reset both IDE channel drives	

Name	Function	Index
BMIDESR0	Bus Master IDE Status Register 0 for IDE Primary Channel (R/W)	PCI Configuration Space 72h or Base Address #4 + 02h

Bit	
7	Simplex only (R)
6	Drive 1 DMA Capable 0—no DMA capability 1—DMA capability
5	Drive 0 DMA capable 0—no DMA capability 1—DMA capability
4, 3	Reserved
2	DMA Interrupt 0—no interrupt occurs on IDE bus for DMA transfer 1—interrupt generated on IDE bus for DMA transfer (software writes 1 to clear bit)
1	Errors 0—no error 1—error (write 1 to clear error)
0	Bus Master IDE Active (Read-only) 0—all data transfer completely 1—data transfer not complete

Name	Function	Index
UDIDETCR0	Ultra DMA IDE Timing Control Register 0 for IDE primary channel (R/W)	PCI Configuration Space 73h or Base Address #4 + 03h

Bit	
7-6	Primary Channel Slave Drive Ultra DMA Cycle Time 00—1 clock 01—2 clocks 10—3 clocks 11—4 clocks (default)
5-4	Primary Channel Master Drive Ultra DMA Cycle Time 00—1 clock 01—2 clocks 10—3 clocks 11—4 clocks (default)
3-2	Reserved
1	Primary Channel Slave Drive DMA Mode 0—Multi-word/Single-word DMA (default)
0	Primary Channel Master Drive DMA Mode 0—Multi-word/Single-word DMA (default)

<b>Name</b>	<b>Function</b>	<b>Index</b>
DTPR0	Descriptor Table Pointer Register 0 for IDE Primary Channel (R/W) 4 bytes	PCI Configuration Space 74h or Base Address #4 + 04h

---

**Bit**


---

31-2	Base address of descriptor table
1-0	Reserved

<b>Name</b>	<b>Function</b>	<b>Index</b>
BMIDECR1	Bus Master IDE Command Register 1 for Second Channel (R/W)	PCI Configuration Space 78h or Base Address #4 + 08h

---

**Bit**


---

7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Read or Write Control 0—PCI bus master reads are performed 1—PCI bus master writes are performed
2	Reserved
1	Reserved
0	Start/Stop Bus Master 0—disable bus master operation 1—enable bus master operation



Name	Function	Index
BMIDESR1	Bus Master IDE Status Register 0 for Second Channel (R/W)	PCI Configuration Space 7Ah or Base Address #4 + 0Ah

#### Bit

7	Simplex only (R)
6	Drive 3 DMA Capable 0—no DMA capability 1—DMA capability
5	Drive 2 DMA capable 0—no DMA capability 1—DMA capability
4, 3	Reserved
2	DMA Interrupt 0—no interrupt occurs on IDE bus for DMA transfer 1—interrupt generated on IDE bus for DMA transfer (software writes 1 to clear bit)
1	Errors 0—no error 1—error (write 1 to clear error)
0	Bus Master IDE Active 0—all data transfer completely 1—data transfer not complete

Name	Function	Index
UDIDETCR1	Ultra DMA IDE Timing Control Register 1 for IDE secondary channel (R/W)	PCI Configuration Space 7Bh or Base Address #4 + 0Bh

#### Bit

7-6	Secondary Channel Slave Drive Ultra DMA Cycle Time 00—1 clock 01—2 clocks 10—3 clocks 11—4 clocks (default)
5-4	Secondary Channel Master Drive Ultra DMA Cycle Time 00—1 clock 01—2 clocks 10—3 clocks 11—4 clocks (default)
3-2	Reserved
1	Secondary Channel Slave Drive DMA Mode 0—Multi-word/Single-word DMA (default)
0	Secondary Channel Master Drive DMA Mode 0—Multi-word/Single-word DMA (default)

Name	Function	Index
DTPR1	Descriptor Table Pointer Register 1 for Second Channel (R/W) 4 bytes	PCI Configuration Space 7Ch or Base Address #4 + 0Ch
Bit		
31-2	Base address of descriptor table	
1-0	Reserved	

## 1.8 Active Count Function

Active Count	R/W Active Time
0000	16 clocks
0001	1 clock
0010	2 clocks
0011	3 clocks
0100	4 clocks
0101	5 clocks
0110	6 clocks
0111	7 clocks
1000	8 clocks
1001	9 clocks
1010	10 clocks
1011	11 clocks
1100	12 clocks
1101	13 clocks
1110	14 clocks
1111	15 clocks

## 1.9 Recovery Count Function

Recovery Count	Read/Write Recovery Time
0000	16 clocks
0001	2 clocks
0010	3 clocks
0011	4 clocks
0100	5 clocks
0101	6 clocks
0110	7 clocks

0111	8 clocks
1000	9 clocks
1001	10 clocks
1010	11 clocks
1011	12 clocks
1100	13 clocks
1101	14 clocks
1110	15 clocks
1111	1 clock

## 1.10 Task File Registers

Name	Host Addr	Function
HDATA*	1F0(170)	data register (RW)
HDWPC	1F1(171)	write pre-comp (WO)
HDERR	1F1(171)	error register (RO)
HDSCCT	1F2(172)	sector count (RW)
HDSSN	1F3(173)	starting sector # (RW)
HDCLL	1F4(174)	cylinder low (RW)
HDCLH	1F5(175)	cylinder high (RW)
HDS DH	1F6(176)	SDH (RW)
HDCMD	1F7(177)	command (WO)
HDSTT	1F7(177)	status (RO)
HDFDR	3F6(376)	fixed disk control auxiliary register (WO)
HDASR	3F6(376)	alternate status auxiliary register (RO)

\*HDATA can be accessed as a 16- or 32-bit-wide register, for all commands.

## 1.11 Configuration Setup

Depending on your motherboard chip set, either Configuration Mechanism #1 or Configuration Mechanism #2 is applicable. Configuration Mechanism #2 is described below. For Configuration #1 methodology, refer to the PCI Spec 2.1.

### Notes:

- 1) Although PCI BIOS (INT 1Ah) is a portable alternative to mechanism #1 and #2, it is not recommended because MS-DOS's EMM386.SYS causes the system to hang when function FIND PCI DEVICE is accessed
- 2) The PCI646U2 supports byte, word, and dword reads/writes of configuration space.

### Configuration Mechanism #2

- 1) Enter PCI Configuration Mode by writing 10h to port CF8h.
- 2) Scan the PCI device IDs from 0h to Fh for the presence of a PCI646U2 controller. (There should be 1095h in port Cx00h and 0646h in port Cx02h, where x=device index.) For other devices and configurations, please refer to Section 1.2 to determine the proper Device ID to be used.

- 3) To read or write internal registers, read or write to port Cxyyh, where x=device ID from (2) and yy=configuration register's index.
- 4) Exit PCI Configuration Mode by writing 00 to port CF8h.

## 1.12 PIO Mode Interrupt Processing

When DSA1 is pulled low during reset, both IDE ports are in PCI IDE Legacy Mode. When DSA1 has no pull-down during reset, each IDE port may independently be set to PCI IDE Legacy Mode or Native Mode via the Programming Interface Byte (configuration register PROGIF, Index 9h).

When an IDE port is in PCI IDE Legacy Mode, the PCI646U2 is compatible with standard ISA IDE. The IDE task file registers are mapped to the standard ISA port addresses, and IDE drive interrupts occur at IRQ14 (primary) or IRQ15 (secondary).

When an IDE port is in PCI IDE Native Mode, the IDE task file registers may be mapped to non-standard port addresses, and IDE drive interrupts occur at PCI INTA#. Therefore, if both IDE ports are in PCI IDE Native Mode, drive interrupts from both IDE ports are multiplexed into PCI INTA#. In this case, the interrupt status bits must be polled to determine which IDE port generated the interrupt, or whether the interrupt was generated by another PCI device sharing INTA# on the bus.

- 1) The host reads CFR (index 50h). If bit 2 is set, then the interrupt occurred on the primary IDE port.
- 2) The host reads ARTTIM23 (index 57h). If bit 4 is set, then the interrupt occurred on the secondary IDE port.
- 3) If 1) and 2) are both false, then the interrupt was generated by another PCI device sharing INTA# with the PCI646U2.

---

### NOTE

The interrupt status of each channel can also be determined by the value of either bit 2 or bit 3 in the MRDMODE register. This register is one of the PCI Master Control registers (refer to section 1.7) and may be accessed through the I/O space, provided that the value of Base Address #4 is valid. This is a safer, more efficient method of accessing the interrupt status in a multitasking environment.

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## 1.13 DMA Programming

See Revision 1.0 of Intel's "Programming Interface for Bus Master IDE Controller" for information about bus master DMA programming.

## 1.14 Read Ahead Operation

The chip will snoop the IDE command register. If a read or read multiple command is written to it, then the chip will load the readahead count according to the current BRST register (index 59h) setting.

## 1.15 IDE Controller Pinout

### Host Interface Pinout

Name	Pin #	Type	Function
RESET#	1	I	Reset input
PCIMODE	2	I	Tied HIGH if PCI mode
C/BE<3>#	3	B/T	
C/BE<2>#	4	B/T	
C/BE<1>#	5	B/T	
C/BE<0>#	6	B/T	
AD<31>	7	B/T	
AD<30>	8	B/T	
AD<29>	9	B/T	
AD<28>	10	B/T	
AD<27>	11	B/T	
AD<26>	12	B/T	
AD<25>	13	B/T	
AD<24>	14	B/T	
AD<23>	17	B/T	
AD<22>	18	B/T	
AD<21>	19	B/T	
AD<20>	20	B/T	
ENIDE	21	I	Enable chip operation
IRQ14	22	T/O	Tri-state output to interrupt 14 (PC-AT compatible)
AD<19>	23	B/T	
AD<18>	24	B/T	
AD<17>	25	B/T	
AD<16>	26	B/T	
AD<15>	28	B/T	
AD<14>	29	B/T	
AD<13>	30	B/T	
AD<12>	31	B/T	
AD<11>	32	B/T	
AD<10>	33	B/T	
AD<9>	34	B/T	
AD<8>	35	B/T	
AD<7>	42	B/T	

Name	Pin #	Type	Function
AD<6>	43	B/T	
AD<5>	44	B/T	
AD<4>	45	B/T	
AD<3>	46	B/T	
AD<2>	47	B/T	
AD<1>	48	B/T	
AD<0>	49	B/T	
PCIREQ#	81	T/O	
PCIGNT#	82	I	
IRQ15	83	T/O	To interrupt 15 (PC-AT compatible)
INTA#	84	O/D	Interrupt request to PCI host
TEST0#	85	I	Select DC test.
PCICLK	89	I	Clock input
TRDY#	92	S/T/S	
DEVSEL#	93	S/T/S	
PERR#	95	S/T/S	
PAR	96	B/T	
STOP#	97	S/T/S	
FRAME#	98	S/T/S	
IRDY#	99	S/T/S	
IDSEL	100	I	

### Drive Interface Pinout

PCI	Pin #	Type	Function
DSD<15>	36	B/T	
DSD<14>	37	B/T	
DSD<13>	38	B/T	
DSD<12>	39	B/T	
DSD<11>	50	B/T	
DSD<10>	51	B/T	
DSD<9>	52	B/T	
DSD<8>	53	B/T	
DCSO#	55	B/T	Chip select for command register access to the primary channel
DCS1#	56	B/T	Chip select for control register access to the primary channel
DIOR#	57	O	IOR# for the primary IDE port

PCI	Pin #	Type	Function
HDMARDY#/ HSTROBE			
DIOW#/STOP	58	O	IOW# for the primary IDE port
DRST#	59	O	Drive Reset
DMARQ1	60	I	
DCHRDY1/ DDMARDY1#/ DSTROBE1	61	I	Drive channel ready 1
DSD<7>	62	B/T	
DSD<6>	63	B/T	
DSD<5>	64	B/T	
DSD<4>	65	B/T	
DSA<0>	68	B/T	Drive address 0
DSA<1>	69	B/T	Drive address 1. Select "Compatibility Mode" (Legacy) or "Native Mode" at power-up.
DSA<2>	70	B/T	Drive address 2
DSD<3>	71	B/T	
DSD<2>	72	B/T	
DSD<1>	73	B/T	
DSD<0>	74	B/T	
DIRQ1	75	I	Primary channel IRQ
DCHRDY0/ DDMARDY0#/ DSTROBE0	76	I	Drive channel ready 0
2NDIOR#/ 2NDHDMARDY#/ 2NDHSTROBE	77	O	IOR# for the secondary IDE port
2NDIOW#/ 2NDSTOP	78	O	IOW# for the secondary IDE port
DCS3#	79	B/T	Drive chip select for control register access to the secondary channel
DCS2#	80	B/T	Drive chip select for command register access to the secondary channel
DIRQ2	86	I	Secondary channel IRQ
2NDIDEEN#/ DMACK0#	87	B/T	
SID# / DMACK1#	88	B/T	
DMARQ0	94	I	

## VDD/VSS Pins

VDD Pins	VSS Pins
16	15
41	27
67	40
91	54
	66
	90

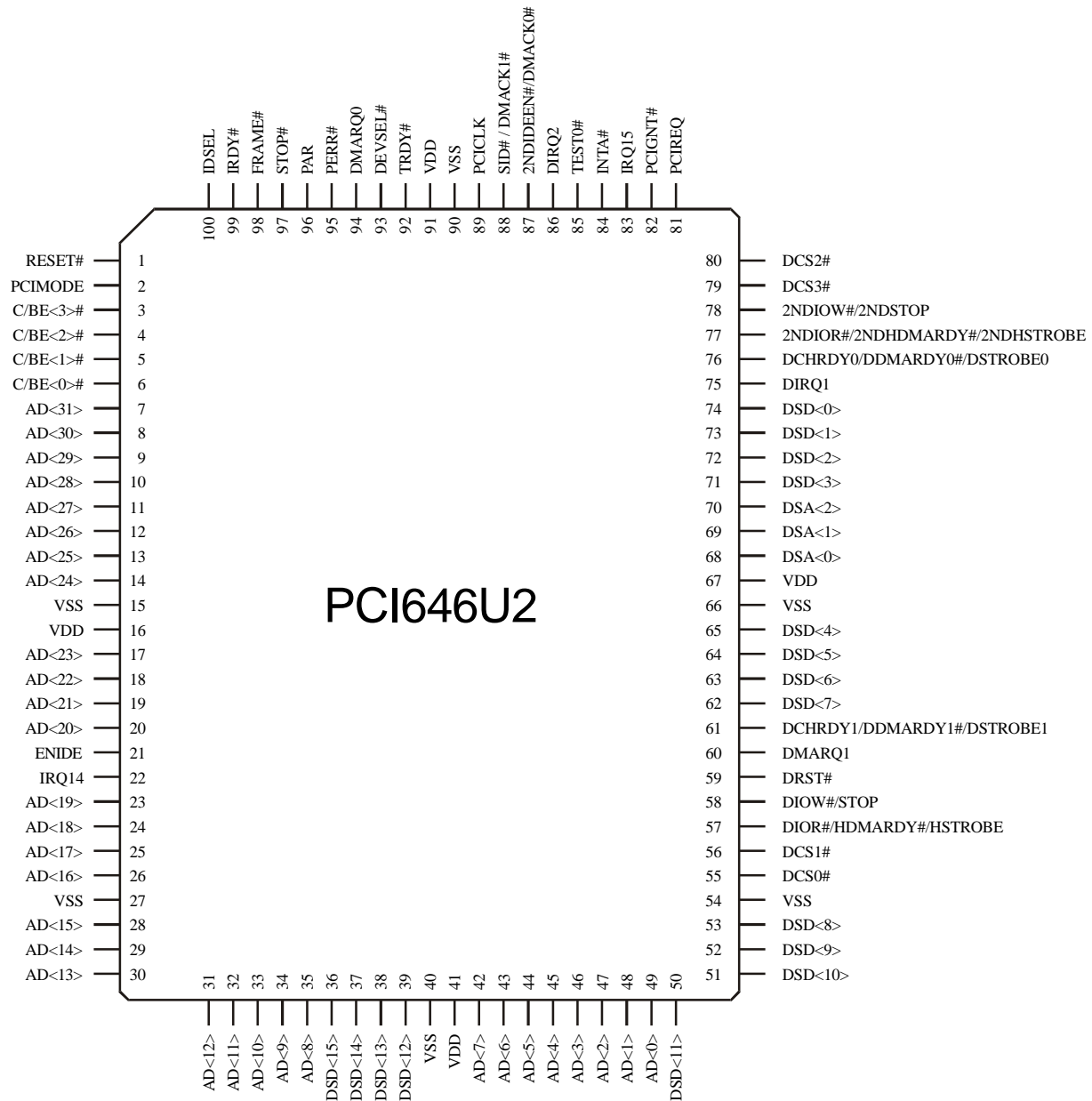
## 1.16 Bootstrap Jumper Settings

No.	Jumper name	Description	Resistive value	Pull down (jumper in)	No pull down (jumper out)
1	DSA0	At power-up reset, the state of this signal is used to enable/disable the primary IDE channel. By default, no pull down is connected to this jumper.	1k ohms	Disable primary IDE channel access	<b>(Default)</b> Enable primary IDE channel access
2	DSA1	When the status of this jumper = 0, base address registers always return 0. Primary IDE channel will use IRQ14 and Secondary IDE channel will use IRQ15. IDE Task file registers are mapped to the default port addresses of 1F <sub>h</sub> (primary) and 17 <sub>h</sub> (secondary). Both channels are operating in legacy mode and can not be switched to native mode by software. When the status of this jumper = 1, base address registers' function depends on the status of JP7, CS2. If JP7 = 0, (jumper in), then channels are native mode capable but boot up as native and can be switched to legacy by software. If JP7 = 1, (jumper out), then channels are also native mode capable but boot up as legacy and can be switched to native mode by software. The software can switch the modes by programming the programmable interface register at index 9 <sub>h</sub> . By default, no pull down is connected to this jumper.	1k Ohms	Not Native Mode Capable	(Default) Native Mode Capable
3	DSA2	This chip is always used as a storage device. Pull down is mandatory to this jumper to configure the chip.	1k ohms	<b>(Default)</b> Power up as a storage device (PID = 0646 <sub>h</sub> )	<b>N/A</b>

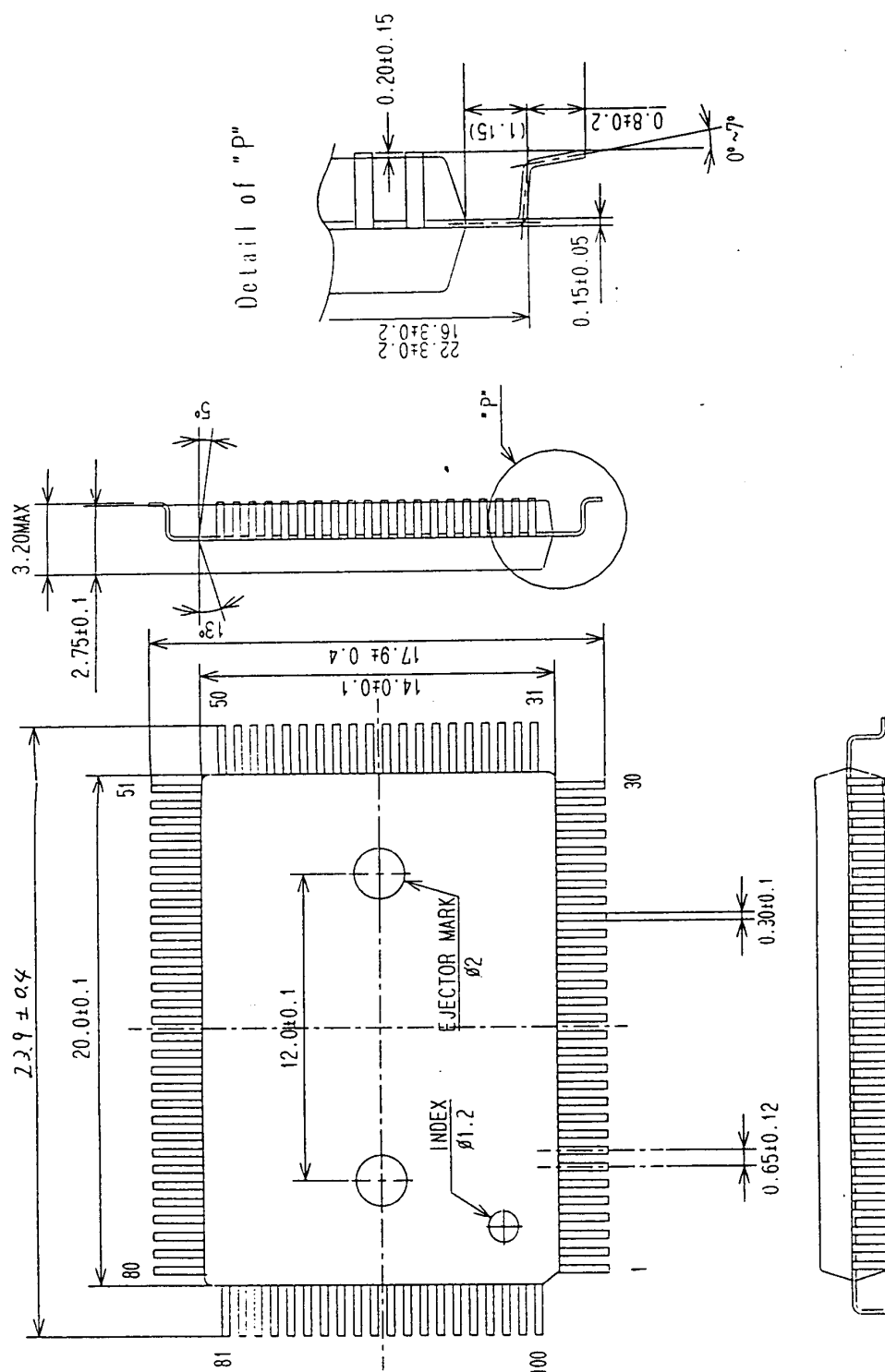


No.	Jumper name	Description	Resistive value	Pull down (jumper in)	No pull down (jumper out)
4	ENIDE	This signal is an active high input that controls the default disk operation mode following reset. When set to low, the chip is disabled following reset. This mode allows software to first scan for system hardware and then enable the chip later. When left floating or pulled high, the chip is enabled and cannot be disabled via software. By default, pull down is required to this jumper.	0 ohm	<b>(Default)</b> Chip is disabled at reset.	Chip is enabled at reset.
5	2NDIDEEN /DMACK0-	At power-up reset, the state of this signal is used to enable/disable the secondary IDE channel. By default, pull down is required to this jumper.	680 ohms	<b>(Default)</b> Enable secondary IDE channel access	Disable secondary IDE channel access
6	CS3-	At power-up reset, the state of this signal determines whether or not EPROM access is enabled. EPROM support is for add-on card design in order to resolve any compatibility issue with motherboard BIOS. EPROM support will be enabled if a pull down resistor is in place.	680 ohms	<b>(Default)</b> EPROM support	No EPROM support
7	CS2-	At power-up reset, the state of this signal determines whether or not the chip powers up in native mode. The chip will power up in native mode if a pull down resistor is in place.	680 ohms	<b>(Default)</b> Native mode	Legacy mode
8	CS1-	At power-up reset, the state of this signal determines whether or not the chip powers up as an IDE device sub-class or a RAID device sub-class. Note that by configuring the device to RAID mode can avoid the conflicts arising from the motherboard's BIOS assignment of IDE address.	680 ohms	RAID device (sub-class code = 04h)	<b>(Default)</b> IDE device (sub-class code = 01h)
9	CS0-	At power-up reset, the state of this signal is latched on a register located at PCI Configuration Register Index 04Fh, bit 1. This is used for FIFO threshold control. By default, pull down is required to this jumper.	680 ohms	<b>(Default)</b> Index 4Fh bit 1 value = '0' Data will start to transfer if FIFO is not empty.	Index 4Fh bit 1 value = '1' Data will start to transfer if FIFO is half full.
10	SID# / DMACK1#-	At power-up reset, the state of this signal determines whether to load the CMD ID into the sub-system ID and sub-system vendor ID configuration registers.	680 ohms	Do not overwrite the sub-system ID and sub-system vendor ID at PCI_RST#	<b>(Default)</b> Replace with CMD values for sub-system ID and sub-system vendor ID at PCI_RST#

## 1.17 Pinout Diagram (PQFP Package)

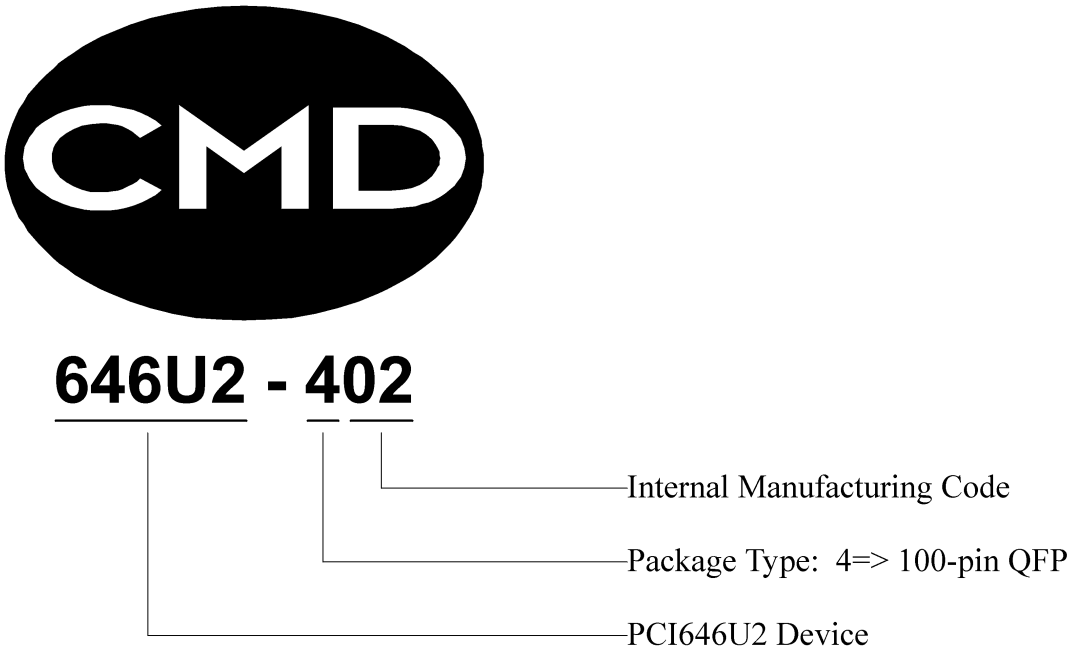


### 1.18 Mechanical Dimensions (PQFP Package)



## 1.19 Physical Part Markings

The latest revision of the PCI0646U2 will be physically marked as follows:



Previous versions of the PCI0646U2 will be marked in one of the following ways:



PCI0646U2



PCI0646U2

## 1.20 Part Number to Order

To order the latest revision of the PCI0646U2 please use the following part number:

**ICS-0646U2-402**

## 2 PCI646U2 Power Specifications

### 2.1 DC Specifications

#### Maximum Ratings

Symbol	Parameter	Limits	Units
VDD	DC supply voltage	-0.3 to +7.0	Volts
Vin	DC Input Voltage	-0.3 to VDD +0.3	Volts
Stg	Storage Temperature	-40 to +125	Deg. C
Iin	DC Input Current	±10	µA

#### Recommended Operating Conditions (Vss = 0V)

Symbol	Parameter	Min	Max	Units
VDD	DC supply voltage	4.75	5.25	Volts
Vin	Input Voltage	Vss	VDD	Volts
Topr	Operating Temperature	0	+70	Deg. C

### 2.2 DC Characteristics

(For VDD= 5V, 0 to 70 Deg. C)

Symbol	Parameter	Min	Max	Units	Notes
VIL	Input Voltage Low	-0.3	0.8	Volts	Note 2
VIH	Input Voltage High	2.0	VDD+0.3	Volts	Note 2
VOL	Output Voltage Low		0.55 0.40	Volts Volts	Note 1 Note 3
VOH	Output Voltage High IOH = -2mA	2.4		Volts	Note 1
ILO	Output Leakage Current	-10	10	µA	
ILI	Input High Current Vin = VDD	-10	10	µA	
IIL	Input Low Current Vin = VSS	-10	10	µA	
CIN	Input or I/O Capacitance		10	pF	

#### Notes

1. All PCI signals are PCI-compliant driver pins. See PCI specifications.
2. DIRQ1, DIRQ2, DMARQ0, DMARQ1, DCHRDY, DCHRDY1 and DSD[0..15] are TTL Schmitt trigger pins.
3. IOL = 16mA: DCS3#, DCS2#, DCS1#, DCS0#, IRQ14, IRQ15, DRST#, DSA[0..2], DIOR#, DIOW#, 2NDIOR#, 2NDIOW#, DSD[0..15], DMACK0# and DMACK1#.

## 2.3 AC Specifications\*

### Timing Waveform

All AC timing is measured from the 0.8V and 2.0V on the source signal to the 0.8V and 2.0V level on the signal under test.

### Clock Timing

Parameter	Min	Max	Units
CLK Frequency	0	40	MHz
CLK Period	25		ns
CLK High Time	10		ns
CLK Low Time	10		ns
CLK Rise Time		2	ns
CLK Fall Time		2	ns

### Host Interface Timing (loading = 50 pf)

Signal		Min (ns)	Max (ns)
FRAME#, IRDY#, TRDY#, CBE#, AD[0..31], STOP#, PAR, PERR#, DEVSEL#, IDSEL, PCIGNT#	Setup time to CLK high	7	
DEVSEL#, FRAME#, STOP#, IRDY#, TRDY#, PAR, PERR#, PCIREQ#	High to low from CLK high	4	11
	Low to high from CLK high	3	10
AD[0..31]	Read delay from CLK high in Target mode	4	11
AD[0..31]	Active to float delay from CLK high	8	28
AD[0..31], CBE#	Write delay from CLK high in Master mode	4	11

### IDE Drive Timing (loading = 75 pf)

Signal		Min (ns)	Max (ns)
DCS0#, DCS1#, DSA[0..2]	High to low from CLK high	6	21
	Low to high from CLK high	5	18
DIOR#, DIOW#	High to low from CLK high	5	18
	Low to high from CLK high	4	15
DSD to DIOW# (2 CLKS)	Low to high setup time	45	56
	Hold time	50	57

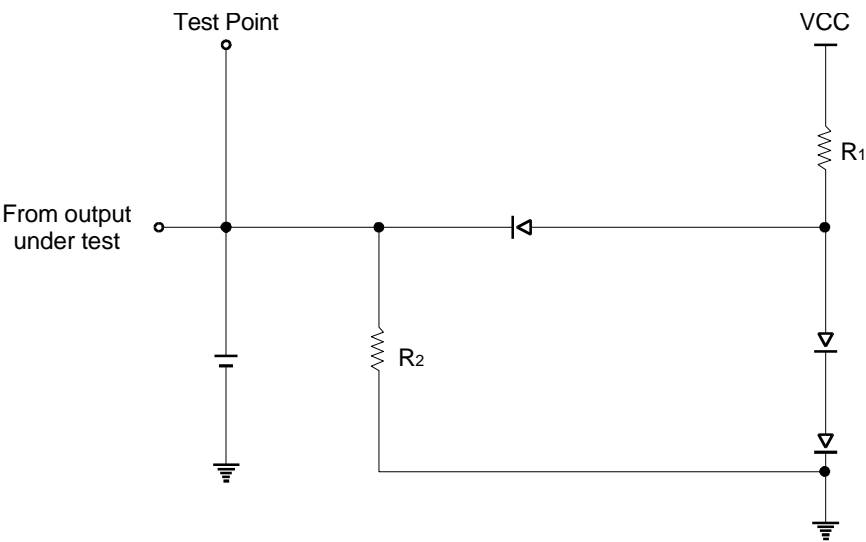
\* Compliance to ATA-4 timing requirements verified with CMD internal test conditions.

DCS0# low to DIOW#, DIOR# low for port 1F0h	52	59
IOCHRDY to CLK high setup time	2	

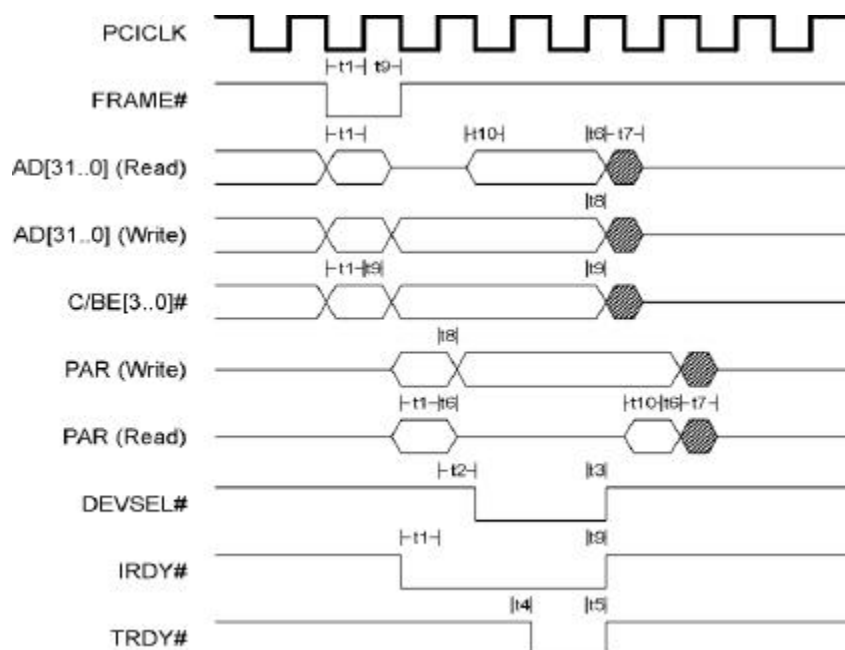
### IDE Drive Timing (loading = 120 pf)

Signal		Min (ns)	Max (ns)
DCS0#, DCS1#, DSA[0..2]	High to low from CLK high	9	33
	Low to high from CLK high	7	24
DIOR#, DIOW#	High to low from CLK high	7	26
	Low to high from CLK high	6	20
DSD[0..15] to DIOW# (2 CLKS)	Low to high setup time	45	56
	Hold time	50	57
DCS0# low to DIOW#, DIOR# low for port 1F0h		52	59
IOCHRDY to CLK high setup time		2	

## 2.4 Output Test Load



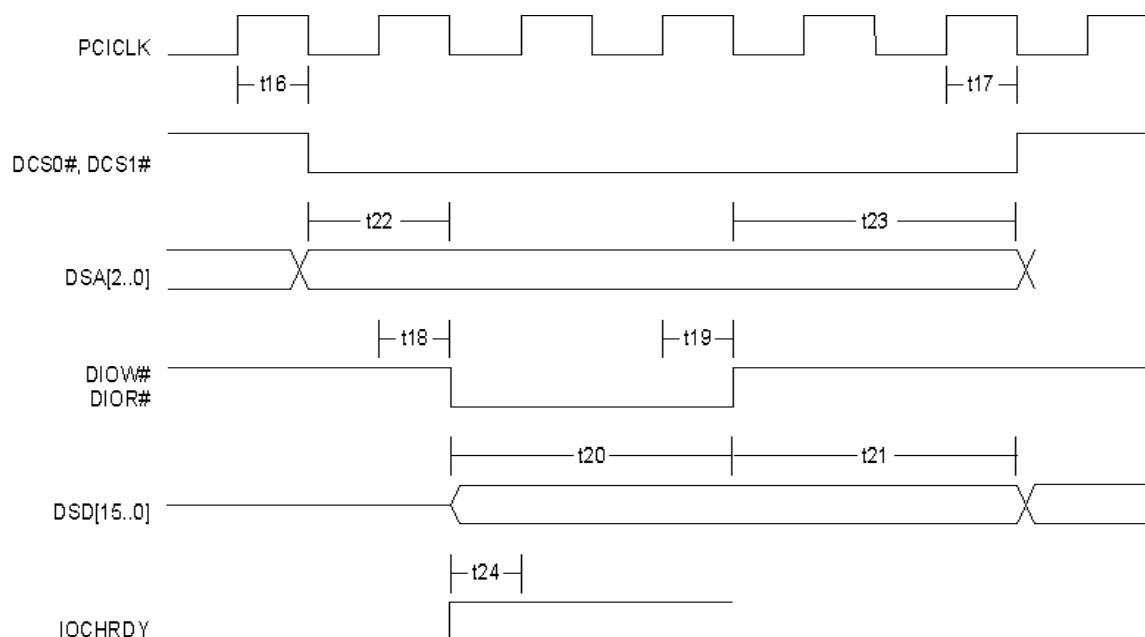
## 2.5 PCI Read/Write Timing in Target Mode



Symbol	Parameter	Timing
t1	FRAME#, IRDY#, C/BE[3..0]#, AD[31..0], PAR setup time	7 ns
t2	DEVSEL#, high to low from CLK high	4-11 ns
t3	DEVSEL#, low to high from CLK high	3-10 ns
t4	TRDY#, high to low from CLK high	4-11 ns
t5	TRDY#, low to high from CLK high	3-10 ns
t6	AD[31..0], PAR hold time in Read	4-11 ns
t7	Active to float delay from CLK	8-28 ns
t8	AD[31..0], PAR hold time in Write	0 ns
t9	IRDY#, C/BE[3..0]#, FRAME# hold time	0 ns
t10	AD[31..0], PAR setup time in Read	19-26 ns

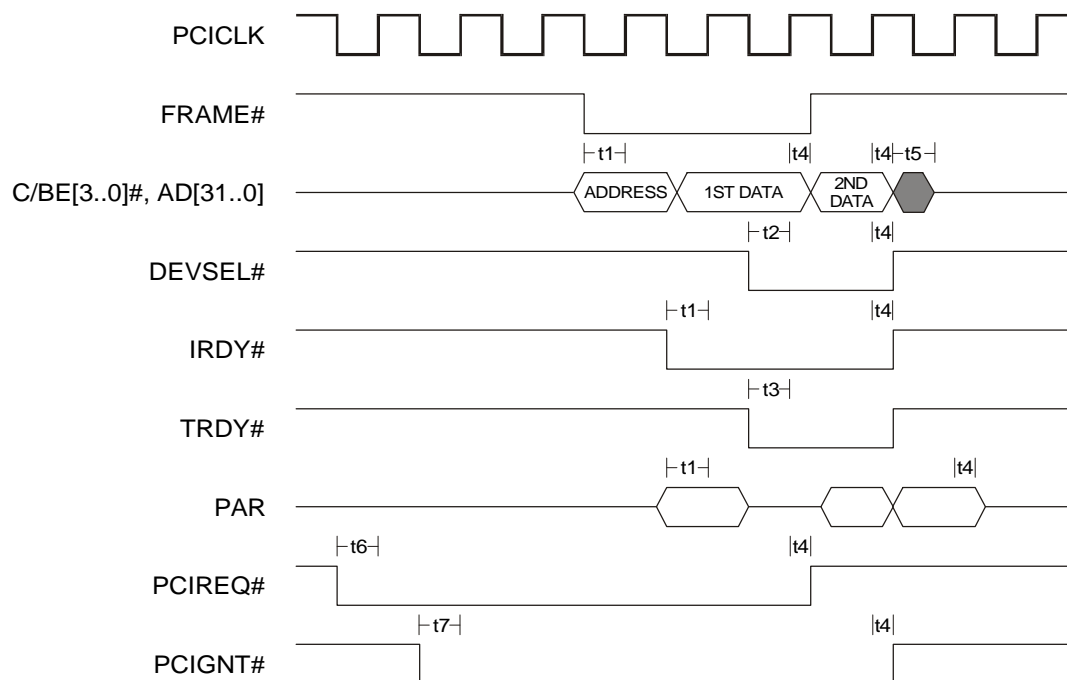


## 2.6 IDE Timing



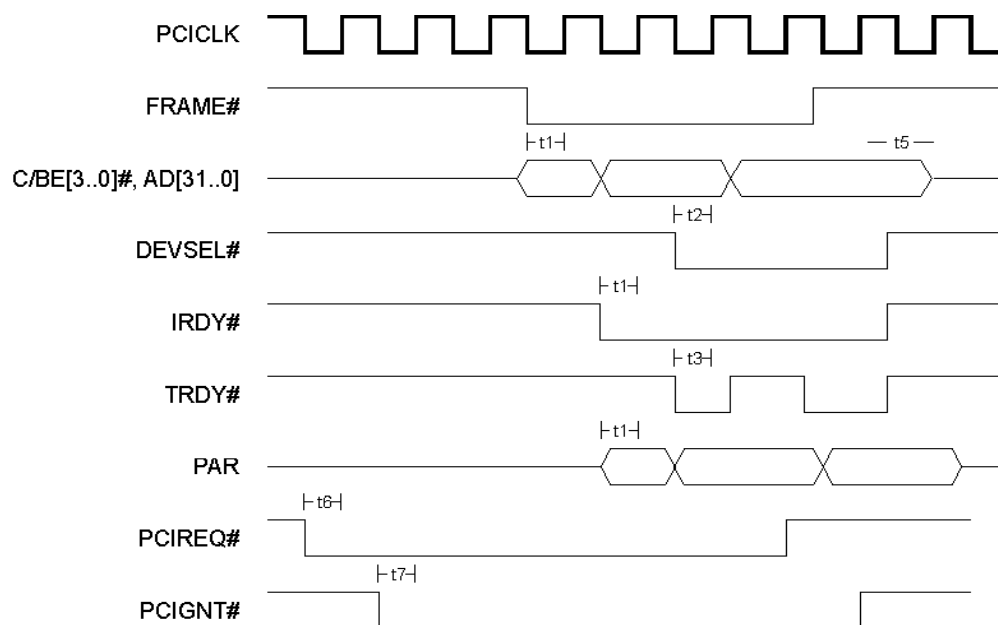
Symbol	Parameter	Timing
t16	DCS0#, DCS1#, DSA[2..0] high to low from CLK high	6-21 ns
t17	DCS0#, DCS1#, DSA[2..0] low to high from CLK high	5-18 ns
t18	DIOW#, DIOR# high to low from CLK high	5-18 ns
t19	DIOR#, DIOW# low to high from CLK high	5-17 ns
t20	DSD[15..0] to DIOW# setup time (2 CLKS)	45-56 ns
t21	DSD[15..0] to DIOW# hold time (2 CLKS)	50-57 ns
t22	DCS0# low to DIOW#, DIOR# low for port 1F0 (2CLKS)	52-59 ns
t23	DIOW#, DIOR# high to DCS0# high for port 1F0 (2CLKS)	53-60 ns
t24	IOCHRDY to CLK high setup time	2 ns

## 2.7 PCI DMA Master Read Timing (33MHz PCICLK)



See table in next section for an explanation of timing symbols.

## 2.8 PCI DMA Master Write Timing (33MHz PCICLK)



Symbol	Parameter	Timing
t1	FRAME#, IRDY#, C/BE[3..0]#, AD[31..0], PAR setup time	19-26 ns
t2	DEVSEL# setup time	7 ns
t3	TRDY# setup time	7 ns
t4	AD[31..0], FRAME#, IRDY#, C/BE[3..0]#, DEVSEL#, TRDY#, PAR, PCIREQ#, PCIGNT# hold time from rising edge of PCICLK.	0-11 ns
t5	Active to float delay from CLK	8-28 ns
t6	PCIREQ# setup time	18-25 ns
t7	PCIGNT# setup time	7 ns

# Appendix A Timing Settings Guide

This appendix is included to assist device driver developers in programming proper timing settings for the PCI646U2 chip.

## A.1 PCI Bus Speed and Clock Cycle

First, use the following table to determine the PCI bus speed of your system.

System Speed (MHz)	Likely bus speed (MHz)
66, 100, 133, 166, 200	33
60, 90, 120, 150	30
75	25

Use the bus speed from the previous table to determine the length of a clock cycle on the following table.

Likely bus speed (MHz)	Length of clock cycle (nsec)
33	30
30 <sup>2</sup>	33
25 <sup>1</sup>	40

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### NOTES

1) A PCI bus speed of 25MHz can only support Ultra DMA speed up to mode 1. The minimum cycle time for Ultra DMA mode 2 is 55ns; minimum cycle time for Ultra DMA mode 1 is 75ns. Each clock period for 25MHz is 40ns. The 646U2 needs a minimum of 1.5 PCI clocks (60ns in 25MHz) to detect a strobe from the drive. Therefore, at a PCI bus speed of 25MHz, the 646U2 can only support up to Ultra DMA mode 1.

2) A PCI bus speed of 30MHz is recommended for use up to Ultra DMA mode 1. The minimum cycle time for Ultra DMA mode 2 is 55ns; minimum cycle time for Ultra DMA mode 1 is 75ns. Each clock period for 30MHz is 33ns. The 646U2 needs a minimum of 1.5 PCI clocks to detect a strobe from the drive. If the PCI clock duty cycle is 50/50, then the 646U2 can support Ultra DMA mode 2. However, if the PCI clock duty cycle is 30/70, 1.5 PCI clocks can be 56.1ns. Therefore, at a PCI bus speed of 30MHz, it is recommended to use up to Ultra DMA mode 1.

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## A.2 Setting the Drive Mode

To determine what data transfer mode an ATA or ATAPI drive supports, you have to issue either an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command to the drive. Words 53 and 88 of identify device information will specify the fastest mode it supports. Refer to the ATA/ATAPI specification for a description of that information.

To set the drive to the desired data transfer mode, issue a SET FEATURE command to the drive. Refer to the ATA/ATAPI specification for a description of that command.

## A.3 Timing Table

The following table describes the minimum timing parameters required for different mode settings. All times are in nanoseconds (nsec).

Mode	Cycle Time	Address setup for DIOR/DIOW (ARTTIM register)	8-bit DIOR/DIOW active time (CMDTIM-active)	8-bit DIOR/DIOW recovery time (CMDTIM-recovery)	16-bit DIOR/DIOW active time (DRWTIM-active)	16-bit DIOR/DIOW recovery time (DRWTIM-recovery)
PIO 0	600	70	290	--	165	--
PIO 1	383	50	290	--	125	--
PIO 2	240	30	290	--	100	--
PIO 3	180	30	80	70	80	70
PIO 4	120	25	70	25	70	25
MDMA 0	480	*	*	*	215	265
MDMA 1	150	*	*	*	80	--
MDMA 2	120	*	*	*	70	--
UDMA 0	114	*	*	*	N/a	n/a
UDMA 1	75	*	*	*	N/a	n/a
UDMA 2	55	*	*	*	N/a	n/a

Since all access to task file registers are by PIO, you can calculate the values for the entries marked with "\*" based on the default PIO mode of the drive obtained from identify device information, even though the drive is programmed to do DMA data transfer. The entries marked with "--" mean there is no specified value. These values can be calculated by subtracting active time from cycle time.

### NOTE

In the above timing table, the sum of active time and recovery time may be greater or smaller than cycle time. The important point is that wherever applicable, cycle time, active time, and recovery time for any mode setting has to be equal or greater than the appropriate entry in the above table.

Once the drive mode is determined, program the PCI646U2 timing registers and other related registers as necessary. Ensure that the drive is set to the proper mode before programming the PCI646U2 timing registers.

### A.3.1 IDE Task File Timing Control Register (CMDTIM) at offset 0x52<sup>1</sup>

The following is a description of how timing registers should be programmed. This is based on a PCI bus speed of 33MHz and a clock cycle of 30 nsec.

The IDE task file registers must be accessed by PIO regardless of what data transfer type the drive is programmed to accept. There are some older drives that may not report correct data on the fastest PIO mode that they support. In these instances, it is safe to program the register based on the drive's default PIO mode.

If the default PIO mode of the drive is 2, this register should be programmed to 0xAF<sup>0</sup>. The upper 4 bits of this register represent an active time of 10 clocks (300nsec) which is the minimum time greater than 290nsec. The lower 4 bits represent a recovery time of 1 clock. There is no 0 clock of recovery time defined and the minimum is 1.

If the default PIO mode of the drive is 3, this register should be programmed to 0x32<sup>0</sup>. The upper 4 bits of this register represent an active time of 3 clocks (90nsec) which is the minimum time greater than 80nsec. The lower 4 bits represent a recovery time of 3 clocks (90nsec) which is the minimum time greater than or equal to 90nsec (cycle time – active time; or 180nsec – 90nsec = 90nsec.)

The time specified by this register constitutes a negligible portion to the whole data transfer time. Even if this register is programmed to the slowest PIO mode timing, it should have no performance penalty.

### A.3.2 Drive x Address Setup Register (ARTTIMx)

The **x** represents the drive number. If it is 0 or 1, it represents master or slave drive of primary channel respectively. If it is 2/3, it represents master/slave drive of secondary channel. This register reflects the address set up time for IDE Task File access. Like the CMDTIM register, this register has to follow PIO timing requirements, no matter what data transfer type the drive is programmed to.

If the default PIO mode of the device is 1, this register should be set to 0x40<sup>0</sup> (2 clocks). The 60nsec address set up time is greater than the minimum requirement of 50nsec for PIO mode 1. Drive 2 and drive 3 in the secondary channel share the same address setup count. Bit 6-7 of ARTTIM23 register should be programmed to the slower default PIO timing of the two drives.

The time specified by this register constitutes a negligible portion to the whole data transfer time. The performance difference is insignificant, even if this register is programmed to a longer time.

### A.3.3 Drive x Data Read/Write or DACK Timing Register (DRWTIMx) for PIO and Multi-word DMA

If the drive is set to Multiword DMA mode 2, this register should be programmed to 0x3F<sup>0</sup>. The upper 4 bits of this register represent an active time of 3 clocks (90nsec) which is the minimum time greater than 70nsec. The lower 4 bits represent a recovery time of 1 clock (30nsec) which is the minimum time greater than or equal to 30nsec (recovery time = cycle time – active time; or 120nsec – 90nsec = 30nsec.)

If the drive is set to PIO mode 4, this register should be programmed to 0x3F<sup>0</sup>. The upper 4 bits of this register represent an active time of 3 clocks (90nsec) which is the minimum time greater than 70nsec. The lower 4 bits represent a recovery time of 1 clock (30nsec) which is the minimum time greater than or equal to PIO mode 4 recovery time (25nsec). The sum of active and recovery time equals cycle time.

### A.3.4 Ultra DMA IDE Timing Control Register (UDIDETCRx) for Ultra DMA

This register is used only when the drive is set to run in Ultra DMA mode. If this register is used for a certain drive, the corresponding DRWTIM register for that drive will be invalid. Set bit 0 and/or bit 1 of this register depending on which drive(s) you want to interface with in Ultra DMA timing.

If the master drive is set to UDMA mode 2, bit 4-5 should be programmed to 01<sub>b</sub><sup>•</sup> (2 clocks / 60nsec) and is the minimum time greater than the 55nsec cycle time for UDMA mode 2.

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**NOTE**

Unless otherwise indicated all data content is shown in Hexadecimal. <sub>b</sub> indicates data content in Binary.

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## Appendix B Cable Limitations for Ultra DMA Mode Two with Four Drives

One objective in the development of the PCI646U2 was a low pin-count package. This was accomplished in a 100-pin PQFP package by sharing the data lines of the two IDE channels. Instead of the traditional daisy-chain cable configuration (figure 1), the chip and the devices can now be connected in a “Y-shape” cable configuration (figure 2). Because the “Y-shape” cable configuration connects to a single port, the total cable length combining both the Primary and Secondary channels ( $C1+C2$ ) should not exceed 18 inches in accordance with the IDE Specification.

**Although not advised**, testing has demonstrated that two cables with a total length of 24 inches ( $C1+C2$ ) may be used with both of the IDE channels fully loaded with four devices and running Ultra 33 mode 2. A combined length of 36 inches ( $C1+C2$ ) has been tested without problems, but only with one drive on each channel and running Ultra 33 mode 2. These limitations are caused by reflections generated by signals travelling in the longer cables. The IDE bus signal quality is significantly degraded by such reflections as the total cable length increases. This limitation has only been observed in Ultra DMA Mode two only. This cable limitation does not apply to Ultra DMA mode zero, mode one, all of the Multiword DMA (Enhanced IDE) modes and all of the PIO modes.

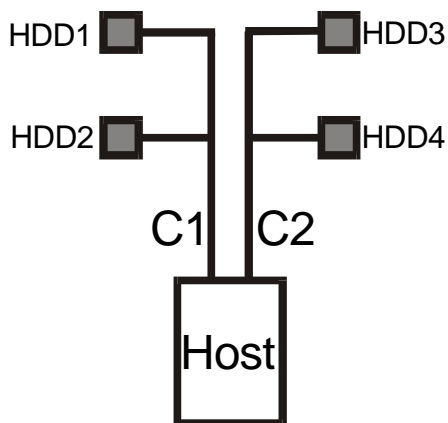


Figure 1

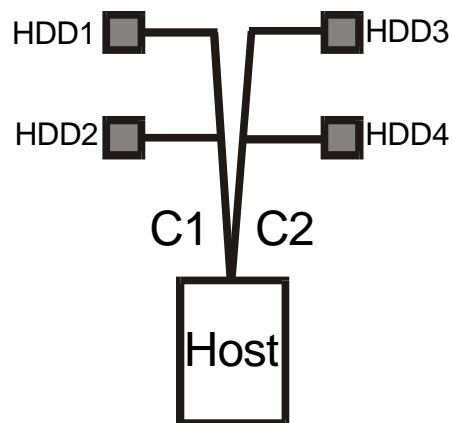


Figure 2



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